

Letter

A 1 V 92 dB SNDR 10 kHz Bandwidth Second-Order Asynchronous Delta-Sigma Modulator for Biomedical Signal Processing

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Abstract: In this paper, a second-order asynchronous delta-sigma modulator (ADSM) is proposed based on the active-RC integrators. The ADSM is implemented in the 0.18 μm CMOS Logic or Mixed-Signal/RF, General Purpose process from the Taiwan Semiconductor Manufacturing Company with a center frequency of 848 kHz at a supply voltage of 1 V with a 92 dB peak signal-to-noise and distortion ratio (SNDR), which corresponds to 15 bit resolution. These parameters were achieved in all the endogenous bioelectric signals bandwidth of 10 kHz. The ADSM dissipated 295 μW and had an area of 0.54 mm^2 . The proposed ADSM with a high resolution, wide bandwidth, and rail-to-rail input voltage range provides the universal solution for endogenous bioelectric signal processing.

Keywords: asynchronous delta-sigma modulator (ADSM); center frequency; operational amplifier; biomedical signals; biosensors

1. Introduction

Biomedical electronics have acquired significant attention in healthcare, with a focus on the development of biosensors that enable online monitoring, detection, prevention, and personalized medicine for a variety of chronic and acute diseases. Especially in the last few years, there has been growing interest in the design of biomedical wireless sensors [1–3]. Biomedical signals can be subdivided into two major classes: (1) endogenous signals that arise from natural physiological processes and are measured within or on living creatures (e.g., (EOG), electroencephalogram (EEG), electrocardiogram (ECG or EKG), electromyogram (EMG), temperature, blood glucose, etc.) and (2) exogenous signals applied from the outside (generally noninvasively) to measure internal structures and parameters. Endogenous bioelectric signals are invariably small, ranging from single microvolts to over 100 mV. Their bandwidths range from DC to perhaps 10 kHz at most [4–7]. The voltage and frequency ranges of some common biopotential signals are shown in Figure 1.

A general biomedical system consists of an energy source, a differential amplifier, analog-to-digital conversion (ADC), digital signal preprocessing, and a communication subsystem. The ADC is one of the key building blocks, which enables converting analog signals from biomedical sensors to a digital format that can be easily processed and analyzed. For the design of the ADC, many authors choose the SAR architecture due to its suitability for low-power and low-voltage requirements [8–11]. Recently, delta-sigma ($\Delta\Sigma$) ADC has been gaining more and more popularity. Compared to other conversion techniques, $\Delta\Sigma$ ADCs cover the widest conversion region of the resolution-versus-bandwidth plane, providing the most efficient solution to digitize diverse types of signals in many different applications such as biomedical ones [12]. There exist two basic types of $\Delta\Sigma$ modulators: discrete-time (DTDSM) and continuous-time (CTDSM). The DTDSM is more

attractive for high-resolution applications due to its higher linearity and accuracy. On the other hand, less stringent amplifier speed specifications are required in CTDSM due to the absence of switches in the active-RC integrator, allowing achieving a higher speed of operation and lower power consumption. The asynchronous $\Delta\Sigma$ modulator (ADSM) can be considered as a special type of CTDSM. ADSM is simple, does not require any clocking, matches well with mainstream CMOS technology, and can operate at low current and supply voltages [13–15]. A comparison between DTDSM, CTDSM, and ADSM is shown in Table 1.

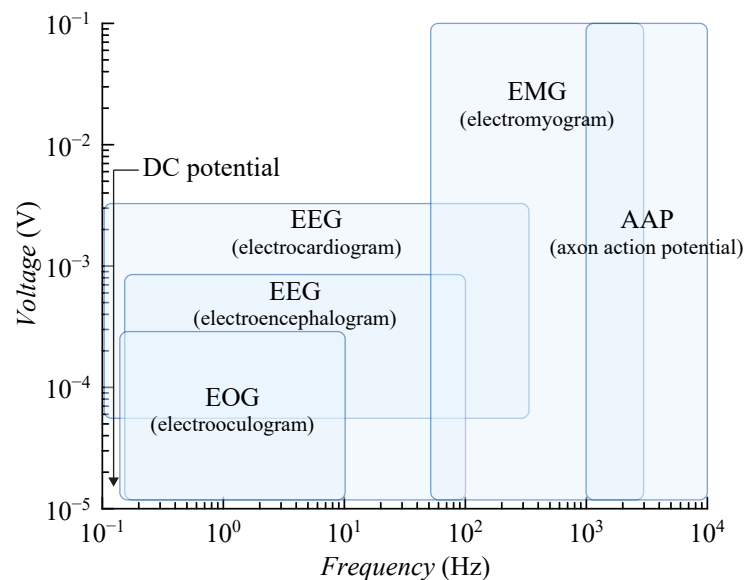


Figure 1. Voltage and frequency ranges of some common biopotential signals.

Table 1. Comparison between DTDSM, CTDSM, and ADSM.

DTDSM	CTDSM	ADSM
+ Synchronous system	+ Synchronous system	+ Immunity to clock jitter
+ High resolution	+ Implicit antialiasing filter	+ Implicit antialiasing filter
+ Highly linear SC integrator	+ Higher sampling frequency	+ Simple circuit
+ Accurately defined integrator gains and transfer function	+ Relaxed operational amplifier speed requirements	+ Relaxed OpAmp speed requirements
+ Low sensitivity to clock jitter and excess loop delay	+ Higher conversion speed	+ Higher conversion speed
+ Low sensitivity to DAC settling time	+ Low power	+ Low power
- Low conversion speed	- Sensitivity to clock jitter	+ Do not require a clock
- Required pre-antialiasing filter	- Excess loop delay	- Complex decoding scheme
- Required non-overlapping clock generator	- Lower resolution	- Lack of noise shaping
		- Lower resolution

In several publications, DTDSMs are used for biomedical signal processing [1,16,17]. There also exists solutions utilizing ADSM [18–20]. These ADSM are distinguished by very low power consumption in the order of tens of nanowatts. However, their bandwidth is very low in the order of tens of Hertz. The proposed ADSM covers the full bandwidth of endogenous bioelectric signals up to 10 kHz. The differential input range equals V_{DDA} with a 0.5 V reference level (V_{CM}). The proposed ADSM with high resolution, wide bandwidth, and rail-to-rail input voltage range provides the universal solution for endogenous bioelectric signal processing. The circuit not only offers an alternative to the developed CTDSMs and DTDSMs, but it also fills the gap between published ADSMs, which do not allow processing the full spectrum of biomedical signals according to Figure 1 except for those with a very high bandwidth in the order of MHz. An important parameter of ADSM is the center frequency, the calculation of which is part of this work. The following sections provide the details of our approach.

2. Asynchronous Delta-Sigma Modulator

There are two major types of architecture for $\Delta\Sigma$ modulators. The first one is the single-loop and the second the multi-loop architecture. Multi-loop architectures are commonly denoted as cascade or MASH (multi-stage noise shaping). A major drawback of MASH modulators is that precise matching of the analog and digital signal processing paths is required to avoid large errors (quantization noise leakage) caused by integrator gain coefficient variations. Because RC integrators are used in this design, where variations of about 20% in the RC time constant can be expected, the single-loop architecture was chosen in this work. Its stronger ability to achieve high SNDR since it does not suffer from matching errors, which severely affect MASH modulators, is the major advantage in the design.

The block diagram of the second-order ADSM based on the cascade of integrators with distributed feedback (CIFB) topology is shown in Figure 2.

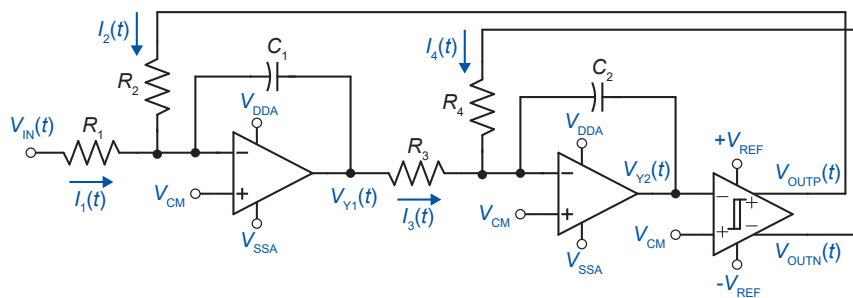


Figure 2. Simplified schematic of the second-order ADSM with the CIFB topology.

The circuit consists of two integrators and a binary quantizer with hysteresis. The output V_{OUTP} (or V_{OUTN}) is a pulse width modulated square wave of period T_{PER} with a pulse width T_{PW} . The duty cycle d is proportional to the amplitude of the input signal (Equation (1)). Moreover, the period T_{PER} of the asynchronous modulator output signal is modulated by the normalized input voltage V_{IN} (Equation (2)) [21].

$$d = \frac{V_{IN} + 1}{2} = \frac{T_{PW}}{T_{PER}} \quad (1)$$

and:

$$\frac{f_0}{f_c} = 1 - V_{IN}^2 \quad \text{and} \quad |v| < 1 \quad (2)$$

where f_0 is the output carrier frequency, f_c is the maximum value of f_0 , namely the center frequency, and $|V_{IN}| < 1$ is the normalized input amplitude.

The center frequency of ADSMs determines the carrier-to-bandwidth ratio ($CBR = f_c/(2B)$, where B is the input signal bandwidth), which is the ratio between the center frequency and the signal bandwidth. This ratio is equal to the oversampling ratio (OSR) in synchronous delta-sigma modulators. It determines the minimal center frequency required for a certain conversion accuracy. The critical condition can occur when V_{IN} is close to the full scale. The output frequency will decrease, and the high-frequency distortions around the center frequency shift to the low-frequency region. Consequently, distortions can leak into the baseband and adversely affect the modulator linearity for large input amplitudes. Therefore, the center frequency should be set far away from the baseband to avoid these components shifting into the signal baseband, and a high order filter is required to attenuate these out-band components. In order to achieve a high center frequency without degeneration of the linearity, the second-order topology was chosen. To calculate the center frequency of the proposed ADSM, the integrators' output voltages are expressed as:

$$V_{Y1}(t) = - \left(\frac{I_1(t)}{C_1} + \frac{I_2(t)}{C_1} \right) t + V_{CM} \quad (3)$$

$$V_{Y2}(t) = - \left(\frac{I_3(t)}{C_2} + \frac{I_4(t)}{C_2} \right) t + V_{CM} \quad (4)$$

where $I_1(t)$, $I_2(t)$, $I_3(t)$, and $I_4(t)$ can be expressed as:

$$I_1(t) = \frac{V_{IN}(t) - V_{CM}}{R_1} \quad (5)$$

$$I_2(t) = \frac{V_{REF}(t) - V_{CM}}{R_2} \quad (6)$$

$$I_3(t) = \frac{V_{Y1}(t) - V_{CM}}{R_3} \quad (7)$$

$$I_4(t) = \frac{V_{REF}(t) - V_{CM}}{R_4} \quad (8)$$

In order to find the center frequency, the timing diagram in Figure 3 is considered, which corresponds to the schematic in Figure 2.

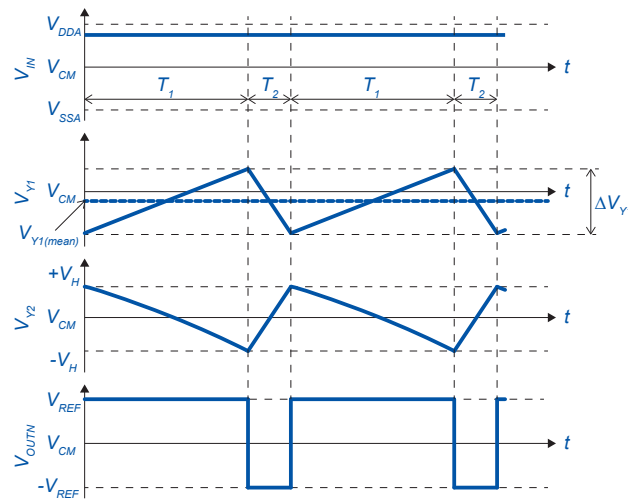


Figure 3. Timing diagram of the asynchronous sigma delta modulator with a constant input.

The duty cycle of the ADSM is given by the ratio of rising (S_{RE})-to-falling edge (S_{FE}) speed. To facilitate the equations, a symmetrical power supply is considered ($V_{DDAs} = V_{DDA} - V_{CM}$, $V_{CM} = 0$ V, $V_{SSAs} = V_{SSA} - V_{CM}$, $V_{REF} = V_{DDAs} = |V_{SSAs}|$; $|V_{HL} - V_{CM}| = V_{HH} - V_{CM} = V_H$). During the T_1 period, the output voltage of the first integrator V_{Y1} rises with speed, given by:

$$S_{RE1} = \frac{dV_{Y1}}{dt} = \frac{I_1 + I_2}{C_1} = \frac{V_{IN}R_2 + V_{REF}R_1}{R_1R_2C_1} \quad (9)$$

and the falling edge during T_2 :

$$S_{FE1} = \frac{dV_{Y1}}{dt} = \frac{I_1 + I_2}{C_1} = \frac{V_{IN}R_2 - V_{REF}R_1}{R_1R_2C_1} \quad (10)$$

The first integrator output voltage swing is in the range of:

$$\Delta V_{Y1} = V_{Y1(mean)} \pm |V_H| \frac{I_2}{I_4} \quad (11)$$

where V_H is the comparator threshold voltage.

In order to find $V_{Y1(mean)}$, we calculate $I_{3(mean)}$. The duty cycle of the second integrator output V_{Y2} is the same as the first one. From Equations (9) and (10), the value of $I_{3(mean)}$ is calculated to meet the duty cycle requirements.

$$I_{3(mean)} = \frac{V_{Y1(mean)}}{R_3} = -\frac{V_{IN}R_2}{R_1R_4} \quad (12)$$

For period T_1 , we can write:

$$T_1 = \frac{2V_H R_1 R_4 C_2}{R_1 V_{REF} - V_{IN} R_2} \quad (13)$$

$$T_2 = \frac{2V_H R_1 R_4 C_2}{R_1 V_{REF} + V_{IN} R_2} \quad (14)$$

The entire period can be expressed as:

$$T_{PER} = T_1 + T_2 \quad (15)$$

When a zero input is applied $V_{IN} = 0$, the output of the ADSM is a square wave with a duty cycle of 50%. By defining T_C as the period of the output signal, it can be calculated as:

$$T_C = T_{PER} = 2T_1 = 2T_2 = \frac{4V_H R_4 C_2}{V_{REF}} \quad (16)$$

Similar to the conventional synchronous CTDSMs, propagation delay is also an issue in ADSMs. The delay of the comparator increases the effective value of hysteresis and negligibly affects the center frequency of the ADSM. Therefore, the impact of the comparator delay, τ , on the center frequency of the proposed ADSM can be given by:

$$T_C = T_{PER} = 2T_1 = 2T_2 = \frac{1}{f_C} = \frac{4V_H R_4 C_2}{V_{REF}} + \tau \quad (17)$$

Equation (17) shows that the center frequency f_C of the modulator will decrease for a higher delay of the comparator, which degenerates the input bandwidth and linearity of the modulator [20].

3. Transistor Level Realization

In this section, the transistor level implementation of the ADSM will be described. Figure 4 illustrates the circuit diagram of the proposed ADSM. The implemented architecture is fully differential to minimize even-order harmonics, as well as common-mode noise.

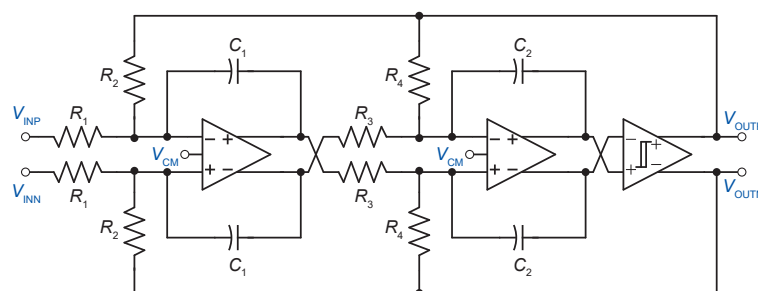


Figure 4. Proposed second-order asynchronous delta-sigma modulator.

3.1. Active-RC Integrator

In the proposed design, the active-RC integrators were used due to simplicity, high linearity, parasitic insensitivity, as well as the overall power consumption. The ideal transfer function of the active-RC integrator is given by:

$$Int(s) = \frac{1}{sRC} = k_i \frac{f_s}{s} \quad (18)$$

where f_s is the sampling frequency and k_i is the scaling coefficient.

The parameters of the resistors and capacitors were designed to achieve a high center frequency according to Equation (16). The lower limit for R and C is defined by matching consideration and maximum charging current in the case of R . The upper limit for R is set by the allowed thermal noise level, which itself is fixed by the overall dynamic range requirements. Finding optimal R and C was also confirmed by behavioral simulations in MATLAB/Simulink, as well as variations of about 20% in the RC time constant. The R and C values were $R_1 = 650 \text{ k}\Omega$, $R_2 = R_4 = 500 \text{ k}\Omega$, $R_3 = 357 \text{ k}\Omega$, $V_H = 90 \text{ mV}$, $C_1 = C_2 = 2 \text{ pF}$, and $I_R = 1 \text{ }\mu\text{A}$. It can be calculated from Equation (16) that $f_C = 1.39 \text{ MHz}$, and from Equation (11), $V_{Y1(\text{mean})} = (0 \pm 90) \text{ mV}$. The validity of these results was verified in MATLAB/Simulink and is shown in Figure 5.

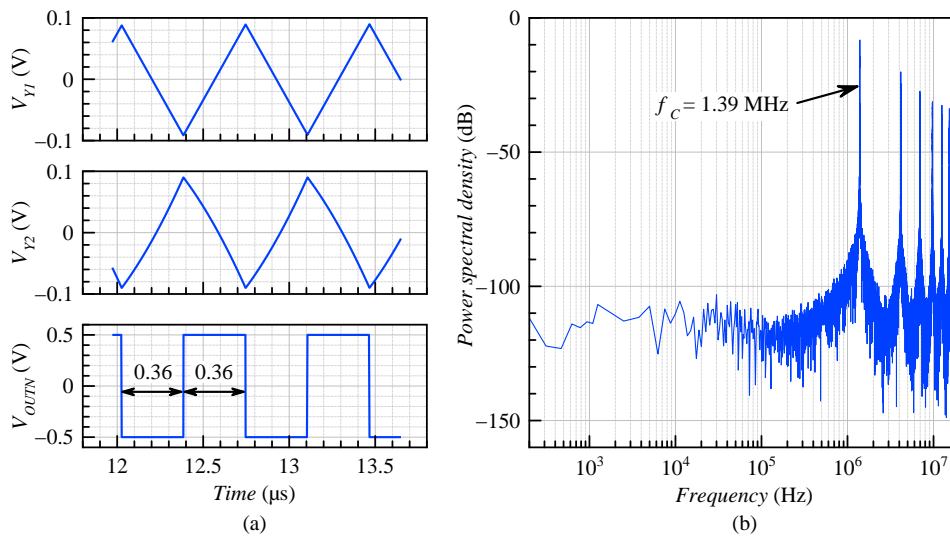


Figure 5. MATLAB model simulation results: (a) timing diagram and (b) frequency spectrum of the ADSM for $V_{IN} = 0 \text{ V}$.

As will be seen later, nonidealities such as input parasitic capacitances of the operational amplifier and the delay of the comparator negligibly affect the center frequency of the modulator.

3.2. Class AB Fully Differential Operational Amplifier

The integrators in the ADSM were each implemented using the two-stage, Class A/AB operational amplifier topology shown in Figure 6. This topology combines a simple differential pair as the first stage with a Class A/AB second stage, wherein push-pull operation is implemented using current mirrors [22]. The slew-rate is limited only by the first stage.

$$SR = \frac{I_5}{C_{C1} + C_{G6} + C_{G13}} \quad (19)$$

The minimum value of the operational amplifier slew-rate can be determined from the falling edge speed of V_{Y2} (S_{FE2}) according to Figure 3. The input parasitic capacitance of the comparator (C_{comp}) should be included in the calculations. Thus,

$$|S_{FE2}| = \frac{dV_{Y2}}{dt} = \frac{I_3 + I_4}{C_2 + C_{comp}} = \frac{V_{Y1}R_4 + V_{REF}R_3}{R_3R_4(C_2 + C_{comp})} \quad (20)$$

The use of PMOS input transistors makes it possible to avoid the body effect. The compensation network is comprised of capacitor C_C and resistor R_M , which cancels the right half plane zero.

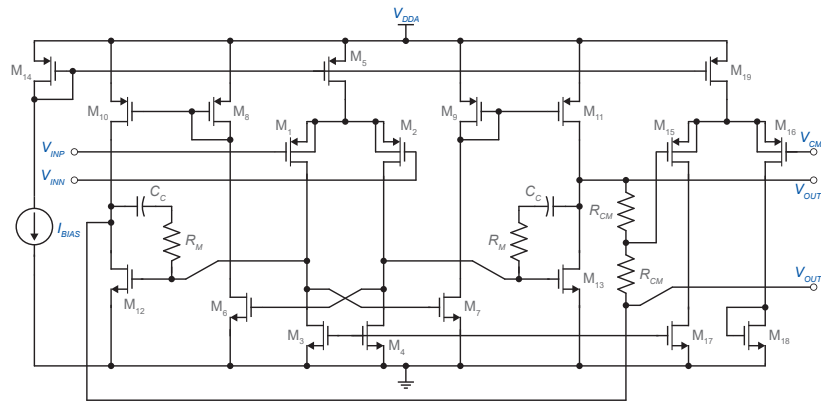


Figure 6. Circuit schematic of the two-stage Class A/AB operational amplifier.

For the detection of the common-mode output voltage, two equal resistors were used ($R_{CM} = 500\text{ k}\Omega$). The voltage between the two resistors is subtracted from the desired common-mode output voltage, V_{CM} , and scaled by the one-stage differential amplifier that consists of source-coupled pair M_{15} – M_{16} , diode-connected loads M_{17} and M_{18} , and tail current source M_{19} . The main reason for using this solution is that the input to the common-mode sense amplifier (gate of M_{15}) is almost constant. Therefore, this CMFB solution does not limit the operational amplifier output voltage swing. Table 2 sums up the simulated parameters of the operational amplifier used in the integrators.

Table 2. Simulated parameters for the operational amplifier ($C_L = 3\text{ pF}$).

Parameter	Condition	Value
Hysteresis	$ V_{TH} = V_{TL} $	90 mV
Time delay	$C_L = 3\text{ pF}$	50 ns
Slew-rate	$C_L = 3\text{ pF}$	42 V/ μs
Power consumption	duty cycle = 50%	5 μW
Input capacitance		0.4 pF
I_{BIAS}		2.5 μA

3.3. Comparator with Hysteresis

The schematic of a comparator using the internal positive feedback circuit is given in Figure 7. The comparator consists of a differential pair (M_1 – M_2) with output inverters in order to achieve reasonable voltage swings, output resistance, and differential output. A second, smaller differential pair, M_6 – M_7 , unbalances the input differential pair. The inputs of the second differential pair are tied to the output signals in such a way as to introduce positive feedback and, hence, hysteresis.

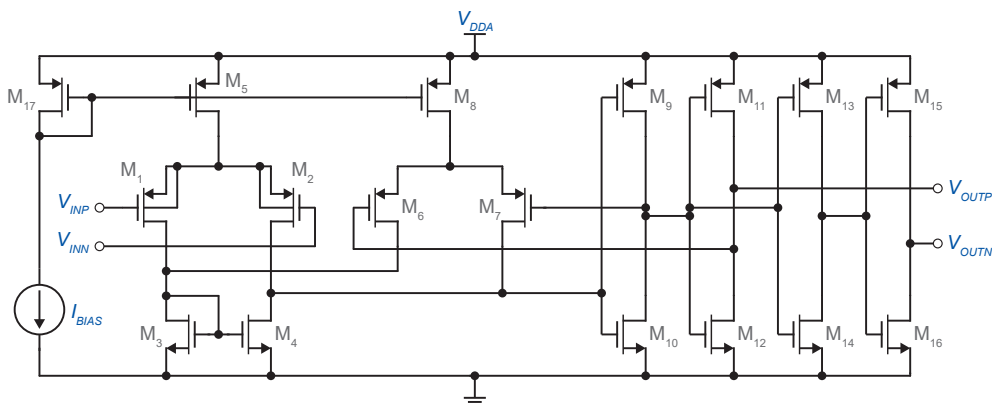


Figure 7. Comparator with hysteresis using an unbalanced differential pair.

If M_1 and M_2 are operating in strong inversion, the amount of hysteresis $V_{TH} - V_{TL}$ can be calculated using [23]:

$$V_{TH} - V_{TL} = \frac{2(\sqrt{I_{D3} + I_{D11}} - \sqrt{I_{D3} - I_{D11}})}{\sqrt{\mu C_{OX}(W/L)_1}} \quad (21)$$

If M_1 and M_2 are operating in weak inversion,

$$V_{TH} - V_{TL} = 4nU_T \tanh^{-1}(I_{D11}/I_{D3}) \quad (22)$$

Assume that the gate of M_1 (V_{INP}) is tied to V_{DDA} . With the input of M_2 (V_{INN}) much less than V_{DDA} , M_1 is off and M_2 on, and V_{OUTP} is at V_{DDA} and V_{OUTN} at V_{SSA} , thus turning on M_7 and turning off M_4 and M_6 . In this state, no current flows through the differential pairs. As the voltage at the V_{INP} input decreases toward the threshold point (Equations (21) or (22)), some of I_{D5} begins to flow through M_1 and M_3 , and simultaneously, some of the hysteresis bias current I_{D8} begins to flow through M_4 . This continues until the point where the current through M_1 equals the current I_{D8} . Just beyond this point, the comparator switches its state.

Figure 8 shows the voltage transfer characteristic of the comparator. The hysteresis bias current I_{D8} was $6.8 \mu\text{A}$, and the input bias current I_{D5} was $10 \mu\text{A}$. The output high-to-low threshold, V_{TL} , was simulated as -90 mV . The output low-to-high threshold, V_{TH} , was simulated as $+90 \text{ mV}$. The amount of hysteresis was 180 mV . Simulated parameters of the comparator circuit are given in Table 3.

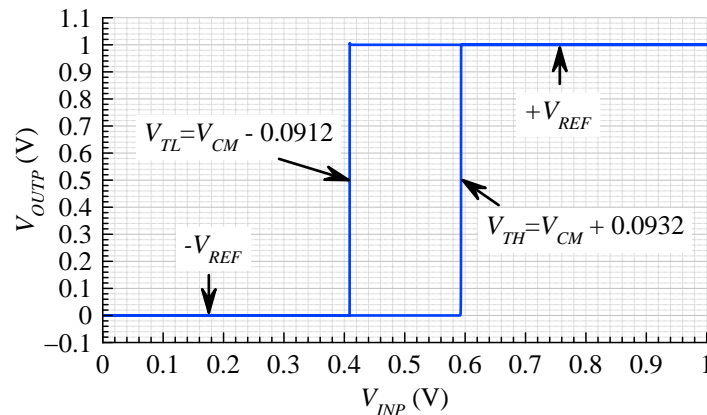


Figure 8. Simulated DC transfer characteristic of the comparator.

Table 3. Simulated parameters for the comparator.

Parameter	Condition	Value
Hysteresis	$ V_{TH} = V_{TL} $	90 mV
Time delay	$C_L = 3 \text{ pF}$	50 ns
Slew-rate	$C_L = 3 \text{ pF}$	42 V/ μs
Power consumption	duty cycle = 50%	5 μW
Input capacitance		0.4 pF
I_{BIAS}		2.5 μA

According to parameters mentioned in Tables 2 and 3, the center frequency was recalculated to $f_C = 857 \text{ kHz}$.

4. Simulation Results

The ADSM was designed utilizing the $0.18 \mu\text{m}$ CMOS Logic or Mixed-Signal/RF, General Purpose process from the Taiwan Semiconductor Manufacturing Company. The circuit was designed for $V_{DD} = 1 \text{ V}$ and $I_{BIAS} = 2.5 \mu\text{A}$. After completion of the layout design, its parasitic extraction was

performed to find the parasitic resistances and capacitances corresponding to the designed devices and interconnects. After parasitic extraction, all simulations were performed using the Spectre simulator on the Cadence platform. The layout of the ADSM is shown in Figure 9. The layout size is $350 \times 155 \mu\text{m}$.

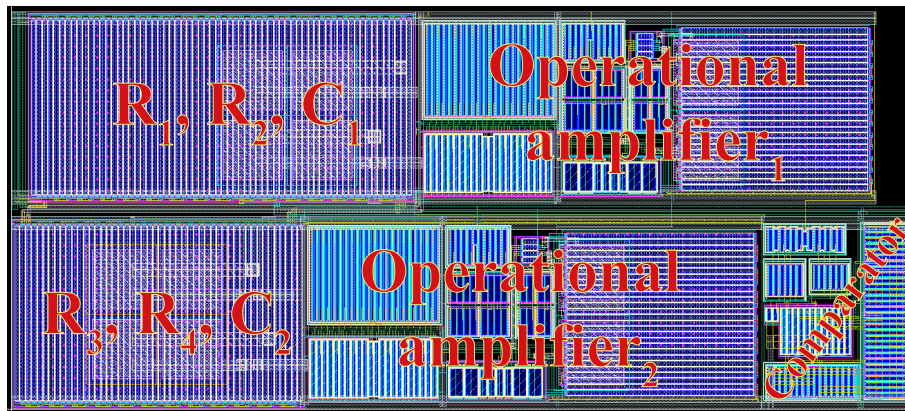


Figure 9. Layout of the proposed ADSM.

The ADSM output bitstream can be recovered by applying an ideal low pass filter with a cut-off frequency at the signal bandwidth. When ADSMs are used in A/D data conversion, a decoding circuit is required. The simplest one is the sample and hold circuit with a high sampling frequency. The time domain waveforms of the output signal V_{OUTN} for $V_{IN} = 0 \text{ V}$ and the corresponding frequency spectrum are shown in Figure 10. The limit cycle frequency of the post-layout model of the ADSM was equal to 848 kHz and was very close to the calculated value in Section 3.3 ($f_C = 857 \text{ kHz}$). The small difference was caused by the parasitic capacitances and resistances extracted from the layout.

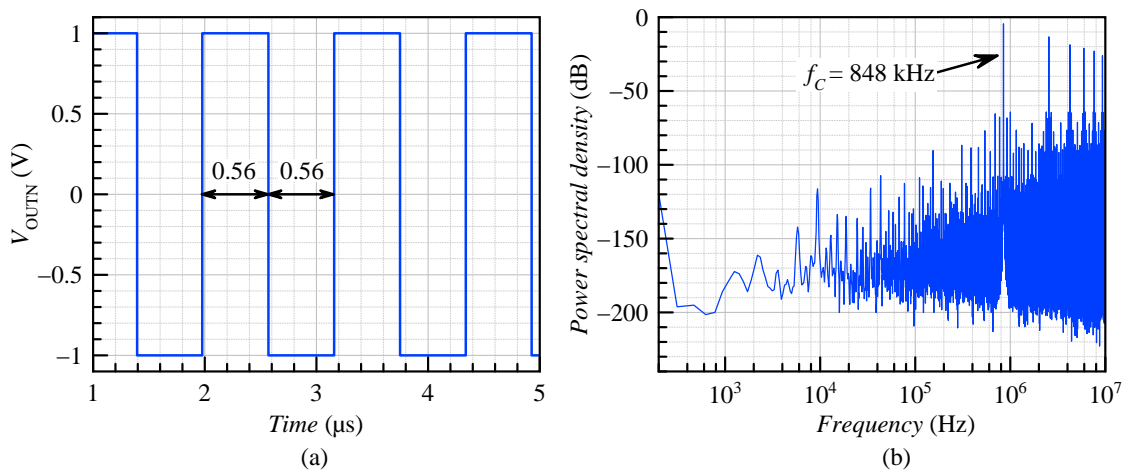


Figure 10. Post-layout simulation results: (a) timing diagram and (b) frequency spectrum of the ADSM for $V_{IN} = 0 \text{ V}$.

Figure 11 shows the simulated spectrum of the ADSM for a sinusoidal input signal with an amplitude of (a) 100 mV (20% modulation depth) and (b) 500 mV (100% modulation depth). The corresponding spectra were obtained by applying a signal at $f_{IN} \leq f_{Bandwidth}/3$ to include at least the second and third harmonic inside the band of interest. Due to this reason, the input frequency was set to 3.125 kHz, and then the third harmonic component was located in the 10 kHz bandwidth. The achieved SNDR was (a) 91.84 dB and (b) 78.13 dB. In the second case, the significant SNDR reduction was caused by higher harmonic tones.

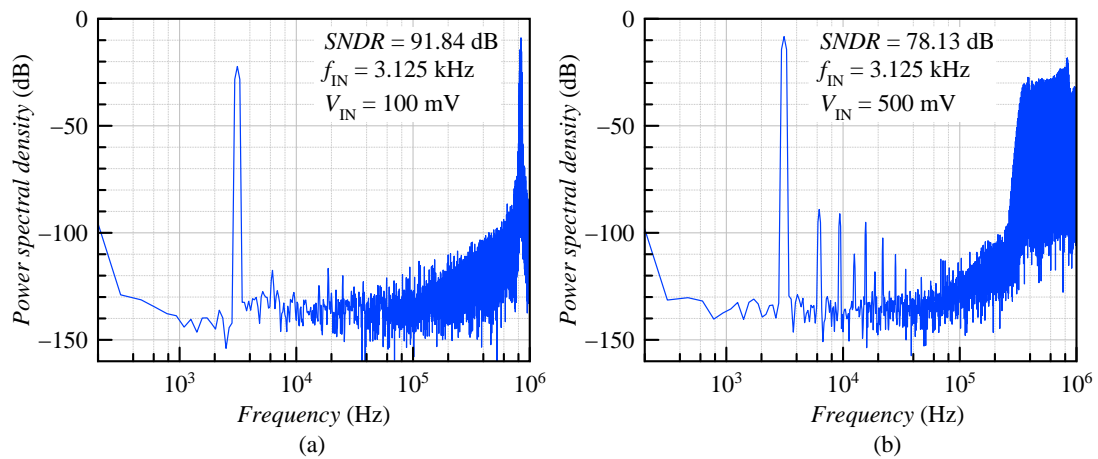


Figure 11. PSD of the ADSM for the sinusoidal input signal with an amplitude of (a) $V_{IN} = 100$ mV and (b) $V_{IN} = 500$ mV.

Figure 12a shows the simulated dynamic range (DR) with respect to the amplitude of the input signal with a frequency of both 3.125 kHz and 6.25 kHz. As the sine wave amplitude increased, the SNDR increased to reach the peak of 91.84 dB at -14 dBFS, and then dropped to 78.13 dB at 0 dBFS.

Figure 12b shows the SNDR vs. input signal frequency with an amplitude of both 100 mV and 500 mV. In the case of the input sine wave amplitude of 100 mV, the SNDR was above 88 dB for all frequencies up to the 10 kHz bandwidth. In the second case, the SNDR dropped from 110 dB to below 80 dB at frequencies smaller than 5 kHz ($f_{Bandwidth}/2$). This was because the second harmonic penetrated into the baseband and significantly reduced the SNDR. The dynamic range was equal to 112 dB.

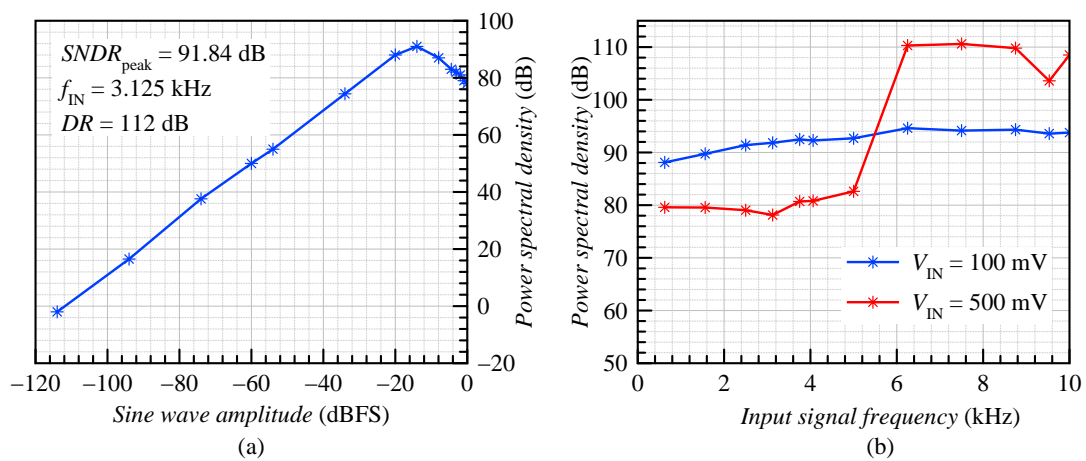


Figure 12. Plot of the SNDR vs. the (a) input sine wave amplitude and (b) input signal frequency.

Table 4 presents a comparison of the proposed ADSM with other DSMs, which are capable of processing endogenous bioelectric signals in the full frequency range. Two figures of merit (FOM_1 , FOM_2) are defined in Equations (23) and (24) for a better comparison. The first one emphasizes power consumption, whereas the second one emphasizes resolution. A better performance of DSMs is indicated by smaller FOM_1 and larger FOM_2 values.

$$FOM_1 = \frac{P_{cons}}{2^{ENOB} 2BW} \quad (23)$$

$$FOM_2 = DR + 10 \log \frac{BW}{P_{cons}} \quad (24)$$

Table 4. Specifications of the proposed ADSM in comparison with other DSMs.

Parameter	This Work	[24] 2015	[25] 2016	[26] 2018	[27] 2012
Technology	180 nm	130 nm	65 nm	65 nm	130 nm
Topology	ADSM	DTDSM	CTDSM	DTDSM	DTDSM
Order	2	3	3	3 (2-1 MASH)	3
Quantizer	1 bit	1 bit	5 bit	1 bit	1 bit
Supply voltage	1 V	0.4 V	1 V	1 V	0.25 V
Modulator frequency	848 kHz	3.2 MHz	6.4 MHz	5 MHz	1.4 MHz
Bandwidth	10 kHz	20 kHz	25 kHz	25 kHz	10 kHz
Peak SNDR	92 dB	76.1 dB	95.2 dB	94.6 dB	61 dB
Dynamic range	112 dB	82 dB	103 dB	98.5 dB	≅ 58 dB
Power consumption	290 μ W	63 μ W	800 μ W	175 μ W	7.5 μ W
Area	0.54 mm ²	0.33 mm ²	0.256 mm ²	0.384 mm ²	0.3375 mm ²
FOM_1	0.45 pJ/step	0.31 pJ/step	0.34 pJ/step	0.079 pJ/step	0.41 pJ/step
FOM_2	187 dB	167 dB	177.9 dB	176.2 dB	-

As can be concluded from Table 4, the proposed modulator offers a high SNDR and the best values of FOM_2 . Higher power consumption could be further improved utilizing a one-stage operational amplifier with much lower power consumption. The most attractive feature of ADSMs is the simple circuit architecture and clock-less operation. This feature can be very useful in applications in wireless sensors, where a decoding circuit (e.g., time-to-digital converter) is realized outside the integrated circuit.

5. Conclusions

This paper presents a second-order ADSM utilizing active-RC integrators. The circuit was designed in the 0.18 μ m CMOS Logic or Mixed-Signal/RF, General Purpose process from the Taiwan Semiconductor Manufacturing Company. Post-layout simulation was performed using the Spectre simulator on the Cadence platform. The proposed ADSM with a center frequency of 828 kHz achieves a 92 dB peak SNDR, while having a Walden FOM of 0.45 pJ/step and a Shreier FOM of 187 dB. These parameters together with a bandwidth of 10 kHz provide the universal solution for endogenous bioelectric signal processing. The overall power consumption is 295 μ W, while the chip area corresponds only to 0.54 mm².

Author Contributions: Conceptualization, V.K. and L.F.; methodology, V.K. and L.F.; validation, V.K., R.P., L.F. and J.H.; formal analysis, V.K. and J.H.; investigation, V.K., L.F., and R.P.; writing, original draft preparation, V.K.; writing, review and editing, V.K., L.F., and J.H. All authors have read and agreed to the published version of the manuscript.

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Abbreviations

The following abbreviations are used in this manuscript:

ADC	Analog-to-digital converter
ADSM	Asynchronous delta-sigma modulator
CBR	Carrier-to-bandwidth ratio
CIFB	Cascade of integrators with distributed feedback
CTDSM	Continuous-time delta-sigma modulator
DR	Dynamic Range
DTDSM	Discrete-time delta-sigma modulator
FOM	Figure-of-merit
MASH	Multi-stage noise shaping
SNDR	Signal-to-noise and distortion ratio

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