Voltage-Mode All-Pass Filters Using Universal Voltage Conveyor and MOSFET-Based Electronic Resistors

Norbert HERENCSAR[1], *Jaroslav KOTON*[1], *Jan JERABEK*[1], *Kamil VRBA*[1], *Oguzhan CICEKOGLU*[2]

[1]Dept. of Telecommunications, Brno University of Technology, Purkynova 118, 612 00 Brno, Czech Republic
[2]Dept. of Electrical and Electronic Engineering, Bogazici University, 34342-Bebek-Istanbul, Turkey

herencsn@feec.vutbr.cz, koton@feec.vutbr.cz, jerabekj@feec.vutbr.cz, vrbak@feec.vutbr.cz, cicekogl@boun.edu.tr

Abstract. *The paper presents two novel realizations of voltage-mode first-order all-pass filters. Both circuits use single universal voltage conveyor (UVC), single capacitor, and two grounded resistors. Using the two NMOS transistors-based realizations of the electronic resistor with two symmetrical power supplies, presented all-pass filter circuits can be easily made electronically tunable. Proposed filter structures provide both inverting and non-inverting outputs at the same configuration simultaneously and they have high-input and low-output impedances that are desired for easy cascading in voltage-mode operations. The non-idealities of the proposed circuits are also analyzed and compared. The theoretical results of both circuits are verified by SPICE simulations using TSMC 0.35 μm CMOS process parameters. Based on the evaluation, the behavior of one of the circuits featuring better performance was also experimentally measured using the UVC-N1C 0520 integrated circuit.*

Keywords

All-pass filter, analog signal processing, MOSFET-C circuit, universal voltage conveyor, voltage-mode.

1. Introduction

First-order all-pass filters (APFs) are widely used to shift the phase of an input signal while keeping the amplitude constant over the frequency range of interest. For the voltage-mode (VM) all-pass filters high-input impedance is important, if these circuits are used as a load to another analog filter in the signal-processing path for compensating phase shifts. Due to this property, there is no need for an additional buffer or current conveyor for cascading which decreases the number of active elements in the design. In the current technical literature huge number of papers deal with VM APFs [1]–[14] (and the references cited therein), however, not all of them have high-input or low-output impedance, hence, are not suitable for cascading. For example, cascadable circuits in [1] and [2] employing differential voltage current conveyors (DVCCs) and grounded passive elements require critical capacitor matching condition that is definitely a disadvantage of these solutions. This is eliminated in circuits [3]–[5] that feature with high-input and low-output impedance. However, the disadvantage of the circuits proposed in [1]–[5] is that two active elements always have to be used, which is not that economical. In grounded capacitor-based all-pass filters using single dual-output second-generation CC [6] or single DVCC [7] resistor matching is required. All-pass filters in [8] and [9] using canonic number of passive and active elements (i.e. single resistor, single capacitor, and single DDCC) can be mentioned as example. Unfortunately, both circuits do not feature with high-input impedance. The resistorless VM APF using two DVCCs and a single grounded capacitor is presented in [10], however, it also suffers from a lack of high-input impedance. Another all-pass filter [11] employing DDCCs and grounded passive elements is cascadable and suitable for integrated circuit (IC) implementation, but the use of two active elements increases the chip area of the circuit. Papers [12]–[14] present such compact all-pass filters that realize both inverting and non-inverting responses simultaneously. All the mentioned circuits employ floating capacitors. The use of grounded capacitors in [1]–[7] and [9]–[11] can be seen as an advantage from easier IC implementation and absorbing parasitic capacitance points of view. However, using advanced IC technologies the floating capacitor can also easily be implemented. These new IC technologies offer a second poly layer (poly2), which also enables the realization of floating capacitors as double poly (poly1-poly2) capacitors [8]. A floating capacitor can also be implemented as metal-insulator-metal (MIM) capacitor [6]. They are standard today and commonly used in analog IC designs.

To the best of the authors' knowledge, from the mentioned circuits, only the solutions in [13] and [14] have high-input/low-output impedance and provide both inverting and non-inverting outputs at the same configuration simultaneously. Therefore, the aim of this paper is to present new such APFs that fulfill both above mentioned requirements. For this purpose the universal voltage conveyor (UVC) is used that is ideal for such circuit design due to its high-impedance voltage input and mutually inverse low-impedance voltage outputs. The behavior of the proposed circuits has been verified by SPICE and, furthermore, the circuit with better performance was also experimentally measured.

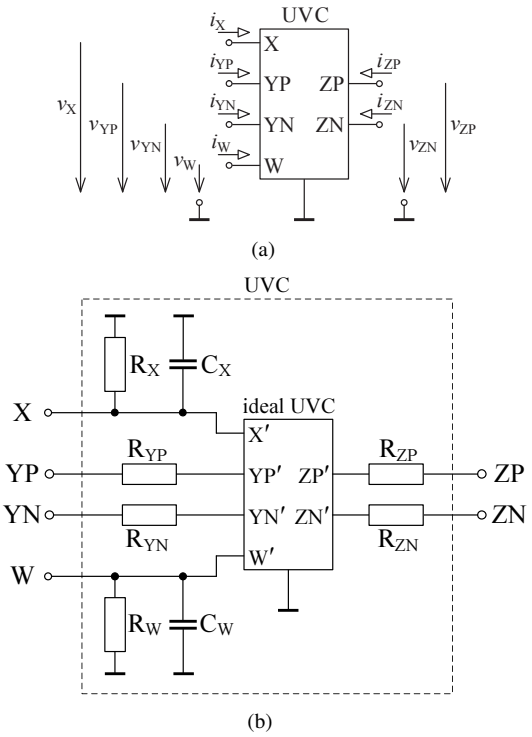

Fig. 1. (a) Circuit symbol of the UVC, (b) model of the UVC including parasitic elements.

Generation/type	Interconnected
xVCI	W and ZP
xVCII	W and ground
xVCIII	W and ZN

Tab. 1. Configuration of UVC to realize required generation of VC.

2. Voltage Conveyors

Voltage conveyors have been defined using the duality principle to current conveyors (CCs) in 1981 [15]. As in the theory of CCs, also here the first- and second-generation VCs (VCI, VCII, IVCI, and IVCII) were described [15]–[17]. The best known VC is the plus-type differential current voltage conveyor (DCVC+) [18] that is more often labeled as the current differencing buffered amplifier (CDBA) [19]. Recently, the current-controlled CDBA (CCCDBA) [20], inverting CDBA (ICDBA), and current-controlled ICDBA (C-ICDBA) have also been introduced [21].

Based on the idea of the "universal" active element [22] and also on the basis of the universal current conveyor (UCC) [23]–[29], the universal voltage conveyor (UVC) [13], [17], [26], [30]–[35] was designed and developed, using the CMOS 0.35 μm technology, under the designation UVC-N1C 0520 at our workplace, and produced in cooperation with AMI Semiconductor Czech, Ltd., (now ON Semiconductor Czech Republic, Ltd.). The circuit symbol of the UVC is shown in Fig. 1(a). It is defined as a six-port active element, which has one voltage input X, two difference current inputs (YP, YN), two mutually inverse voltage outputs (ZP, ZN), and one auxiliary port W. By connecting or grounding suitable terminals of the UVC, it helps to realize all existing types of voltage conveyors. In Tab. 1, only the generations are mentioned. Specific types of voltage conveyors can be found in [35]. From Tab. 1, the port W is generally used to determine the generation of the VC. However, it can be used as an independent input port of the active element. By the modification of the UVC the differential-input buffered and transconductance amplifier (DBTA) [36]–[38] has been defined.

Using standard notation, the relationship between port currents and voltages of a non-ideal UVC can be described by the following hybrid matrix:

$$\begin{bmatrix} i_{\mathrm{X}} \\ v_{\mathrm{YP}} \\ v_{\mathrm{YN}} \\ i_{\mathrm{W}} \\ v_{\mathrm{ZP}} \\ v_{\mathrm{ZN}} \end{bmatrix} = \begin{bmatrix} Y_{\mathrm{X}} & \alpha_1(s) & -\alpha_2(s) & 0 & 0 & 0 \\ 0 & Z_{\mathrm{YP}} & 0 & \delta_1(s) & 0 & 0 \\ 0 & 0 & Z_{\mathrm{YN}} & \delta_2(s) & 0 & 0 \\ 0 & 0 & 0 & Y_{\mathrm{W}} & 0 & 0 \\ \gamma_1(s) & 0 & 0 & 0 & Z_{\mathrm{ZP}} & 0 \\ -\gamma_2(s) & 0 & 0 & 0 & 0 & Z_{\mathrm{ZN}} \end{bmatrix} \cdot \begin{bmatrix} v_{\mathrm{X}} \\ i_{\mathrm{YP}} \\ i_{\mathrm{YN}} \\ v_{\mathrm{W}} \\ i_{\mathrm{ZP}} \\ i_{\mathrm{ZN}} \end{bmatrix}. \tag{1}$$

In (1), $Y_{\mathrm{X}} = sC_{\mathrm{X}} + 1/R_{\mathrm{X}}$, $Y_{\mathrm{W}} = sC_{\mathrm{W}} + 1/R_{\mathrm{W}}$ are parasitic admittances and $Z_k = R_k$ (k =YP, YN, ZP, ZN) are the parasitic resistances at relevant terminals of the UVC, respectively, as it is shown in Fig. 1(b). Parameter $\alpha_j(s)$ is frequency dependent non-ideal current gain, and $\delta_j(s)$ and $\gamma_j(s)$ are frequency dependent non-ideal voltage gains for $j = 1, 2$. Ideally they are equal to unity and using a single-pole model [39], they can be defined as:

$$\alpha_j(s) = \frac{\alpha_{oj}}{1 + \tau_{\alpha_j} s}, \tag{2a}$$

$$\delta_j(s) = \frac{\delta_{oj}}{1 + \tau_{\delta_j} s}, \tag{2b}$$

$$\gamma_j(s) = \frac{\gamma_{oj}}{1 + \tau_{\gamma_j} s}. \tag{2c}$$

Here, α_{oj} is DC current, δ_{oj} and γ_{oj} are DC voltage gains of the element, respectively. The bandwidths $1/\tau_{\alpha_j}$, $1/\tau_{\delta_j}$, and $1/\tau_{\gamma_j}$ depend on the fabrication of active devices and on the order of a few gigarad/s in current technologies are ideally equal to infinity. At low and medium frequencies i.e., $f \ll (1/(2\pi)) \times \min\{1/\tau_{\alpha_j},\ 1/\tau_{\delta_j},\ 1/\tau_{\gamma_j}\}$, (2a)–(2c) turn to:

$$\alpha_j(s) \cong \alpha_{oj} = 1 + \varepsilon_{\alpha_{ij}}, \tag{3a}$$

$$\delta_j(s) \cong \delta_{oj} = 1 + \varepsilon_{\delta_{v1j}}, \tag{3b}$$

$$\gamma_j(s) \cong \gamma_{oj} = 1 + \varepsilon_{\gamma_{v2j}}. \tag{3c}$$

whereas $\varepsilon_{\alpha_{ij}}$ is current tracking error, $\varepsilon_{\delta_{v1j}}$ and $\varepsilon_{\gamma_{v2j}}$ are voltage tracking errors that satisfy the following inequalities $|\varepsilon_{\alpha_{ij}}| \ll 1$, $|\varepsilon_{\delta_{v1j}}| \ll 1$, and $|\varepsilon_{\gamma_{v2j}}| \ll 1$.

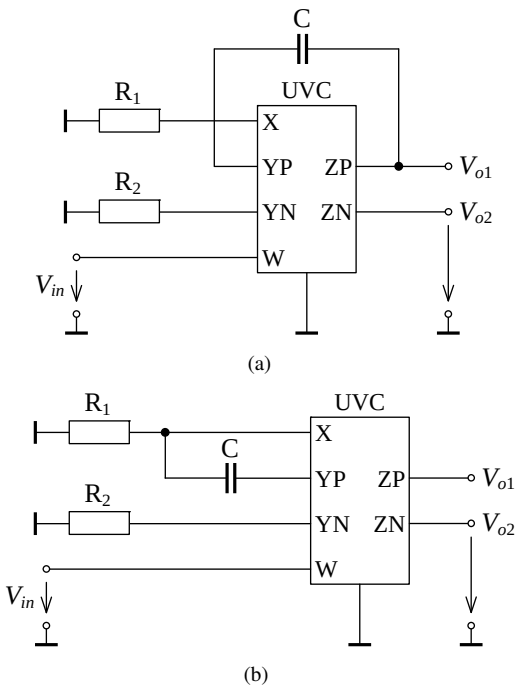

Fig. 2. Proposed all-pass filters.

3. Proposed All-pass Filters

Proposed VM first-order all-pass filters are shown in Fig. 2. Both circuits employ one UVC, two resistors and a capacitor as well. This Section deals with detailed evaluation of their performance.

3.1 First Proposed Circuit

Considering the ideal UVC and assuming $R_1 = R_2 = R$, for the first proposed circuit in Fig. 2(a) routine analysis yields voltage transfer functions in the following forms:

$$T_1(s) = \frac{V_{o1}}{V_{in}} = \frac{sCR-1}{sCR+1}, \tag{4a}$$

$$T_2(s) = \frac{V_{o2}}{V_{in}} = -\frac{sCR-1}{sCR+1}. \tag{4b}$$

As it is seen from these equations, both inverting (4a) and non-inverting (4b) output of VM first-order all-pass filter can be realized with the same circuit topology.

The phase responses of the filter are given as follows:

$$\varphi_1(\omega) = 180^\circ - 2\text{arctg}(\omega CR), \tag{5a}$$

$$\varphi_2(\omega) = -2\text{arctg}(\omega CR). \tag{5b}$$

Hence, the pole frequency can be found as $\omega_p = 1/(CR)$ and its sensitivity to passive elements is as $S^{\omega_p}_{C,R} = -1$. As it is seen from above equations, the proposed configuration can provide phase shifting both between 180° to 0° and 0° to -180°.

Taking into account the non-idealities of UVC, excluding parasitic resistances and capacitances, the proposed all-pass filter transfer functions (4a) and (4b) become:

$$T_1(s) = \frac{V_{o1}}{V_{in}} = \frac{\gamma_{o1}(\alpha_{o1}\delta_{o1}sCR - \alpha_{o2}\delta_{o2})}{\alpha_{o1}\gamma_{o1}sCR+1}, \tag{6a}$$

$$T_2(s) = \frac{V_{o2}}{V_{in}} = -\frac{\gamma_{o2}(\alpha_{o1}\delta_{o1}sCR - \alpha_{o2}\delta_{o2})}{\alpha_{o1}\gamma_{o1}sCR+1}. \tag{6b}$$

and the frequency dependent phase responses are given by:

$$\varphi_1(\omega) = 180^\circ - \text{arctg}\left(\frac{\alpha_{o1}\delta_{o1}\omega CR}{\alpha_{o2}\delta_{o2}}\right) - \text{arctg}(\alpha_{o1}\gamma_{o1}\omega CR), \tag{7a}$$

$$\varphi_2(\omega) = -\text{arctg}\left(\frac{\alpha_{o1}\delta_{o1}\omega CR}{\alpha_{o2}\delta_{o2}}\right) - \text{arctg}(\alpha_{o1}\gamma_{o1}\omega CR). \tag{7b}$$

Now, the zero ω_z and pole ω_p frequencies are not equal and can be expressed as:

$$\omega_z = \frac{\alpha_{o2}\delta_{o2}}{\alpha_{o1}\delta_{o1}CR}, \quad \omega_p = \frac{1}{\alpha_{o1}\gamma_{o1}CR}. \tag{8}$$

For an all-pass filter zero frequency ω_z is equally important as the pole frequency ω_p. Therefore, careful design of UVC will be needed.

The active and passive sensitivities of ω_z and ω_p are given as:

$$S^{\omega_z}_{\alpha_{o2},\delta_{o2}} = -S^{\omega_z}_{\alpha_{o1},\delta_{o1},C,R} = 1, \;\; S^{\omega_z}_{\gamma_{o1},\gamma_{o2}} = 0, \tag{9a}$$

$$S^{\omega_p}_{\alpha_{o1},\gamma_{o1},C,R} = -1, \;\; S^{\omega_p}_{\delta_{o1},\alpha_{o2},\delta_{o2},\gamma_{o2}} = 0. \tag{9b}$$

From (9a) and (9b) it is evident that the sensitivities of active and passive components for both zero ω_z and pole ω_p frequencies are unity in relative amplitude.

For a complete analysis of the circuit, it is also important to take into account the main parasitic impedances of the UVC. Considering parasitics shown in (1), except for the admittance Y_X, the ideal transfer functions (4a) and (4b) of the all-pass filter in Fig. 2(a) turn to:

$$T_1(s) = \frac{V_{o1}}{V_{in}} = \frac{\begin{array}{c} sC[\delta_{o1}(R_2+R_{YN})(\alpha_{o1}\gamma_{o1}R_1+R_{ZP})- \\ -\gamma_{o1}\alpha_{o2}\delta_{o2}R_{YP}R_1] - \gamma_{o1}\alpha_{o2}\delta_{o2}R_1 \end{array}}{(R_2+R_{YN})[sC(R_{YP}+R_{ZP}+\alpha_{o1}\gamma_{o1}R_1)+1]}, \tag{10a}$$

$$T_2(s) = \frac{V_{o2}}{V_{in}} = -\frac{\begin{array}{c} \gamma_{o2}R_1\{sC[\alpha_{o1}\delta_{o1}(R_2-R_{YN})+ \\ +\alpha_{o2}\delta_{o2}(R_{YP}-R_{ZP})] - \alpha_{o2}\delta_{o2}\} \end{array}}{(R_2+R_{YN})[sC(R_{YP}+R_{ZP}+\alpha_{o1}\gamma_{o1}R_1)+1]}, \tag{10b}$$

(10a) and (10b) show that the voltage gains at $\omega = 0$ are equal to $\gamma_{o1}\alpha_{o2}\delta_{o2}R_1/(R_2+R_{YN})$ and $\alpha_{o2}\delta_{o2}\gamma_{o2}R_1/(R_2+R_{YN})$, respectively, resulting in slightly modified gains. However, by good design of UVC and precise matching of resistors R_1 and R_2 the gain of the filter is equal to 1. From

(10) the non-ideal zero ω_z and pole ω_p frequencies including parasitics can be calculated as:

$$\omega_z = \frac{\gamma_{o1}\alpha_{o2}\delta_{o2}R_1}{C[\delta_{o1}(R_2+R_{YN})(\alpha_{o1}\gamma_{o1}R_1+R_{ZP})-\gamma_{o1}\alpha_{o2}\delta_{o2}R_{YP}R_1]}, \quad (11a)$$

$$\omega_p = \frac{1}{C(R_{YP}+R_{ZP}+\alpha_{o1}\gamma_{o1}R_1)}. \quad (11b)$$

From (11a) and (11b) it is clear that both zero ω_z and pole ω_p frequencies are affected by the parasitics and non-idealities of the active element used, however, they can be minimized by:

(i) making the α_{oj}, δ_{oj}, and γ_{o1} (for $j = 1,2$) very close to unity and/or,

(ii) choosing $R_1 \gg R_{ZP}$ and $R_{YP} \approx R_{YN}$ and/or,

(iii) choosing $R_1 \gg R_{YP}+R_{ZP}$.

3.2 Second Proposed Circuit

Assuming again $R_1 = R_2 = R$ for the second proposed circuit in Fig. 2(b) and considering the ideal UVC, straightforward analysis gives the following voltage transfer functions:

$$T_1(s) = \frac{V_{o1}}{V_{in}} = \frac{2sCR-1}{2sCR+1}, \quad (12a)$$

$$T_2(s) = \frac{V_{o2}}{V_{in}} = -\frac{2sCR-1}{2sCR+1}. \quad (12b)$$

From (12a) and (12b), the phase responses of the filter can be derived as:

$$\varphi_1(\omega) = 180^\circ - 2\text{arctg}(2\omega CR), \quad (13a)$$

$$\varphi_2(\omega) = -2\text{arctg}(2\omega CR), \quad (13b)$$

from which the pole frequency can be found as $\omega_p = 1/(2CR)$ and its sensitivity to passive elements is as $S^{\omega_p}_{C,R} = -1$. From the above equations it can be seen that the second proposed configuration also provides phase shifting both between 180° to 0° and 0° to –180°.

Assuming non-ideal UVC from (1), excluding parasitic resistances and capacitances, the proposed all-pass filter transfer functions (13a) and (13b) turn to be:

$$T_1(s) = \frac{V_{o1}}{V_{in}} = \frac{\gamma_{o1}[\delta_{o1}sCR(\alpha_{o1}+1)-\alpha_{o2}\delta_{o2}]}{sCR(1+\alpha_{o1})+1}, \quad (14a)$$

$$T_2(s) = \frac{V_{o2}}{V_{in}} = -\frac{\gamma_{o2}[\delta_{o1}sCR(\alpha_{o1}+1)-\alpha_{o2}\delta_{o2}]}{sCR(1+\alpha_{o1})+1}. \quad (14b)$$

The frequency dependent phase responses are given as follows:

$$\varphi_1(\omega) = 180^\circ - \text{arctg}\left(\frac{\delta_{o1}\omega CR(\alpha_{o1}+1)}{\alpha_{o2}\delta_{o2}}\right) - \\ -\text{arctg}[\omega CR(1+\alpha_{o1})], \quad (15a)$$

$$\varphi_2(\omega) = -\text{arctg}\left(\frac{\delta_{o1}\omega CR(\alpha_{o1}+1)}{\alpha_{o2}\delta_{o2}}\right) - \\ -\text{arctg}[\omega CR(1+\alpha_{o1})]. \quad (15b)$$

The zero ω_z and pole ω_p frequencies of the filter in Fig. 2(b) can be expressed as:

$$\omega_z = \frac{\alpha_{o2}\delta_{o2}}{\delta_{o1}CR(\alpha_{o1}+1)}, \quad \omega_p = \frac{1}{CR(1+\alpha_{o1})}, \quad (16)$$

that differ from each other again, as in the circuit from Fig. 2(a). Hence, to receive $\omega_z = \omega_p$ careful and precise design of UVC is needed to obtain unity current and voltage gains.

The active and passive sensitivities of ω_z and ω_p can be calculated as:

$$S^{\omega_z}_{\alpha_{o2},\delta_{o2}} = -S^{\omega_z}_{\delta_{o1},C,R} = 1, \; S^{\omega_z}_{\alpha_{o1}} = -\frac{\alpha_{o1}}{\alpha_{o1}+1}, \; S^{\omega_z}_{\gamma_{o1},\gamma_{o2}} = 0. \quad (17a)$$

$$S^{\omega_p}_{C,R} = -1, \; S^{\omega_p}_{\alpha_{o1}} = -\frac{\alpha_{o1}}{\alpha_{o1}+1}, \; S^{\omega_p}_{\delta_{o1},\gamma_{o1},\alpha_{o2},\delta_{o2},\gamma_{o2}} = 0. \quad (17b)$$

From (17a) and (17b) it is evident that the sensitivities of active and passive components for both zero ω_z and pole ω_p frequencies are again not larger than unity in relative amplitude. Hence, the second proposed filter also shows low sensitive performance.

Taking into account the main parasitic impedances of the UVC in (1), except for the admittance Y_X, the ideal transfer functions (12a) and (12b) change to:

$$T_1(s) = \frac{V_{o1}}{V_{in}} = \frac{\gamma_{o1}R_1\{sC[\delta_{o1}(R_2+R_{YN})(1+\alpha_{o1})- \\ -\alpha_{o2}\delta_{o2}R_{YP}]-\alpha_{o2}\delta_{o2}\}}{(R_2+R_{YN})\{sC[R_1(1+\alpha_{o1})+R_{YP}]+1\}}, \quad (18a)$$

$$T_2(s) = \frac{V_{o2}}{V_{in}} = -\frac{\gamma_{o2}R_1\{sC[\delta_{o1}(R_2+R_{YN})(1+\alpha_{o1})- \\ -\alpha_{o2}\delta_{o2}R_{YP}]-\alpha_{o2}\delta_{o2}\}}{(R_2+R_{YN})\{sC[R_1(1+\alpha_{o1})+R_{YP}]+1\}}. \quad (18b)$$

From Eqs. (18a) and (18b) can be seen that the voltage gains at $\omega = 0$ are equal to previous circuit ones, i.e. $\gamma_{o1}\alpha_{o2}\delta_{o2}R_1/(R_2+R_{YN})$ and $\alpha_{o2}\delta_{o2}\gamma_{o2}R_1/(R_2+R_{YN})$, respectively. By good design of UVC and for precisely matched resistors R_1 and R_2 the gain of the filter is equal to unity. The non-ideal zero ω_z and pole ω_p frequencies including parasitics can be calculated as:

$$\omega_z = \frac{\alpha_{o2}\delta_{o2}}{C[\delta_{o1}(R_2+R_{YN})(1+\alpha_{o1})-\alpha_{o2}\delta_{o2}R_{YP}]}, \quad (19a)$$

$$\omega_p = \frac{1}{C[R_1(1+\alpha_{o1})+R_{YP}]}. \quad (19b)$$

Equations (19a) and (19b) clearly show that both zero ω_z and pole ω_p frequencies are again partly affected by the

parasitics and non-idealities of the UVC. However, they can be minimized by making the α_{oj} and δ_{oj} (for $j = 1,2$) very close to unity and/or choosing $2R_2 \gg R_{YN}$ and $R_{YP} \approx R_{YN}$, and/or choosing $R_1 \gg R_{YP}$.

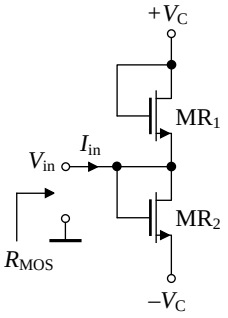

Fig. 3. Grounded resistor using two NMOS and two symmetrical power supplies [11], [41].

Both circuits have the advantage of employing grounded resistors, which enables to use a simple realization of the electronic resistor based on two NMOS transistors as it is shown in Fig. 3 [11], [41] and its resistance can be calculated as follows:

$$R_{MOS} = \frac{V_{in}}{I_{in}} = \frac{L}{2\mu C_{OX} W (V_C - V_T)}. \tag{20}$$

Here, μ is carrier mobility, C_{OX} is the gate capacitance per unit area, V_T is threshold voltage, and W and L are the channel width and length, respectively.

4. Simulations and Measurements

To verify the theoretical study, the behavior of both proposed VM all-pass filters has been verified by SPICE simulations. The CMOS implementation of the UVC bases on the input stage of the current differencing transconductance amplifier (CDTA) [40] and voltage buffer/inverting voltage buffer of the ICDBA [21], and is shown in Fig. 4 [14]. The input stage is formed by transistors M1–M24, transistors M25–M31 form the voltage buffer, and the inverting voltage buffer consists of transistors M32–M40. For this purpose the transistors are modeled by the TSMC 0.35 μm level 3 CMOS process parameters (Tab. 2). The transistor dimensions are listed in Tab. 3. The DC power supply voltages are equal to $\pm$2.5 V and bias currents I_O are 100 μA.

The transistor aspect ratios of the MOSFET-based electronic resistors in Fig. 3 are chosen as $W = 2$ μm and $L = 2$ μm. For the control voltages $V_C = \{0.89;\ 1.04;\ 1.25\}$ V, the values of R_{MOS} are $\{16;\ 10;\ 6.8\}$ kΩ, respectively. The value of the capacitors C for the first and second circuit in Fig. 2 have been chosen as 20 pF and 10 pF, respectively. The ideal and simulated gain and phase responses and electronical tunability of both circuits are shown in Fig. 5. The pole frequency of the proposed filters is varied via control voltages of V_C. In this case the pole frequency of both filters is $f_0 \cong \{0.5;\ 0.795;\ 1.17\}$ MHz, respectively. From the simulation results it can be seen that there is a roll-off in the phase responses for both circuits on both outputs at high-frequency region. However, the phase characteristics of both proposed filters are in close proximity to the ideal ones. The drop off in the gain is mainly caused by the non-ideal voltage transfers δ_{o1} and δ_{o2} that are 0.888 and 0.884, respectively. Total harmonic distortion (THD) variations with respect to amplitudes of the applied sinusoidal input voltages at 795 kHz are shown in Fig. 6. An input with the amplitude of 180 mV yields THD values of 3.67 % and 3.71 % for the first and second outputs of the first proposed filter in Fig. 2(a), respectively. For the second proposed filter in Fig. 2(b) with respect to same amplitude of 180 mV input volatge, the THD values are 2.68 % and 2.70 % for the first and second outputs, respectively. The simulated filters power dissipation is 5.84 mW.

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.MODEL CMOSN NMOS (LEVEL = 3 TOX = 7.9E–9
+ NSUB = 1E17 GAMMA = 0.5827871 PHI = 0.7
+ VTO = 0.5445549 DELTA = 0 UO = 436.256147
+ ETA = 0 THETA = 0.1749684
+ KP = 2.055786E–4 VMAX = 8.309444E4
+ KAPPA = 0.2574081 RSH = 0.0559398 NFS = 1E12
+ TPG = 1 XJ = 3E–7 LD = 3.162278E–11
+ WD = 7.046724E–8 CGDO = 2.82E–10
+ CGSO = 2.82E–10 CGBO = 1E–10
+ CJ = 1E–3 PB = 0.9758533 MJ = 0.3448504
+ CJSW = 3.777852E–10 MJSW = 0.3508721)
.MODEL CMOSP PMOS (LEVEL = 3 TOX = 7.9E–9
+ NSUB = 1E17 GAMMA = 0.4083894 PHI = 0.7
+ VTO = –0.7140674 DELTA = 0 UO = 212.2319801
+ ETA = 9.999762E–4 THETA = 0.2020774
+ KP = 6.733755E–5 VMAX = 1.181551E5
+ KAPPA = 1.5 RSH = 30.0712458 NFS = 1E12
+ TPG = –1 XJ = 2E–7 LD = 5.000001E–13
+ WD = 1.249872E–7 CGDO = 3.09E–10
+ CGSO = 3.09E–10 CGBO = 1E–10
+ CJ = 1.419508E–3 PB = 0.8152753 MJ = 0.5
+ CJSW = 4.813504E–10 MJSW = 0.5)
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Tab. 2. 0.35 μm TSMC CMOS parameters.

PMOS transistors	W(μm)/L(μm)
M3–M8, M10, M15–M18, M20	28.0/0.7
M25, M26, M34, M35	4.0/0.5
M27, M36	10.0/0.5
M32, M33	2.1/1.0
NMOS transistors	**W(μm)/L(μm)**
M1, M2, M9, M11–M14, M19, M21–M24	14.0/0.7
M28, M29, M37, M38	0.8/0.5
M30, M31, M39, M40	10/0.5

Tab. 3. Transistor dimensions of the UVC.

Using the INOISE and ONOISE statements, the input and output noise behavior for both responses of both filters with respect to frequency have also been simulated, as it is shown in Fig. 7. For the first proposed filter, the equivalent input/output noises for both responses at operating frequency ($f_0 \cong 795$ kHz) are found as 80.1/47.6 nV/$\sqrt{\text{Hz}}$ and 92.3/51.9 nV/$\sqrt{\text{Hz}}$, respectively. For the second proposed filter, the equivalent input/output noises for both responses at same operating frequency are found as 80.9/51.1 nV/$\sqrt{\text{Hz}}$ and 83.9/51.9 nV/$\sqrt{\text{Hz}}$, respectively.

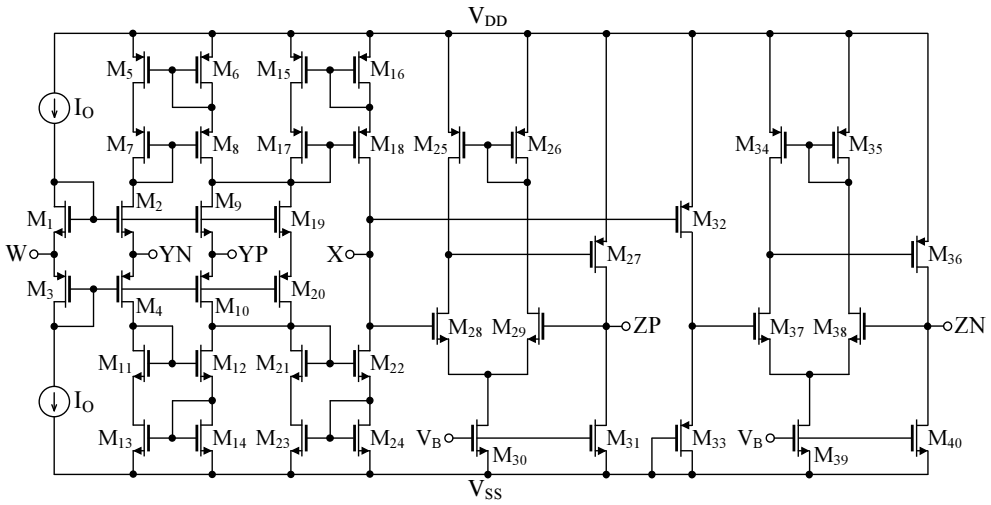


Fig. 4. CMOS implementation of the UVC [14].

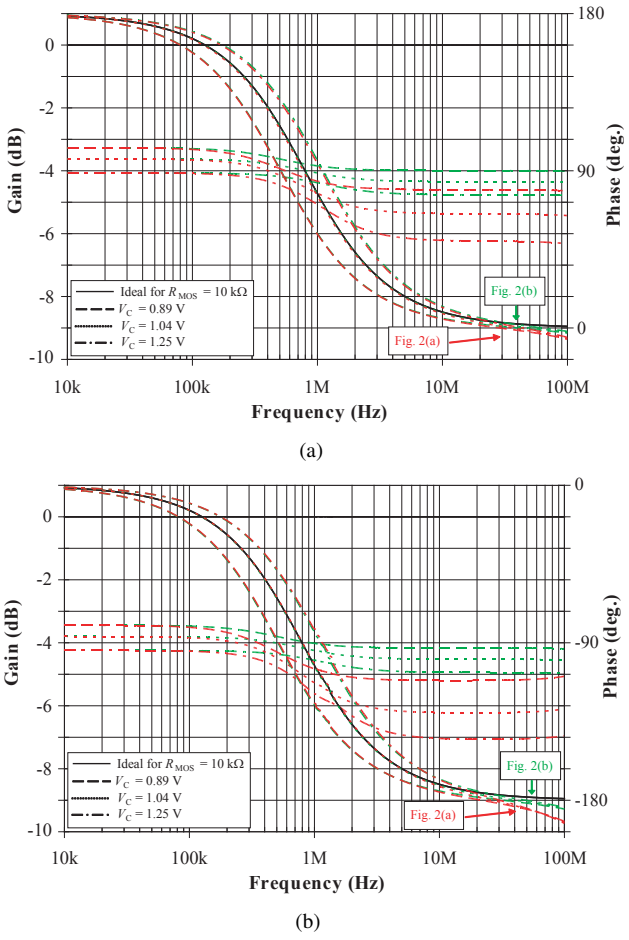


Fig. 5. Ideal (black solid) and simulated gain and phase characteristics of the proposed: (a) inverting and (b) non-inverting VM first-order all-pass filters.

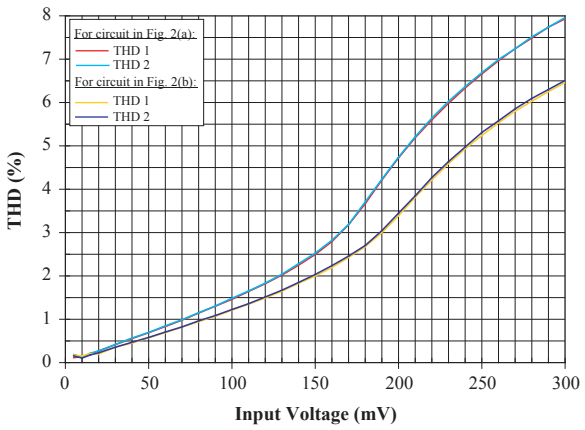


Fig. 6. THD variation for both responses of both proposed all-pass filters against applied input voltage.

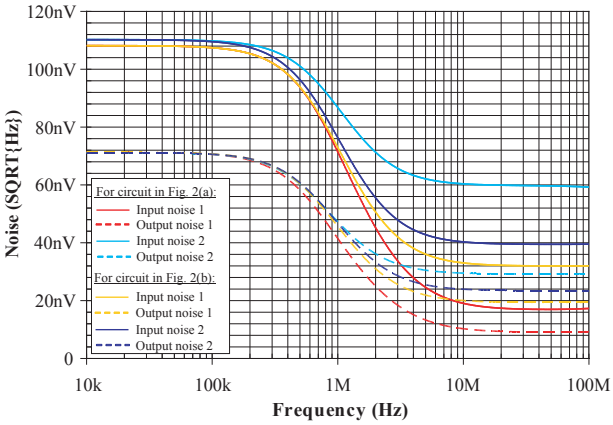
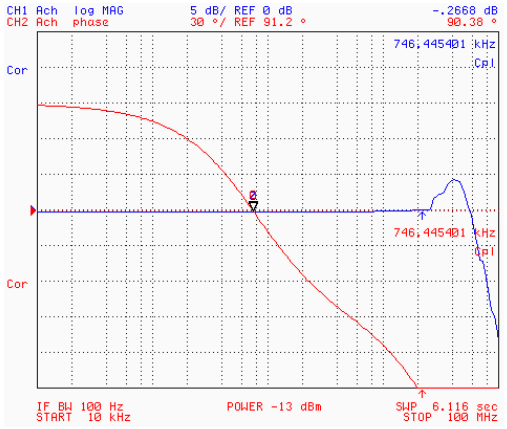
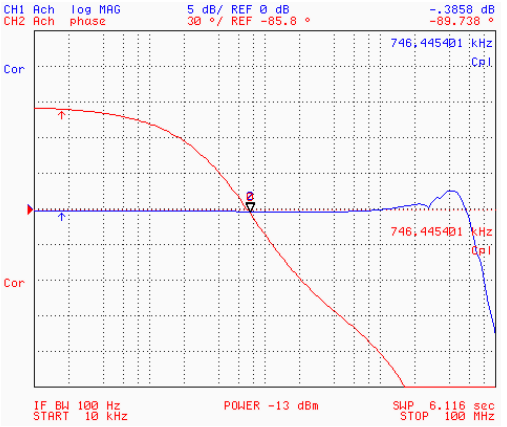


Fig. 7. Input and output noise variations for both responses of both circuits versus frequency.



(a)



(b)

Fig. 8. Measured gain and phase characteristics of the second proposed inverting and non-inverting VM first-order all-pass filter in Fig. 2(b): (a) $T_1(s)$, (b) $T_2(s)$.

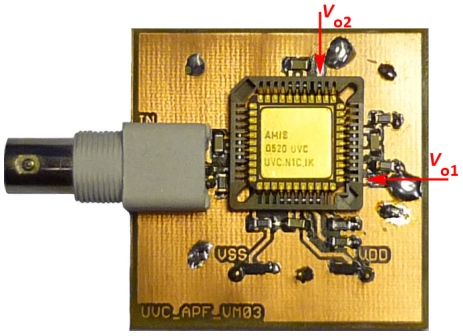


Fig. 9. The prototype PCB of the filter from Fig. 2(b).

From the simulation results presented above it is evident that the second proposed filter in Fig. 2(b) shows better performance such as lower roll-off in the phase responses at high-frequency region and better THD. Therefore, in order to confirm these simulation results, the behavior of the second proposed UVC-based all-pass filter from Fig. 2(b) has also been verified by experimental measurements using network analyzer Agilent 4395A. In the measurements the UVC-N1C 0520 [26], [35] integrated circuit has been used whose power dissipation is 95.7 mW. For the pole frequency of 795 kHz the capacitor and resistors have been chosen as follows: C = 100 pF and $R_1 = R_2$ = 1 kΩ. In this case a 90° phase shift is at $f_0 \cong$ 746.4 kHz and the results are shown in Fig. 8. The lower value of the pole frequency is caused by the behavior of the real UVC [26], [35], however, the real behavior of the filter is still very satisfactory. The developed PCB (printed circuit board) is shown in Fig. 9.

5. Conclusion

In this paper, two novel voltage-mode first-order all-pass filters with high-input and low-output impedances are presented. The high-input and low-output impedances are desired for easy cascading in VM operations. Due to unique internal structure of the active element used, both proposed filters provide both of inverting and non-inverting outputs at the same configuration. Even if the presented circuits require resistor matching condition, it should be noted that in the current IC technology it is possible to match resistors with much better precision than 0.1 % [42]. The use of grounded resistors in both circuits is very advantagous. It enables to use a simple realization of MOSFET-based electronic resistors, which allows easy tuning of pole frequency in both solutions. The proposed filters provide a wide range of frequency response, which is confirmed by SPICE simulations. Moreover, using the fabricated UVC-N1C 0520 prototype, the behavior of the second proposed filter is also experimentally measured.

Acknowledgements

The research described in the paper was supported by the Czech Ministry of Education under research program MSM 0021630513 and Czech Science Foundation projects under No. P102/11/P489 and P102/09/1681. Authors also wish to thank the reviewers for their useful and constructive comments.

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About Authors...

Norbert HERENCSAR received the M.Sc. and Ph.D. degrees in Electronics & Communication and Teleinformatics from Brno University of Technology, Czech Republic, in 2006 and 2010, respectively. Currently, he is an assistant professor at the Department of Telecommunications, Faculty of Electrical Engineering and Communication, Brno University of Technology, Brno, Czech Republic. From September 2009 through February 2010 he was an Erasmus Exchange Student with the Department of Electrical and Electronic Engineering, Bogazici University, Istanbul, Turkey. His research interests include analog filters, current-mode circuits, tunable frequency filter design methods, and oscillators. He is an author or co-author of about 55 research articles published in international journals or conference proceedings. Dr. Herencsar is a member of the IAENG, ACEEE, and IACSIT.

Jaroslav KOTON received the M.Sc. an Ph.D. degree in electrical engineering from the Brno University of Technology, Czech Republic, in 2006 and 2009, respectively. He is currently an assistant professor at the Department of Telecommunications of the Faculty of Electrical Engineering and Communication of Brno University of Technology, Czech Republic. His current research is focused on linear- and non-linear circuit designing methods with current or voltage conveyors, and current active elements. He is an author or co-author of about 65 research articles published in international journals or conference proceedings. Dr. Koton is a Member of IEEE and IACSIT.

Jan JERABEK received the B.Sc. degree in Electrical Engineering in 2005 from the Brno University of Technology, Czech Republic, and the M.Sc. in 2007, from the same university. Currently he studies for the Ph.D. degree at the Department of Telecommunications. His research interests are focused on circuit applications of modern active elements such as current operational amplifiers and multiple-output current followers.

Kamil VRBA received the Ph.D. degree in Electrical Engineering in 1976, and the Prof. degree in 1997, both from the Technical University of Brno. Since 1990 he has been Head of the Department of Telecommunications, Faculty of Electrical Engineering and Computer Science, Brno University of Technology, Brno, Czech Republic. His research work is concentrated on problems concerned with accuracy of analog circuits and mutual conversion of analog and digital signals. In cooperation with AMI Semiconductor Czech, Ltd. (now ON Semiconductor Czech Republic, Ltd.) he has developed a number of novel active function blocks for analog signal processing such as universal current conveyor (UCC), universal voltage conveyor (UVC), programmable current amplifier (PCA), digitally adjustable current amplifier (DACA), and others. He is an author or co-author of more than 650 research articles published in international journals or conference proceedings. Professor Vrba is a member of IEEE and IEICE.

Oguzhan CICEKOGLU received the B.Sc. and M.Sc. degrees from Bogazici University and the PhD. degree from Istanbul Technical University all in Electrical and Electronics Engineering in 1985, 1988 and 1996 respectively. He served as lecturer at the School of Advanced Vocational Studies Electronics Prog. of Bogazici University where he held various administrative positions between 1993 and 1999. He has also given lectures at the Turkish Air Force Academy. He was with the Biomedical Engineering Institute of the Bogazici University between 1999 and 2001. Then he joined the Electrical and Electronics Engineering Department of the same University where he became a professor. Between 2007 and 2010 he served as the Dean of Engineering at Corlu Engineering Faculty of Namik Kemal University, Turkey.

Oguzhan Cicekoglu served in organizing and technical committees of many national and international conferences. He was the guest co-editor of two previous Special Issues of the Analog Integrated Circuits and Signal Processing Journal. One of the publications he co-authored in IEEE Transactions on Circuits and Sytems II-Analog and Digital Signal Processing is among the top cited papers listed in IEEE Circuits and Systems Society web page. He received the Research Excellence Award of Bogazici University Foundation in 2004. He served as the co-chair of Amplifiers and Comparators track in 50th IEEE Midwest-Newcas Joint Conference which is held in Montreal-Canada as a track chair in the 52th IEEE Midwest Symposium held in Cancun-Mexico. His current research interests include analog circuits, active filters, analog signal processing applications and current-mode circuits. He is the author or co-author of about 150 papers published in scientific journals or conference proceedings and conducts review in numerous journals including Analog Integrated Circuits and Signal Processing, IEEE CAS-I, IEEE CAS-II, International Journal of Electronics, International Journal of Circuit Theory and Applications, IEE Proceedings Pt.G, ETRI Journal and several others.

Oguzhan Cicekoglu is a member of the IEEE and is currently the associate editor of International Journal of Electronics.