TOPOLOGY AND BREAKING PROCESS OF HYBRID DC CIRCUIT BREAKER

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Abstract: This study is focused on a general function of hybrid direct current circuit breakers. The one of topics is design topology of these circuit breakers with all necessary branches. Mainly, the study deal with their principles of interruption of fault direct current. The description of issue is in general and then for the specific interesting proposals. The main purpose of these protections is continuous reducing the fault current to the current-zero outside the mechanical breaker contacts which conduct solely the nominal current.

Keywords: Hybrid DC circuit breaker, interruption, fault direct current, proposals

1 INTRODUCTION

The products of electrical engineering are constantly evolved. Many developments and explorations are carried out for reaching the phenomenal attributes and reliable controlling. Therefore, the protections of electrical circuits must be competitive, too and have a front view.

The circuit breakers (CBs) of high voltage direct current grid (HVDC) have been developed continuously and even increasingly in the recent years. The main purpose is to make proposals to reduce or eliminate an electric arc which occurs on the mechanical contacts during short-circuit current interruption. Although existing mechanical circuit breakers (MCBs) offer low conduction loss with negligible resistance, long breaking time and arc extinguishing wear out the mechanical break contacts which makes to decrease their service life. Hybrid circuit breaker (HCB) commutates the fault direct current (DC) to the specific parallel branch consists of power semiconductors. The solid-state switches [2] have a faster breaking time and are controlled by system with high reliability. However, the main limiting factors are on-state resistance and heating. Thereby, it should not utilise for normal conditions in the HCB, solely for break and reclose process. Thus, the hybrid DC circuit breaker increases the fault current interruption capability.

2 HYBRID DC CIRCUIT BREAKER

2.1 STRUCTURE OF CIRCUIT

The circuit topology of hybrid direct current circuit breaker (HCB) often consists of three parallel connected parts. A conductive branch, the main breaker branch of power semiconductors and absorption branch with snubber components.

The conductive branch consists of an ultra-fast disconnector (UFD) to conduct the load current during normal process. The UFD is often combined with a load commutation IGBT switch (LCS) to help the commutation of fault current. In the main breaker branch, power thyristors are very often used for their high current breaking capability and low cost [1], and IGBTs for a fast and reliable full control. The absorption part is employed to next commutate energy and reduce the fault current to a current zero. The rest of accumulated excess energy is shifted to a MOV (metal oxide varistor).

2.2 GENERAL BREAK PROCESS

1. Commutation from the conductive branch to the main breaker branch. The power semiconductors are turned on. The fault current starts to flow in this branch and di/dt significantly decreases across the UFD.

2. Current zero in the conduction branch. The UFD starts to break without the electric arc and a dielectric strength is sequentially increased through the mechanical contacts.

3. Commutation to the absorption branch after the UFD is fully opened. The solid-state switches are usually turned off. Subsequently, all energy commutates to the absorption part and the snubber capacitors are charged.

4. Commutation from the snubber capacitors to the MOV or other absorption components. For instance, the capacitor is charged to the voltage value of MOV and all excess energy transfers outside the HCB. In this article, the reclose and rebreak process after interruption is not presented.

3 HYBRID DC CIRCUIT BREAKER BASED ON SERIES CONNECTION OF THYRISTORS AND IGBT HALF-BRIDGE SUBMODULES

This proposal [1] has all branches described in Chapter 2. The UFD is combined with the LCS for its effectiveness and simplicity. A main breaker has the branch of series connected thyristors and IGBT half bridge submodules with full-controlled lower Q_L and upper arm Q_U, as shown in Fig. 1. The thyristors reduce the number of IGBTs which makes to lower overall costs. Besides, the thyristors withstand the major part of turn-off surge voltage instead of IGBTs. These solid-state switches are series connected to protect themselves against a high DC voltage and surge voltage. The snubber circuit consist of snubber capacitor and parallel connected diodes and resistor. The resistor is used for following reclosing. MOV absorb the excess energy.

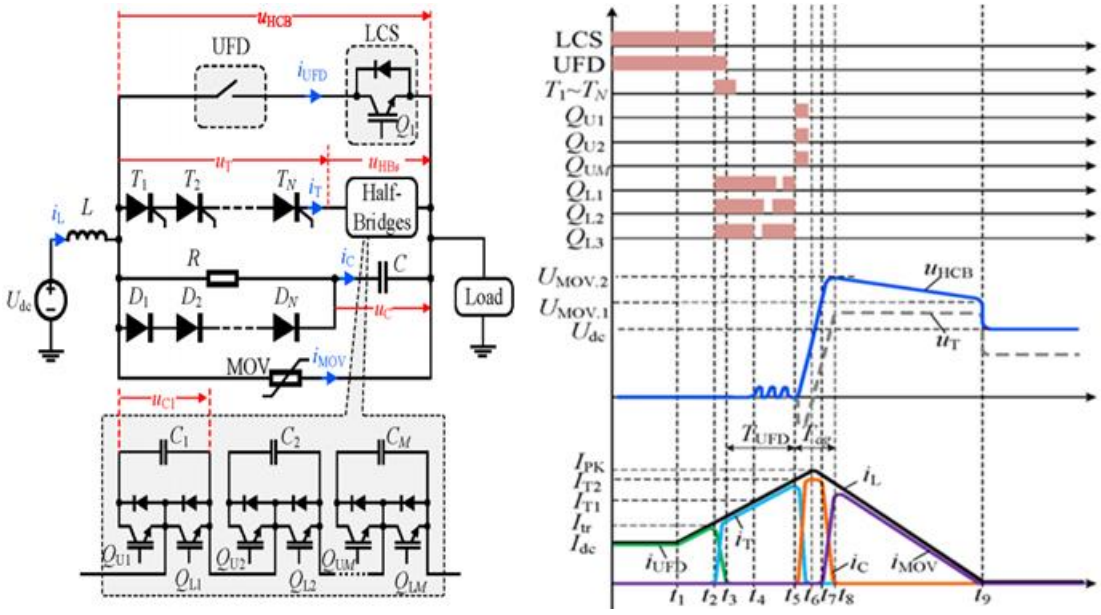

Figure 1: Circuit topology and waveform during break process [1].

The break process of the proposed HCD includes 8 stages, as shown in Fig. 1. **At time t1**, the fault occurs and load current i_L starts to rise linearly through the conductive branch, as shown in Fig. 1. **At time t2** starts the commutation from the LCS to the thyristors. First, turn-on drive signal will be sent to the thyristors (T_1–T_N) and the lower arm IGBTs (Q_{L1}–Q_{LM}) in half-bridges. Then, the LCS will be turn off and afterwards the load current i_T will be transfer to the thyristor branch. **At time t3**, the UFD starts to break without the arc and has a low breaking speed. So, the dielectric strength across it will be built slowly in several milliseconds. After the time delay, **at time t4** are charged

the submodule capacitors of IGBT half bridges for thyristors break. The submodule capacitors will be gradually charged to obtain the voltage value of one submodule capacitor (U_m) and to maintain relatively low du/dt across the mechanical contacts. First, the lower IGBT QLM is turn off while remain QL are conducted. Same way will be for the rest of submodule capacitors until the charge process is complete. **At time t5** is commutation to the snubber circuit. The UFD is full opened and the Q_L are turned off. After the short dead time, the Q_U will be turned on. The generated reverse voltage from submodule capacitors will be applied to force the interruption of thyristors and will need to last long enough to fully turn off these thyristors. **At time t6**, the thyristors and then the Q_U are completely turn off. The snubber capacitor is sequentially charged by the fault current rapidly and its capacity C should be high to limit the maximum du/dt of proposed thyristors. **At time t7**, after the voltage across C reaches the break voltage of MOV ($U_{MOV,1}$), the load fault current will transfer to this MOV. **At time t8**, the fault current starts to decrease at the peak MOV voltage ($U_{MOV,2}$) and **at t9**, it reaches the current zero. This peak MOV voltage is commonly 1,2-2 times of UDC. The bidirectional system is proposed but it is not presented in this article. [1]

4 CASCADED COMMUTATION CIRCUIT OF HYBRID DC CIRCUIT BREAKER

This proposal [2] is different, especially, without the snubber circuit. The conduction branch is without the LCS to reduce the power semiconductors. The commutation circuit is the main branch of HCB and consists of the series connected capacitors (C_C) which are associated with IGBT solid state switch (T_n) in each cascaded voltage stage. The last part of circuit is commutation coil L_C to produce the resonant counter current. The MOV is used in the absorption stage. Its clamping voltage ($U_{MOV,2}$) can be twice the DC source and IGBTs is chosen with respect to this voltage.

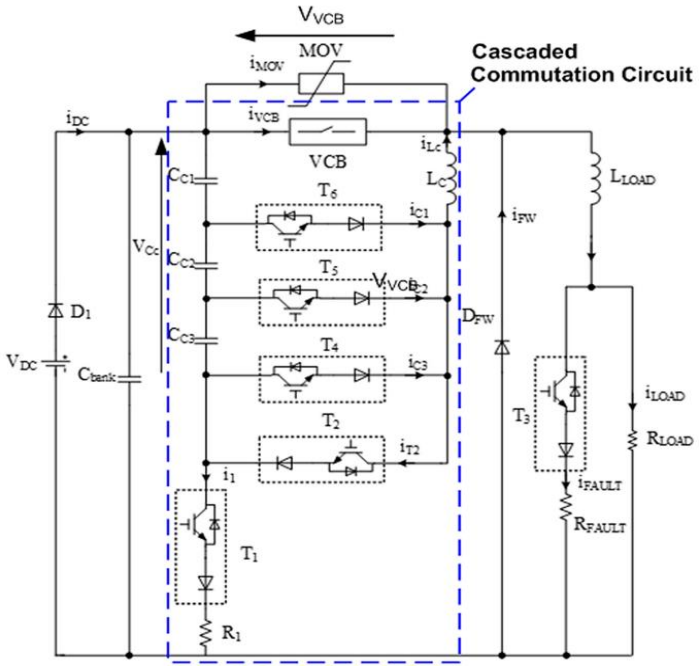

Figure 2: Circuit topology (the UFD is replaced by the vacuum circuit breaker VCB) [2]

When the fault occurs, the T_3 will be turned on and the stored energy of C_{bank} will be transmitted to the R_{FAULT}. Thus, the process of preparation begins. After that, the C_C capacitors start charging the reverse voltage by turning on the IGBT T_2 and turning off the T_1 and this voltage across C_C is equal ($V_{C1} = V_{C2} = V_{C3}$). Then the electrodes start to open with arcing and after the specific distance of contacts, T_4 will be turned on and the resonant counter current ($i_{LC} = i_{C3}$), produced by resonant energy, will be rise and force the fault current though the VCB to decrease ($i_{VCB} = i_{FAULT} - i_{LC}$). Afterwards, the T_5 is closed and the T_4 is opened. The resonant loop is changed ($C_{C1,2} - T_5 - L_C -$ VCB) and i_{LC} is still increased. Then, the T_5 is opened, the T_6 is closed and the fault current reaches

the first current zero. After the current zero, the capacitor voltage is solely V_{C1} to limit the rise rate of transient recovery voltage du/dt through the VCB to maintain the low dielectric strength and to prevent the arcing. The voltage of capacitors C_C is discharged to the voltage zero by sequential switching T_6, T_5 and T_4. When the $C_{C1,2,3}$ is discharged and the VCB is fully opened (T_4 is closed), the all capacitors will be charged by the DC source and the current will flow through R_{FAULT}. After discharging, the i_{VCB} will produce the second current zero, too. The second failure is deemed to interruption failure of breaker. The excess energy will be absorbed in the MOV part, and the fault current will break completely. [2]

The solid-state switches are controlled by sequential time intervals, overlapping for a short duration (1 μs) to ensure commutation current continuity. After interruption, the capacitors need to maintain the DC voltage. Therefore, the required auxiliary circuits (shunt connected resistors) will discharge the capacitor energy when the repair or the maintenance of system is solely necessary. [2]

5 T-TYPE HYBRID DC CIRCUIT BREAKER

This proposal [3] has similar procedures and design as the HCB [1] in Section 2. In Fig. 3 is a bidirectional blocking ability with D1 – D4. The main branch is designed as cascaded full-bridge submodules which consist of the IGBTs and capacitors. The main difference is that these capacitors are already used for charging by the fault current and the subsequent transfer of excess energy to the MOV of individual submodules. When the normal current flows, these capacitors will be precharged by the DC source. During pre-charging, one of IGBTs is closed and the n-1 capacitors are in the process. After that, the sum of n capacitors voltage is higher than the nominal DC voltage. Therefore, this prevent the main branch from connection with the system during normal process as the diode D1 or D2 will stop to conduct.

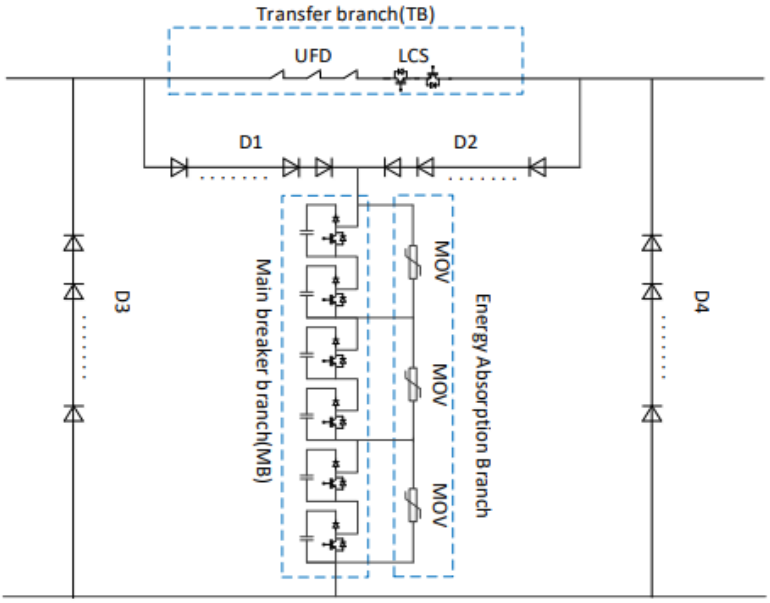

Figure 3: Structure of the T-type with bidirectional system [3]

When the fault current is detected, the IGBTs will be conducted and the LCS will be blocked. In the conduction branch, the current drops to the zero and then the UFD will be full opened under the zero-voltage condition due to pre-charging. It will take no more than 2 ms. Afterwards, the IGBTs can be blocked. The fault current transfer to the capacitors and decrease immediately due to the capacitors has been already pre-charged. After reaching the peak MOV voltage, this current shifts to the absorption branch and the fault is cleared. [3]

6 CONCLUSION

In this article, the interesting topologies of HCB are described and compared. The thyristors and IGBT half-bridge submodule in series [1] in Section 3 have several advancements and advantages. The thyristors withstand the main part of overvoltage and reduce the required number of IGBTs and thus, the overall costs are decreased. The number of thyristors (N) is defined according to the peak voltage of MOV, thyristors and IGBT half-bridge submodule. The submodule capacitors are sequential charged during the UFD breaking. Therefore, the total breaking time is not risen significantly, and the auxiliary supplies are not required. The proposal is verified on high voltage (up to 100 kV) and the equations are simple for verification. The HCB of ABB [4] has a faster breaking time but consists of solely the IGBTs. In Section 4, the commutation circuit [2] produce the resonant counter current to the mechanical contacts. In each commutation branch is solely one IGBT device to reduce the power loss but in high voltage application (>15 kV) will result in more cascaded voltage stages. However, controlling dv/dt through the VCB is increased. The main issue is that the VCB starts to separate the contacts with the electric arc. Therefore, the probability of interruption depends on the first and second current zero through the VCB. The preparation on fault current, charging and discharging capacitors during breaking, and the arc extinguishing prolong the total breaking time, too. The next challenge are difficult resonant equations and controls. The HCB with T-bridge [3] in Section 5 has similar advancements as the HCB in Section 3. The main benefit, the submodule capacitors are pre-charged in normal process and adopt the features of snubber capacitor. Thus, the fault blocking process is shorter compared with the HCB in Section 2 and the peak fault current is lower. The T-bridge structure avoids the dynamic voltage balancing due to the synchronous opening of IGBT. However, the number of submodules and MOV is increased. Thus, the implementation and the calculation will be reflected in overall costs.

The total breaking time of HCB is dependent on the opening mechanical contacts (several ms). The solid-state circuit breaker can achieve the shorter interruption (<1 ms) with lesser components. [2] However, this breaker has significant drawbacks. The physical disconnection of the current path is more reliable with mechanical contacts and the main limiting factors are on-state power losses and heating during normal conditions. The rapid decline di/dt of fault current to produce the induced inductive voltage. Thus, the semiconductors in series must sustain this overvoltage.

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