Saving area and power consumption in 65 nm digital standard cell library

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Abstract—This study aims to investigate multi-bit pulsed latches in comparison with multi-bit flip flops as one of the low-power solutions in 65 nm technology process. Topologies of pulse generators and multi-bit pulsed latches were investigated to find out which can be more suitable. The pulse generator was chosen because of its low power and a small area in comparison with other options. The pulse generator is made of a simple AND logical gate and a double-stacked inverter. The pulsed latch was also chosen because of its low power, small area, and reliability of the circuit. The chosen topology is modified PPCLA. Simulations of the chosen topology had shown that multi-bit flip flops could be replaced with more effective multi-bit pulsed latches.

Keywords—digital standard library, integrated circuits, chip development, low power methods, pulse generator, multi-bit pulsed latch

1. INTRODUCTION

Automotive markets include chips that are developed for automotive-specific application. The problem nowadays is that these chips have high power density which can cause trouble. Some methods can reduce power consumption across the chip. This study will be focused on digital standard cells that are irreplaceable when it comes to integrated circuits. Digital standard cells have significant power consumption in comparison with the whole design, but these digital standard libraries can be enriched with special standard cells that can reduce power consumption to minimum. These special standard cells are also known as low power or ultra-low power solution [2]. One of the low power techniques is the multi-bit pulsed latch which can be used as a replacement for multi-bit flip flops. Multi-bit pulsed latches in comparison with multi-bit flip flops should have smaller area and power consumption [4].

2. DIGITAL STANDARD CELLS IN INTEGRATED CIRCUITS

As it was mentioned before, digital standard cells are an irreplaceable part of automotive-specific applications. Digital standard cells are well-defined cells that can be used in design as a building block [1]. These cells have different views that can represent a different function like schematic, layout, symbol, verilog, liberty, and others [2]. These building blocks are also pre-characterized to save time when they are used in a bigger design. These data of the cells for the whole library; like maximal load, input capacitance, and others are stored in liberty to make more complex simulation faster. Many types of digital standard libraries can be found in the technology; it depends on application or requirements from customers. The performance of the libraries is given by the height of the cells. The digital standard library has all cells with the same height because these cells can be easily connected to power rails and can be easily used with the automatic place and route tool [1]. Digital libraries can be often developed as high-density (HD) or high-speed (HS). High-speed libraries have greater height, larger speed, and bigger power consumption than high-density libraries. The width of the cells is given by the complexity of the cell, but the width of the cell should be minimized to achieve a maximal density of the design. These libraries can be also designed with different models of the transistor that have different threshold voltages [2]. The simplest cell is shown in Figure 1. It represents a simple layout inverter that is composed of two

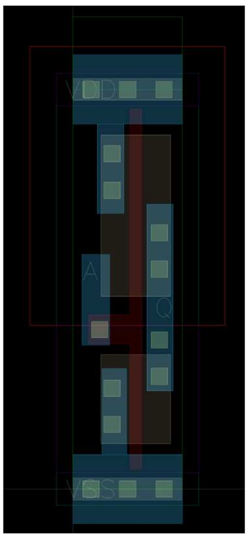

Figure 1: Layout of inverter in 65 nm technology

transistors. The height of these transistors in Figure 1 is not the same because the PMOS transistor is slower than the NMOS transistor with the same height. On the other hand, the PMOS transistor can be used differently because the PMOS transistor is more immune to noise and has smaller leakage than the NMOS transistor. The height ratio of both transistors is given by the technology. These libraries can be composed of many types of common cells. The list of often designed cells is shown in Table 1. These libraries can be also enriched with special digital standard cells that can have better power consumption, area, special purpose, or even performance. Following parts can be considered as digital standard cells: level shifter, power-down cell, isolation cell, state retention flip flop, dual or multi-bit flip flops, dual edge-triggered flip flop, low swing dual edge-triggered flip flop, and a multi-bit pulsed latch. This study is primarily focused on multi-bit pulsed latches [2].

Table 1: List of common cells in the digital standard library

Name of cell	Description of the cell
BUF, INV, AND, OR, NAND, NOR XOR, XNOR	Simple logical functions with multi-inputs and different output strengths
HALF/FULL ADDER	2-bit Half and full adder with different output strengths
MUX / DEMUX	Multiplexor or demultiplexer with different output strength
ECO CELLS	Universal cells can be used in case of need
AOI or OAI	Multi-input and/or or or/and logical combination
FLIP FLOPS or SCAN FLIP FLOPS	Flip flops with reset/set and different output strength, Scan flip flop can be used as a shifter
LATCHES	Flip flop controlled with level
FILLCAP / FILLER	Decoupling capacitance/cell can connect power rails
DELAYS	Used for compensation of STA violations

3. MULTI-BIT PULSED LATCH AS A SPECIAL DIGITAL STANDARD CELL

Multi-bit pulsed latches are a new solution for low-power libraries. The pulsed latch is a simple latch that can be driven by a short pulse instead of a standard square clock source. Multi-bit means that there is more than one latch that can be driven by a short pulse. The function of the pulsed latch is the same as the flip flop only if the latch is driven by a short pulse generated from a standard square clock signal. To put it simply, the multi-bit pulsed latch is composed of two parts; the pulsed latch and a pulse generator which generates a short pulse from a standard square clock source [3].

Table 2: Types of negating delay with AND logical gate

Type of delay	Power [nW]	Predicted width of cell [nm]
Inverter	834.0	973
Stacked inverter	848.4	992
Double-stacked inverter	826.7	930

The pulse generator can be designed as local or as global. A local generator describes a generator that is designed inside of the multi-bit pulsed latch cell. The global generator is designed separately from the multi-bit pulsed latch cell. The local generator is more popular because the load of the generator is known, and the generator is custom designed. That means the parasitic routing is limited to the minimum [3]. The pulse generator is a simple logical combination and a negating delay block which can make enough wide pulse for the pulsed latch. The width of the pulse is dependent on negating the delay block. The size of the cell should be small and that is the reason why only the simplest standard logical gates like AND, OR and XOR can be considered. It can be used as a logical combination as it was mentioned before. The main difference between these logical gates is that the pulse is generated on different events. AND gate makes the pulse on the rising edge, OR gate makes the pulse on the falling edge and XOR makes the pulse on both edges. The output should be changed on the rising edge. That is why the AND gate was chosen. The delay part can be also done differently. The simplest possible way how to make a negating delay block is to make an inverter with a bigger length. However, it can be replaced with a more saving solution like a stacked inverter or a double-stacked inverter. All simulated inverting delay parts are shown in Table 2. The best solution for the delay part is a double-stacked inverter because of the smallest total power and the smallest predicted width of the cell.

Choosing the pulsed latch is more complicated than choosing a pulse generator because the pulsed latch must have scan input. It means that a multi-bit pulsed latch can be connected as a shifter. Standardly, inputs and outputs are independent and are connected separately. The switch is made by the multiplexer and in this case, pass gate multiplexer is used to minimize the number of transistors. The multi-bit pulsed latch is limited by the minimal width of the pulse which can be used for a maximal functional circuit. However, the main problem of multi-bit pulsed latch in scan mode is that the width of the pulse is limited even from the top. If the pulse is too wide, the first latch will be working well but the second latch in the chain will be working on the same pulse. That means the multi-bit pulsed latch will shift the data to the second latch and not only to the first latch. The point to the next latch is often taken from the internal node which represents output data of the first latch. In all circuits that were simulated, there is no internal node that can reach maximal functionality because the propagation delay between the pulse and path to the next latch stage is too short. It means that the simulated circuit can work only in fast or slow corner. There are two solutions to this problem. The first one is an additional delay between the internal node and the input of the next latch. This kind of solution would have a bigger power consumption and bigger size of the area which makes this solution unacceptable. The second solution is to take the point for the next latch from the output stage where the Q is. The path will be long enough to prevent the stability of the circuit in all corners, both fast and slow. Those simulated multi-bit latches are shown in Table 3 and their schematic in Figure 2. The chosen topology PPCLA modified has a great minimal usable width of the pulse and clock to output propagation delay. One of the topologies is working in both cross corners. The total power and number of used transistors are also low. The modified version is different in feedback where on Q_b another inverter was added and from this point a pass gate is taken to the first inverter. When the topology of the pulsed latch is chosen, multi-bit versions of the chosen circuit can be simulated. These multi-bit pulsed latches are typically made in 2, 4, and 8 bits.

Table 3: Types of usable pulsed latches in the digital standard library

Name of pulsed latch	Power [nW]	No. of transistors [-]	Minimal width of pulse [ps]	CLK to Q propagation delay [ps]
PTLA	493.8	10	94	157.3
SSALA	371.6	11	53.5	120.4
SSA2LA	371.7	12	55	113.9
CPNLA	550.5	13	56.5	139.5
PPCLA	313.2	12	41	91.4
PPCLA MOD.	320.7	12	35	112.2

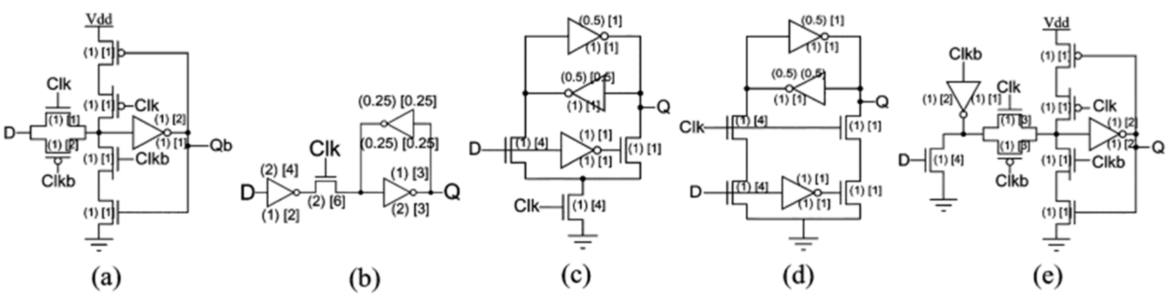

Figure 2: PPCLA (a), PTLA (b), SSALA (c), SSA2LA (d), CPNLA (e) [4]

4. COMPARATION OF THE MULTI-BIT PULSED LATCH AND MULTI-BIT FLIP FLOP IN A SIMPLE SIMULATION

This chapter is comparing designed multi-bit pulsed latches with multi-bit flip flops because it is the first step before stating that multi-bit pulsed latches can be used as a replacement multi-bit flip flop. The comparison is based on power consumption and the predicted area which are the most important specifications of digital standard libraries. The compared circuits are shown in Table 4. One of the advantages of the multi-bit pulsed latch is that with an increasing number of bits, the savings are more significant in comparison with multi-bit flip flops. The generator is becoming less significant in comparison with the whole circuit. A 2-bit version of the pulsed latch has power consumption slightly higher than in the case of the 2-bit flip flop. The difference is about 7.8 % (normal) and 9.4 % (scan). The area can compensate for this difference because it is about 20 % smaller. The cell can be used as an advantage if the designer needs to save only area because it is still useful if the designer needs to save area regardless of power consumption. In the following multi-bit versions of pulsed latches, the power consumption is even better than in the case of multi-bit flip flops. In the 4-bit version, the power savings are about -6.3 % (normal) and -4.3 % (scan). The area is about -31.7 % better. In 8-bit version the power savings are about -14.6 % (normal) and -13.4 % (scan). The area is saved about -38.3 %.

Table 4: Comparison of multi-bit pulsed latches and multi-bit flip flops

	Mode	**Pulsed latch**			**Flip flop**		
Number of bits	**-**	2	4	8	2	4	8
Power consumption [µW]	**Normal**	2.512	4.272	7.689	2.330	4.561	9.003
	Scan	2.535	4.342	7.721	2.318	4.538	8.912
Predicted area [µm^2]	**-**	24.96	42.64	76.96	31.20	62.40	124.80

5. CONCLUSION

The designed multi-bit pulsed latches in 65 nm technology show that the power consumption and the predicted area are better than in the case of multi-bit flip flops. The worst designed cell is a 2-bit pulsed latch which has a slightly bigger power consumption than the 2-bit flip flop. However, this designed cell can still be used because the predicted area is about 20 % smaller than a 2-bit flip flop. The designer can use this cell to reduce area regardless of power consumption. Other designed multi-bit pulsed latches like 4-bit and 8-bit versions have smaller power consumption and smaller area which implies that multi-bit pulsed latches can be used as saving digital standard cells in comparison with multi-bit flip flops. The following step is to layout these designed cells and compare them to have accurate results.

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