BRNO UNIVERSITY OF TECHNOLOGY
FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION

Opponent Review of Doctoral Dissertation

Applicant: Ing. Roman Mego

Title of Dissertation: Parallelism in Digital Signal Processing

Opponent: Ing. Jitka Vágnerová, PhD.

Opponent's Department: Industry

In accordance with the Study and Examination Rules of BUT, in his/her review the opponent will mainly comment on:
a) the topicality of the dissertation,
b) whether the dissertation achieved its given objective,
c) the problem-solving procedure and the results of the dissertation along with the concrete contribution of the doctoral student,
d) the significance for practical application or the progress in the field,
e) formal and language qualities of the dissertation,
f) whether the dissertation fulfils the conditions of Section 47 (4) of the Act,
g) whether the student proved his/her creative abilities in the given research field and whether the work does or does not comply with the standard requirements placed on the dissertations in the given field. The review is not valid without this conclusion.
It is necessary to add a concise commentary to each of the points below.

Ad a) Topicality of the dissertation

The topic of the dissertation is topical.
Comment: The dissertation compares several approaches of parallelism in VLIW-based processors. The topic expands well-known and predictable statements about data and thread parallelism, algorithm parallelism, and high-level versus low-level programming approaches. The low-level programming is most capable for being researched and optimized, so the author focuses on specific algorithms for this approach in the Instruction Mapping Tool for DSPs section, which describes one of the main dissertation goals. The assumptions about non-relevant or non-efficient approaches are discussed in the State-of-the-Art section and some of them are proofed in depth in subsequent chapters. The author also briefly described some deadlock solutions and focused deeply on the more promising ones. Nowadays, the topic becomes more and more relevant, since the motivation is to define a mechanism for power-efficient and performance optimized algorithm.

Ad b) Objective of the dissertation

The objective of the dissertation was achieved.
Comment: The first objective was based on the assumption that the software development tools for instruction-level parallelism were less effective than the tool for data or task parallelism. This assumption is straightforward, it was proved in the section 3, and it was a starting point for the other, more valuable, objectives. The other objectives are related to the instruction-level parallelism, finding a concept suitable for an effective assignment of the available hardware resources, and the optimization method for their effective mapping. These objective lead to an HDL-like approach which is being optimized to achieve less instruction cycles for selected operation, use the available resources effectively, and achieve shorter processing time and bigger power efficiency.

Ad c) Problem-solving procedure and the results of the dissertation and the concrete contribution of the doctoral student

The problem-solving procedure and the results of the dissertation are average.
Comment: The most valuable contribution section of the thesis is the Instruction Mapping Tool for DSPs. Its Algorithm mapping, Node sorting, and Functional unit allocation sections can be good start for further research. A possibility of the usage of the algorithm on different architectures would is an interesting and challenging topic.
Also mapping bottlenecks and deadlock approaches with clear explanation and empiric proof can be helpful for other authors to prevent struggling with a "no go" solution.

Ad d) Significance for practical application or progress in the field

The significance for practical application or progress in the field is average.
Comment: Commercial/institutional applications and/or further research can reuse and extend primarily the sections presenting the instruction-level parallelism tools, the effective assignment of the available hardware resources, and the optimization method for their effective mapping. The algorithms are defined for integer, fixed-point, and floating-point arithmetic, which enables wide use for further research.
The findings presented in sections 3.2.5 and 4 are straightforward and predictable, so they may deserve a less effort and could be rather part of the State of the Art section.

Ad e) Formal and language qualities of the dissertation

Formal and language qualities of the dissertation are above average.

Comment: The thesis is logically sectioned, readable, and easy to understand.

Ad f) The dissertation fulfils the conditions of Section 47 (4) of the Act

The dissertation fulfils the conditions of Section 47 (4)*) Act No. 111/1998 Sb. Higher Education Act: YES

((4) Studies are duly finished with a doctoral state exam and dissertation defence, which prove the ability and readiness to work independently in the field of research or development, or in theoretical and creative arts. The dissertation must comprise original and published results or results accepted for publication.*

Ad g) Creative abilities of the student in the given research field. Compliance with the standard requirements placed on the dissertations in the given field.

The doctoral student did prove his creative abilities in the given research field and the work does comply with the standard requirements placed on the dissertations in the given field.
Comment: The author demonstrates some creativity in the given research field. The dissertation compares approaches to parallelism in VLIW-based processors and relies heavily on existing knowledge. The exploration of specific algorithms in the Instruction Mapping Tool for DSPs section shows promise. While compliance with standard requirements is generally met, further depth and originality would enhance the research.
The Mapping Tool for DSPs section of the dissertation is the main contribution of the thesis. The author delves into algorithm mapping, node sorting, and functional unit allocation, providing insights into optimizing hardware resource allocation. The findings in these areas serve as a foundation for further research and have the potential to be generalized across different architectures.

Overall evaluation: The dissertation explores different approaches to parallelism in VLIW-based processors. It focuses on data and thread parallelism, algorithm parallelism, and high-level versus low-level programming approaches. The author emphasizes the importance of low-level programming for optimization and investigates specific algorithms in the Instruction Mapping Tool for DSPs section. The objective of the dissertation was achieved.

Opponent's questions:

- Are there any limitations for Instruction Mapping Tool for DSPs when being applied to other architectures than VLIW? Are there any potential complications that might hinder its applicability?
- Wide spread of easily accessible AI emerged as a significant game changer in recent months, after the thesis was submitted. Is there a possibility to leverage AI for assistance in optimizing the algorithm discussed in the Instruction Mapping Tool for DSPs section? What benefits or complications could it bring?

I ☒ recommend ☐ do not recommend the dissertation for the defence.

Date: 09.06.2023

Signature: [redacted]