

GRAPHENE FIELD EFFECT TRANSISTOR PROPERTIES MODULATION VIA MECHANICAL STRAIN INDUCED BY MICRO-CANTILEVER

Jan Brodský

Master Degree Programme (2), FEEC BUT

E-mail: jan.brodsky@ceitec.vutbr.cz

Supervised by: Imrich Gablech

E-mail: imrich.gablech@ceitec.vutbr.cz

Abstract: This work presents a new method, which enables the electrical characterization of graphene monolayer with induced mechanical strain. The device is a combination of two-dimensional field effect transistor (2DFET) and a MEMS cantilever, both of which can be used to alter graphene properties. The first method applies external electric field to the graphene monolayer. The second method is based on mechanical bending of the cantilever by external force, which induces mechanical strain in the characterized layer. By sweeping the gate voltage (V_{GS}) in range from -50 V to $+50$ V and measuring the current between drain and source (I_{DS}) with fixed drain-source voltage (V_{DS}) at 1 V, Dirac point of graphene is found at ≈ 9.3 V of V_{GS} . After bending of the cantilever, the sweep is performed again. The induced strain shifts the position of the Dirac point by ≈ 1.3 V to $V_{GS} = 8$ V. Because the fabrication process is compatible with silicon technology, this method brings new possibilities in graphene strain engineering.

Keywords: graphene, Dirac point, MEMS, FET, cantilever, mechanical strain

1 INTRODUCTION

Graphene is a carbon material with hexagonal structure, ideally a monolayer. It has been under extensive research since its first preparation in 2004. Because of its unique properties, such as exceptional chemical stability, mechanical flexibility and high charge carrier mobility, it is a promising material for nanoelectronics. Graphene is a semiconductor with zero bandgap, valence and conduction band meet at Dirac points. It is possible to tune the bandgap, e. g. by application of external electric field, doping or mechanical strain engineering [1]. Mechanical strain inducing is advantageous, because no absorption of secondary substances is involved (doping) and the process is fully recoverable, leaving no permanent change in the graphene [2].

2 DEVICE DESIGN AND FABRICATION

2.1 DESIGN

Using software tool CNST Nanolithography Toolbox together with Python, parametrized layout was created. The dimensions of the chip were (6×6) mm², it had four sets of cantilevers, with respective lengths of (100, 200, 300 and 400) μm and width of 60 μm . The total number of cantilevers was 64, while each cantilever has its own source and drain electrodes with varying channel length from 1 μm to 50 μm . The width of the graphene was set to 10 μm . Silicon-on-Insulator (SOI) wafer was used as the substrate. The gate electrode was contacted from the top by an opened window in SiO₂ layer. The entire layout is shown in **Figure 1**.

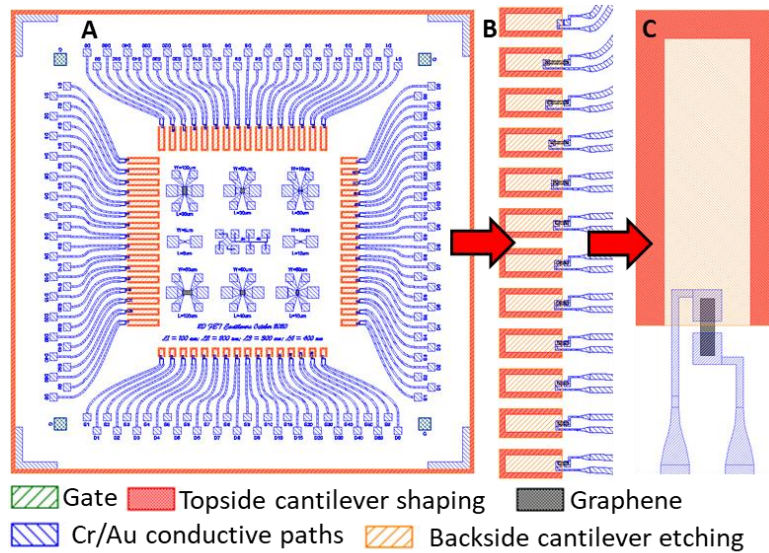


Figure 1: (A) Design of the whole chip with dimensions of (6×6) mm²; (B) Set of cantilevers with electrodes; (C) Detail of a single cantilever.

2.2 FABRICATION

The whole process consisted of 5 lithography steps (**Figure 2**). Thin layer of SiO₂ with thickness of ≈ 90 nm, serving as the gate insulator, was created on the SOI wafer by thermal oxidation process employing O₂.

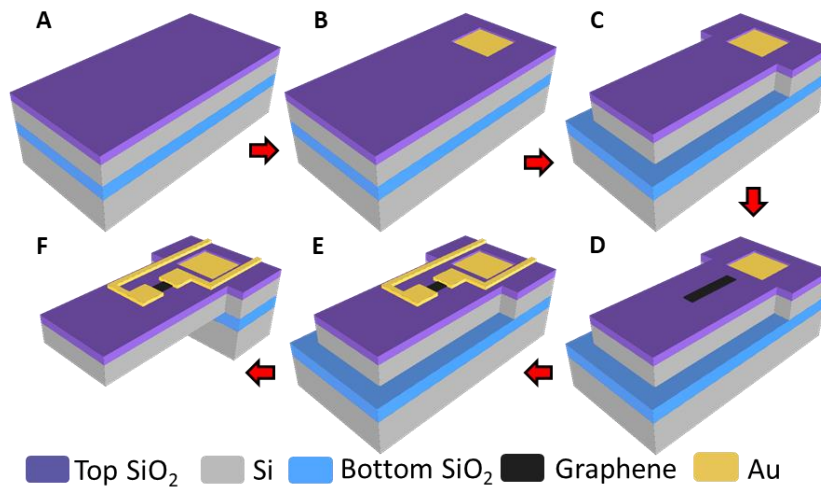


Figure 2: Schematic representation of the fabrication process. (A) SOI substrate; (B) Gate contact; (C) Topside cantilever shaping; (D) Graphene shaping; (E) Electrode lift-off; (F) Shaping cantilevers from the bottom.

During the first lithography, window in the SiO₂ was created by reactive ion etching (RIE), followed by the deposition of Au layer to create the gate contact. In the second step, cantilevers were shaped from the top side by Bosch deep reactive ion etching (DRIE) of the ≈ 3 μ m thick device Si. Afterwards, wafer was properly cleaned in NMP solvent, rinsed in IPA, and finished by O₂ plasma cleaning. Such prepared wafer was used for wet-transfer of CVD grown graphene. In third lithography step, graphene was shaped by covering the pattern in PMMA/AZ 5214 e-beam and photoresist combination and etching in O₂ plasma by RIE. PMMA served only as a protective layer for the graphene. In following step, lift-off of Cr/Au electrodes by e-beam evaporation was realized. In the final step, lithography was performed from the backside of the wafer. Using DRIE once more,

the handle Si ($\approx 500 \mu\text{m}$, bulk silicon) was etched, shaping the cantilevers from the bottom side of the SOI wafer. The final release was also achieved by SiO_2 dry etching. As seen in **Figure 1A** in red, the chips were separated by the DRIE, meaning no dice cutting was necessary. The fabricated chip is shown in Figure 3.

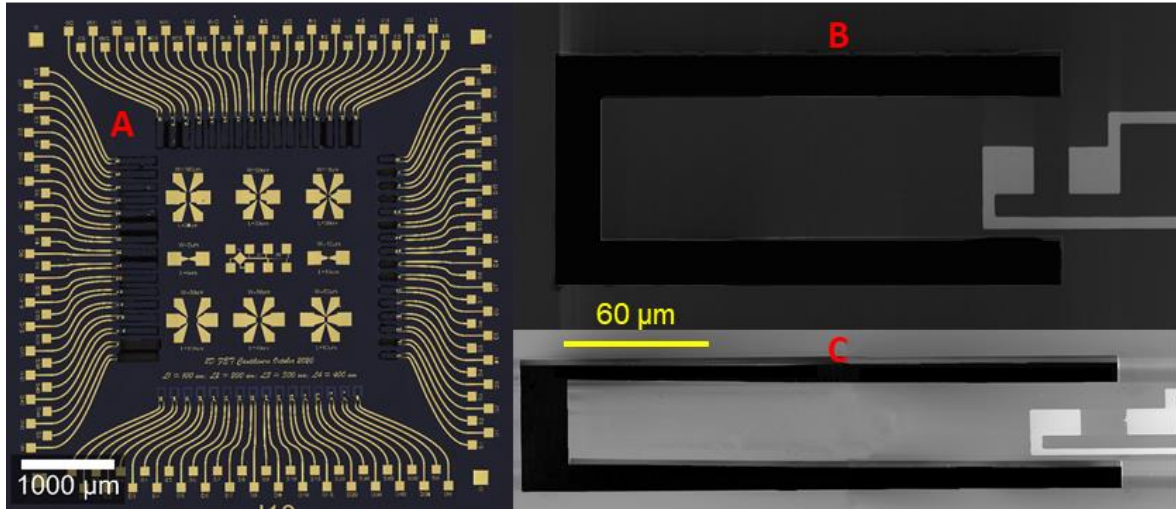


Figure 3: (A) Optical image of the whole chip; (B) SEM image of cantilever from top side; (C) SEM image of cantilever tilted by 55° .

3 EXPERIMENTAL

The individual chips were first cleaned in NMP to remove photoresist residues. Using Raman spectroscopy, it was confirmed that the transferred graphene (Figure 4) is a monolayer [3]. Prior to electrical characterization, the samples were cleaned in acetone and then annealed in vacuum furnace at $\approx 150^\circ\text{C}$ for 36 hours with low temperature ramp of $\approx 3^\circ\text{C}\cdot\text{min}^{-1}$. Dirac point of pristine graphene should be at value of $V_{\text{GS}} \approx 0 \text{ V}$. However, when exposed to air, the graphene becomes p-doped and the Dirac point moves towards higher values of V_{GS} . The cleaning of graphene samples in acetone and annealing partly restores the original position of Dirac point. Using probe station MPS150 and parameter analyzer Keithley 4200A-SCS, V_{GS} was swept in range from -50 V to $+50 \text{ V}$. With fixed voltage V_{DS} , current I_{DS} was measured. The sample was placed in N_2 atmosphere during the measurement, to prevent the doping of the graphene resulting in unwanted shift of the Dirac point. The V_{GS} sweeps were performed three times for each sample, before the bending of the cantilever, with the cantilever bent down and finally with the cantilever returned to its original position.

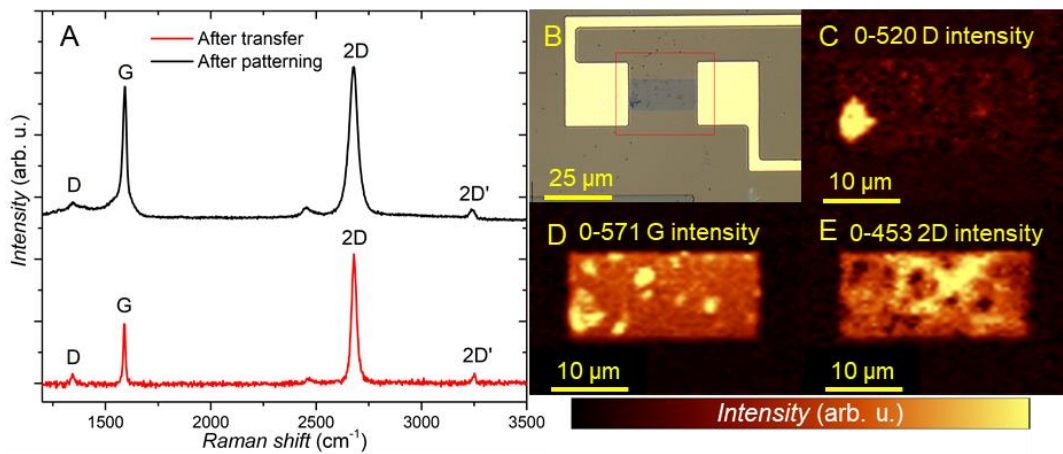


Figure 4: Raman spectra of transferred and patterned graphene: (A) single spectra; (B) optical image of electrode with graphene; Raman map of (C) D peak; (D) G peak; (E) 2D peak.

4 RESULTS

By running the first sweep, Dirac point voltage of slightly p-doped graphene was found at $V_{GS} \approx 9.3$ V (Figure 5). When the cantilever was bent down, the Dirac point voltage shifted by 1.3 V from $V_{GS} \approx 9.3$ V to $V_{GS} \approx 8$ V. For the third sweep, the cantilever was returned to its original position. After the cantilever returned to its initial position, the Dirac point voltage was almost the same as original value with only slight difference of ≈ 0.2 V. The bending process was repeated with other five structures, which show similar behavior with negligible Dirac point voltage differences.

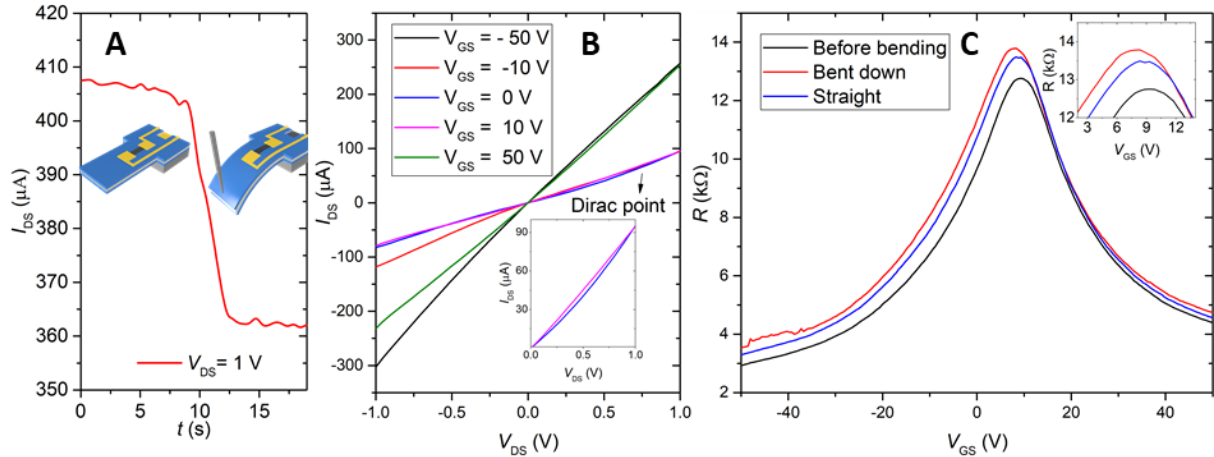


Figure 5: Dirac point voltage shift with induced mechanical strain. (A) Bending of the cantilever in time shows significant decrease of I_{DS} ; (B) I-V characterization with V_{GS} as parameter, hinting the Dirac point voltage (C) Shifting of the Dirac point due to induced mechanical strain by bending.

5 CONCLUSION

In this work, a novel technique for controlling graphene properties through two methods employing electrical field and mechanical strain was introduced. The shift of Dirac point voltage of graphene was achieved by inducing mechanical strain into the monolayer. This opens up new possibilities in graphene strain engineering directly on Si substrates used in integrated circuits. Promising outlook is the possibility to control the stress of deposited films (e. g. ion-beam sputtering using Kaufman source) directly during chip fabrication process which will lead to required strain in graphene after structure release.

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