ACQUISITION SYSTEM FOR ADAPTATION OF DIGITAL PREDISTORTER TO LINEARIZE AMPLIFIERS USING COMPARATOR

Lukáš Jagla

Master Degree Programme (2), FEEC BUT

E-mail: xjagla00@stud.feec.vutbr.cz

Supervised by: Jan Král, Tomáš Götthans

E-mail: jan.kral@vut.cz, gotthans@feec.vutbr.cz

Abstract: This paper presents a design of an acquisition system for adaptation of a digital perdistorter implementing a comparator in the feedback path. The key parts of an acquisition chain are verified by simulations and suitable components are chosen for high-speed performance. Subsequently, a printed circuit board is designed, manufactured and prepared for further testing. Finally, an appropriate firmware is developed to evaluate the proposed hardware and to acquire data for digital predistorter adaptation.

Keywords: Digital predistortion, linearization, power amplifier, comparator, FPGA

1 INTRODUCTION

An essential part of the current wireless systems is a PA (Power Amplifier) enabling to transmit the RF (Radio Frequency) signal of the sufficient power through the environment. The best efficiency of the PA can be achieved when the PA operates as close as possible to its saturation region. Nevertheless, this is causing an undesired output signal distortion which is not acceptable in the current communication systems requiring a linear transmission and working with OFDM (Orthogonal Frequency Division Multiplexing) for instance. There are several methods for extending the linear region of the PA characteristics while achieving satisfactory efficiency, one of them is the DPD (Digital Predistortion) [1]. This work aims at a proposal of an acquisition module for adaptation of digital predistorter using comparator in the baseband. In specific terms, it focuses on hardware and firmware ensuring input data for further design evaluation in terms of deployment in the real DPD system.

2 COMPARATOR IN THE FEEDBACK PATH OF DPD SYSTEM

The proposed DPD system operates with signals in the baseband and enables to use of DSP (Digital Signal Processing) such as in the FPGA (Field Programmable Gate Array) or in a signal processor what makes a great advantage in terms of external components number mitigation. Moreover, it preserves temperature or aging stability [2]. A conventional digital predistorter includes the ADC (Analog-to-Digital Converter) in the feedback path which is the main bottleneck of the system, because in case of wideband signal operation it has to maintain high sample rate and resolution at the same time. These parameters make the ADC hardly available and very power hungry. A possible solution employs the comparator as a 1-bit ADC in the feedback path [3, 4].

3 PROPOSED DPD ARCHITECTURE USING COMPARATOR

The proposed architecture is depicted in Fig. 1 below. The IQ samples are converted to a continuous analog domain at the DPD output and modulated to the carrier frequency at first. Afterwards, the signal goes through the PA to the antenna and its small power is coupled back in the feedback

path. The feedback signal is demodulated and passed to the comparator input. One aspect of the proposed architecture is that the DPD coefficients estimation is based on just one signal component (in this case it is the in-phase component).

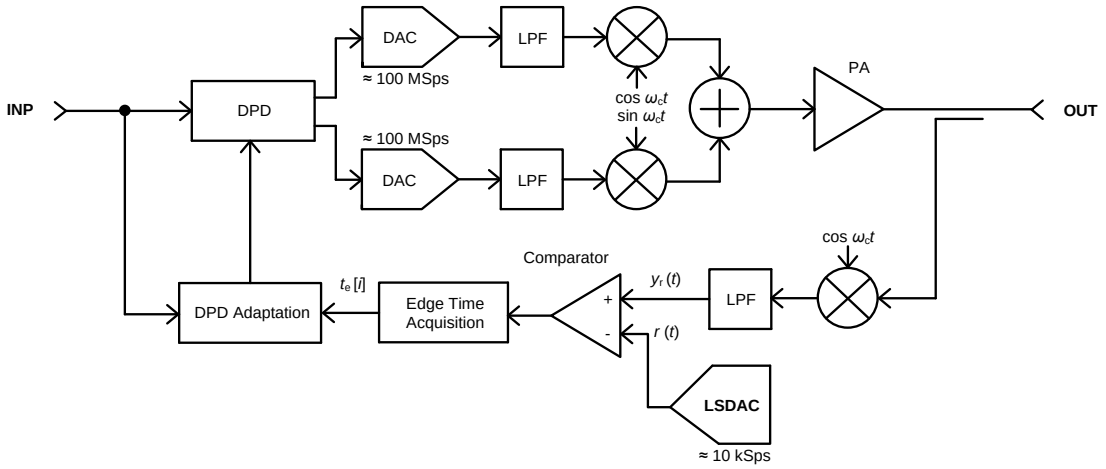

Figure 1: Proposed architecture using comparator in the feedback path.

The signal is compared with the output voltage level of the LSDAC (Low Speed Digital-to-Analog Converter). The comparator output edges indicate the input crossing the set voltage level at time instants $t_e[i]$, where i is the edge index. These time instants are acquired by the edge time acquisition circuit, which is described in the next paragraph. The output signal restoration can be described as follows:

$$y_r(t_e[i]) = r\ (t_e[i]), \tag{1}$$

where $y_r\ (t_e[i])$ denotes a level of the demodulated signal and $r\ (t_e[i])$ equals to a specific voltage level on the LSDAC output at appropriate time instant $t_e[i]$. The entire system is synchronized with single clock signal distributed all over the system the components ensuring the overall coherence between the transmitted and received samples.

3.1 EDGE TIME ACQUISITION CIRCUIT

The essential part of the feedback chain is the edge time acquisition circuit which is depicted in Fig. 2. This block consists of two D flip-flops with connected inputs in parallel but note that at the input of the first one there is a delay path. Subsequently, the comparator output signal edge is acquired at the rising edge of the clock signal. The acquisition precision depends on the set delay and timing properties of the D flip-flops and the clock signal distributor.

The acquisition of the time instants is not intended as the whole signal restoration at the certain sampling rate. It is sufficient to provide just several samples of the output signal at any time for the DPD coefficients estimation.

The time acquisition circuit has been simulated using OrCAD PSpice environment and the results can be seen in Fig. 2 on the right. On the upper side, there is depicted signal of the comparator input and on the following chart there are the inputs and outputs of D flip-flops. The simulation maintains the clock signal frequency of 100 MHz and the set delay equals to 6 ns.

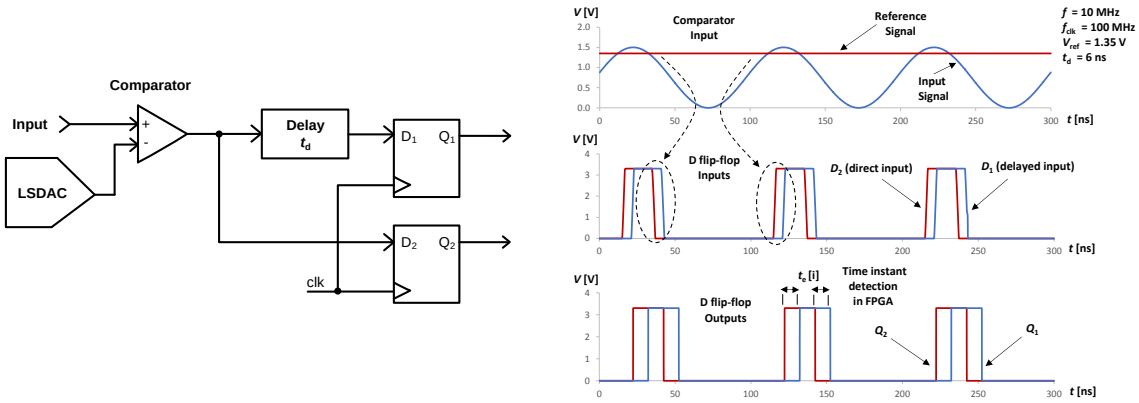

Figure 2: Edge time acquisition circuit (on the left), the simulation results (on the right).

4 PROPOSED ARCHITECTURE EVALUATION CONCEPT

For the purpose of the architecture evaluation a concept depicted in Fig. 3 has been proposed. The core component of the system is the FPGA module Spartan-3A DSP 1800A containing a firmware and stored IQ data samples. These data are transmitted by the DAC Module. The output analog signal follows through the PA and attenuator and finally it is reaching the acquisition module which is the main objective of the development. The acquired edge time instants are sent back to the FPGA module afterwards. In the end, communication with PC (Personal Computer) is established and the data are transferred to the MATLAB software.

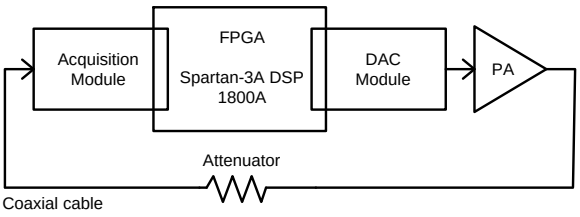

Figure 3: Evaluation concept of the proposed architecture.

4.1 ACQUISITION MODULE DEVELOPMENT

The main objective of the development is the acquisition module containing demodulator, edge time detector circuit, clock signal distributor, and auxiliary components for communication with the FPGA module. The design has to fulfill the following requirements: the maximum working carrier frequency has to be 1600 MHz and the maximum frequency of the clock signal 500 MHz. In accordance with the required timing properties, the clock distributor and the D flip-flops have been selected to achieve the best performance.

The PCB (Printed Circuit Board) has been developed in KiCad environment. The description of the design steps is out of the scope of this paper, but the source files are available online [5]. The PCB is based on IS400 substrate of the 1.6 mm thickness. The manufactured and assembled PCB can be seen in Fig. 4 on the left side.

An appropriate firmware has been developed in VHDL (Very High Speed Integrated Circuit Hardware Description Language). The program flowchart is depicted in Fig. 4 on the right side. In the beginning, all the component registers have to be set up, subsequently, the transmission of the signal samples is started along with the data acquisition. After the last sample is sent, the stored data is transferred to PC (Personal Computer) for the further processing in MATLAB environment.

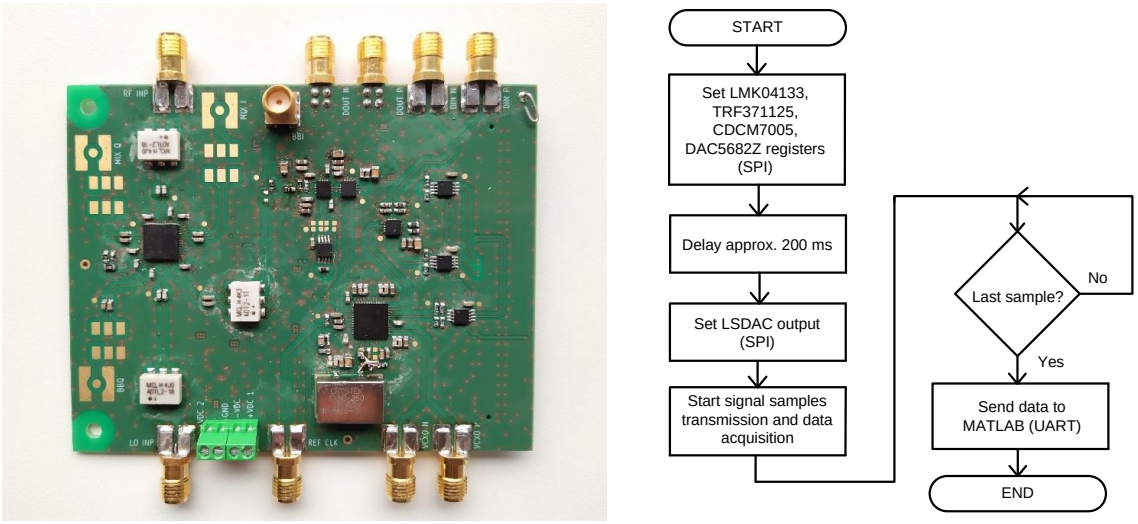

Figure 4: PCB design (on the left), flowchart of the proposed FW (on the right).

5 CONCLUSION

This paper presented the design of the acquisition module for the adaptation of a digital predistorter to linearize power amplifiers. The comparator deployment in the feedback path instead of ADC has been proposed. The PCB of the acquisition module has been developed along with an appropriate firmware in VHDL. The future steps are going to be focused on the hardware verification and the overall assessment of the architecture employment in real DPD systems.

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REFERENCES

[1] GÖTTHANS, Tomáš. *Advanced methods for analyzing non-linear dynamical systems* [online]. Université Paris-Est, 2014 [cit. 2020-05-05]. Available at: https://tel.archives-ouvertes.fr/tel-01127560/file/2014PEST1020.pdf

[2] TEIKARI, Ilari. *Digital Predistortion Linearization Methods for RF Power Amplifiers* [online]. Helsinki University of Technology., 2008 [cit. 2020-05-05]. Available at: https://pdfs.semanticscholar.org/e96b/cf6a9e14949b1ad82673b9149163fbd685ea.pdf

[3] WANG, H. et al. Forward modeling assisted 1-bit data acquisition based model extraction for digital predistortion of RF power amplifiers. *IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR).* Phoenix: IEEE, 2017. pp. 59-62.

[4] WANG, H. et al. 1-bit Observation for Direct-Learning-Based Digital Predistortion of RF Power Amplifiers. *IEEE Transactions on Microwave Theory and Techniques*, 2017, vol. 65, no. 7, pp. 2465-2475.

[5] *PCB files repository* [online]. [cit. 2020-05-05]. Available at: https://github.com/ljagla/kicad-masters-thesis