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Abstract In this paper, we present six area-efficient transimpedance type second-order analog filters. There are many applications where the available signal is current, however the necessary signal for further processing is voltage type. For such applications the presented circuits will be a useful solution. The technique employed is called MOS-only technique and to the best of our knowledge this is the first attempt to implement transimpedance type filters with MOS-only technique. Starting from the core circuit biasing is illustrated and the functionality is shown with LT SPICE simulations using TSMC 0.18u technology parameters. From six core circuits one circuit is selected and the design is completed for illustration purpose.

Keywords MOS Only Filter; MOS-C Filter, Band Pass filter, Transimpedence Filter, Analog Filter

1. Introduction

For an analog filter, in general the input and output variables can be selected independently as voltage or current and this permits four types of circuits, namely voltage mode, current mode transimpedance mode, and transadmittance mode filters. The first type was dominating for many decades, it is used in industrial designs and taught in textbooks, the designs are mainly based on opamps, however current mode counterparts received also attention in the last several decades [1–4]. In many publications the latter type employed current conveyors or similar active elements derived from it. For higher frequencies, other types of filters (e.g. [5, 6]), gm-RL [7], or gm-C [8] type filters can be used. Transimpedance or transadmittance types are also useful depending on application and some related design examples are published before [9–11]

MOS-only approach for circuit design is an alternative approach receiving significant attention during the last decade due to new possibilities it offers [12]. Simplicity in design, component reduction, increase in operating frequency and low cost are some of the advantages. A further advantage is their direct plug-in possibility to the analog or mixed-signal integrated circuit (IC) design. However, this needs some IC design experience if the design needs to be optimized considering other hardware existing in the parent design. MOS-only circuits will roughly fall into two different categories. The first group employs the gate-to-source (C_{gs}) parasitic capacitance of the MOS transistor together with its transconductance g_m to obtain the filtering function. Highest possible frequencies with MOS technology can be achieved. There is some concern on about this type of filters. They will suffer from large manufacturing tolerances and nonlinearity of C_{gs}. The tolerance problem can be solved with automatic tuning techniques. The second group employs MOS capacitors or poly-poly capacitors as the filter capacitor to eliminate the mentioned nonlinear behavior. Poly-poly capacitors can also be employed in the first group to reduce nonlinearity and to decrease the variation due to the tolerance issue. Previously presented related circuits from MOS-only literature are [12–14]].

Transimpedance type MOS-only circuits (or MOS-C) which fall into the second category were presented in

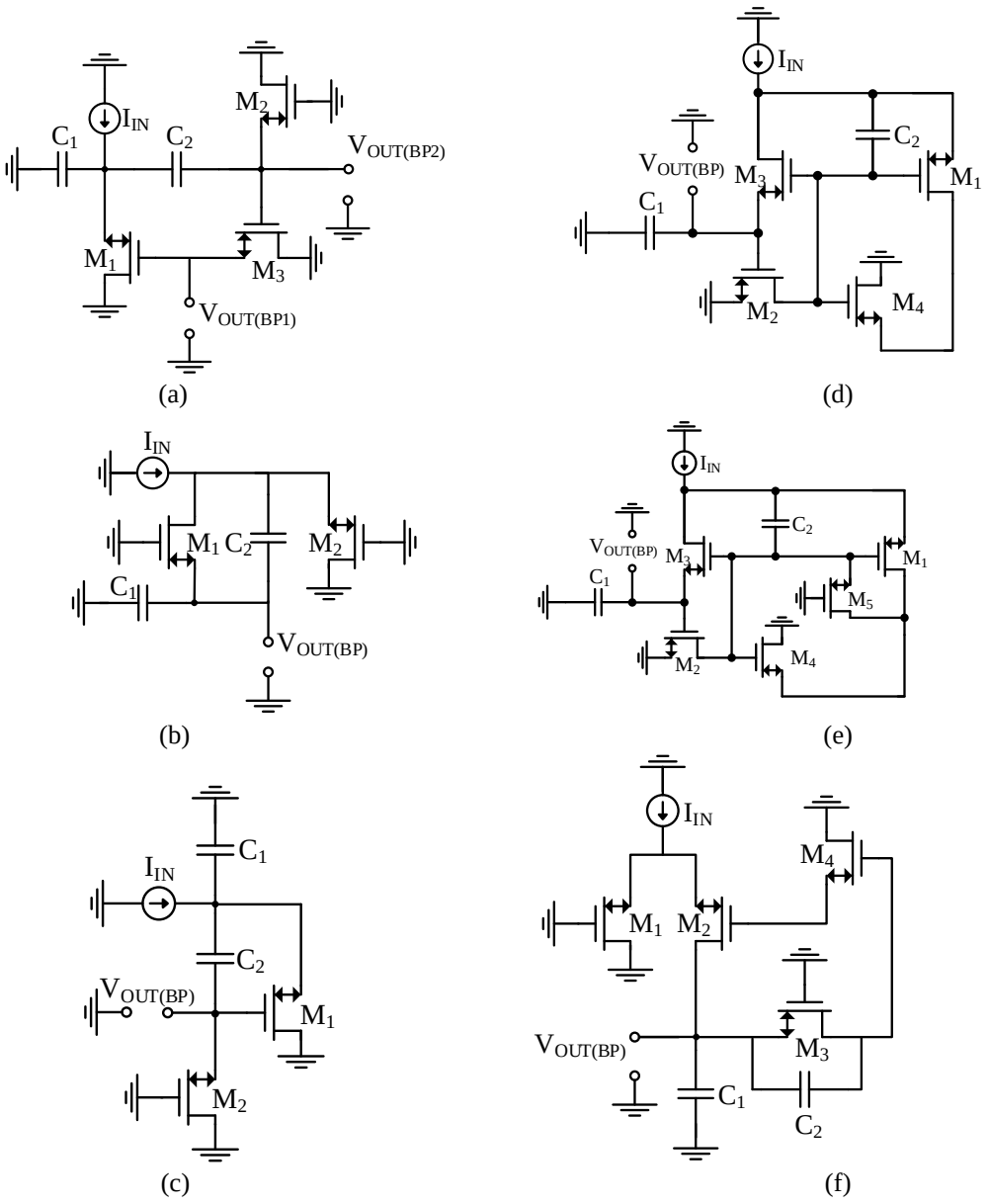

Fig. 1. The core circuits of the proposed transimpedance filters (without bias)

[14]. In this study we present a total of six transimpedance type MOS-only circuits (or MOS-C) which fall into this category. In many of the publications in the literature active component count is a comparison parameter in analog filter designs. This is due to the fact that reduced chip area is expected from these filters and also one expects lower power consumption [12]. The general philosophy of MOSFET-only design approach is as follows: In these circuits only metal-oxide-semiconductor transistors operating in the saturation region are employed instead of generic active building blocks. Therefore instead of a passive resistive element, the transconductance, g_m parameter of MOS transistor is used to obtain resistive (or conductive) dimension. The presented circuits in this study, are easily integrable to an existing analog design with some integrated circuit design experience. They can also be used as independent filter circuits. The design procedure is shown to give guidelines to the IC design engineer.

2. The Six Proposed Transimpedance Filter Circuits

Transimpedance type filters cannot be cascaded with identical filters due to the fact that the input signal is a current and output signal is a voltage. However, these filters are suitable to be used at appropriate interfaces and intermediate stages where the signal types are in desired form.

The six proposed transimpedance type MOS-Only analog filter circuits without biasing components are shown in Fig. 1. These circuits are the core circuits and need DC bias to operate the transistors in saturation regime. The double-sided arrows mean each transistor can be selected as either NMOS or PMOS transistors. However once they are selected the biasing circuit should be designed appropriately. In fact they represent parent circuits and choosing different combinations may result different versions. On the other hand not all of

them may permit biasing in such cases additional transistors may be needed.

When all secondary effects and parasitics of transistors are ignored and they are modeled as ideal transconductors, transfer functions for the first three of these circuits (Fig.1a,b,c) are identical and given in Eq. 1.

$$H(s) = \frac{sC_2}{s^2C_1C_2+s(C_1+C_2)g_{m2}+g_{m1}g_{m2}} \quad (1)$$

Resonant angular frequency and quality factor for these three circuits are given in Eq. 2.

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \qquad Q = \frac{1}{(C_1+C_2)}\sqrt{\frac{g_{m1}C_1C_2}{g_{m2}}} \quad (2)$$

Note that the circuits in Fig. 1a and Fig.1c are related and g_{m3} in Fig. 1a does not appear in the transfer function. Since transistor M3 in Fig. 1a acts as a perfect voltage buffer when all transistors are ideal transconductors, signals at the two nodes labeled as $V_{OUT(BP1)}$ and $V_{OUT(BP2)}$ are identical. Comparison of both circuits illustrates how additional transistors can be inserted without changing the transfer function. This fact is useful when considering biasing conditions. Here M3 does not change the ac analysis results but acts as a dc voltage level shifter. Inserting such transistors appropriately permits easy biasing whenever necessary. Moreover if these cores are used as a plug-in circuit these techniques will be useful when interfacing circuit blocks with different dc levels.

Transfer function for the fourth circuit shown in Fig. 1d is given in Eq. 3.

$$H(s) = \frac{sC_2}{s^2C_1C_2+sC_2g_{m2}+g_{m1}g_{m2}} \quad (3)$$

Resonant angular frequency and quality factor for this circuit is given in Eq. 4.

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \qquad Q = \sqrt{\frac{g_{m1}C_1}{g_{m2}C_2}} \quad (4)$$

Transfer function for the fifth circuit shown in Fig. 1e is given in Eq. 5.

$$H(s) = \frac{s}{C_1\left(1+\frac{g_{m5}}{g_{m3}}\right)\left(s^2+s\frac{\omega_0}{Q}+{\omega_0}^2\right)} \quad (5)$$

Resonant angular frequency and quality factor for this circuit is given in Eq. 6.

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m3}(g_{m2}+g_{m5})}{C_1C_2(g_{m3}+g_{m5})}}$$

$$Q = \frac{\sqrt{g_{m1}g_{m3}(g_{m2}+g_{m5})C_1C_2(g_{m3}+g_{m5})}}{(C_1g_{m1}g_{m5}+C_2(g_{m2}g_{m3}+g_{m5}g_{m3}))} \quad (6)$$

Transfer function for the sixth circuit shown in Fig. 1f is given in Eq. 7.

$$H(s) = \frac{s}{C_1\left(1+\frac{g_{m1}}{g_{m2}}\right)\left(s^2+s\frac{\omega_0}{Q}+{\omega_0}^2\right)} \quad (7)$$

Resonant angular frequency and quality factor for this circuit is given in Eq. 8.

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}g_{m3}}{C_1C_2(g_{m1}+g_{m2})}} \quad Q = \sqrt{\frac{g_{m3}C_1(g_{m1}+g_{m2})}{C_2g_{m1}g_{m2}}} \quad (8)$$

Note that here g_{m4} does not appear in the transfer function thus it does not effect the ac response. However it shifts the dc level. The transfer function is similarly independent from g_{m4} for the circuit in Fig. 1e. Since ideal ac models of both NMOS and PMOS transistors are identical they can be selected arbitrarily as long as biasing is possible.

3. Circuit Design Process with single spacing

The actual design starts by picking up a core circuit, selecting transistor types NMOS or PMOS and biasing it properly. Filter circuits in Fig. 1a and Fig. 1b were studied in detail in [13]. We selected the circuit in Fig. 1d in this study for illustration purpose. Complete circuit with bias is shown in Fig. 2. Since there is no high impedance node in the circuit, biasing circuit is relatively simple. Transistors M8-M11 in Fig. 2 are the current mirrors biasing the core transistors. Transistors M5-M7 are used to bias these current mirrors.

Selected filter circuit is designed for a center frequency of 7 MRad/s which corresponds 1.13 MHz. C1 and C2 capacitor values are 10pF and 1 pF respectively. 10 pF capacitors can be built in a compact area with Double Metal-Insulator-Metal (Double MIM) capacitors in standard CMOS processes. The circuit is

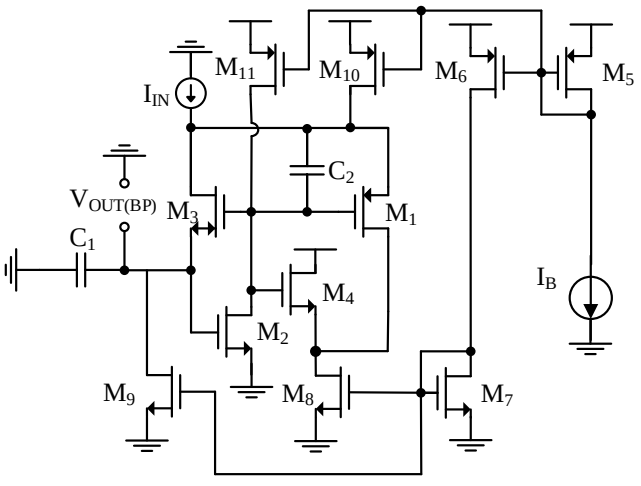

Fig. 2. 4th transimpedance filters with biasing

Table 1. Device sizes and bias currents

	M1	M2-M4	M5-M7	M8	M9	M10	M11	C1	C2
W (µm)	5	2	1	5	10	10	5		
L (µm)	0.5	0.5	1	1	1	1	1		
I_D (µA)	1	1	0.2	1	2	2	1		
Cap (pF)								10	1

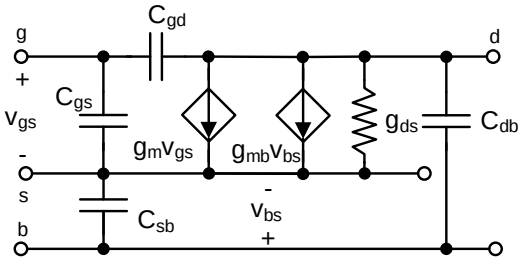

Fig. 3. High frequency small signal model of MOSFET

realized in a 180 nm CMOS process. Lengths of all core transistors are chosen as 500 nm to reduce channel length modulation and other short channel effects. Widths of NMOS transistors are chosen as 2 µm and widths of PMOS transistors are chosen as 5 µm. Transistor transconductances are approximately 20 µS for these sizes for a bias current of 1 µA.

However, a transistor is not a perfect transconductor. Channel Length Modulation acts as a small signal resistor between drain and source (g_{ds}) and Body Effect acts as a second transconductor controlled by bulk to source voltage (g_{mb}). A more complete small signal transistor model including these effects and parasitic capacitances is shown in Fig. 3. Even this model is incomplete and does not reflect short channel effects such as Gate Induced Drain Leakage (GIDL), Drain induced Barrier Lowering (DIBL), Substrate Current Induced body effect (SCBE). These short channel effects have significant effects on transistor behavior in submicron CMOS processes. When these filter circuits are implemented with real transistors, their behavior deviates from the ideal transconductor implementation.

The most problematic nonideal effect is the channel conductance g_{ds} created by channel length modulation. It creates a parasitic signal path between drain and source of the transistor. When drain of a transistor is on the signal path, this component will create significant deviation. When sources or drains of all transistors in a filter topology are grounded, backgate conductance transconductance g_{mb} and channel conductance g_{ds} have no effect or act as resistors from source or drain to ground. However, if both drain and source of a transistor is on the signal path, the feed-forward path through the channel conductance of the transistor will create a zero. Any filter topology with a common gate transistor will suffer from this problem. The added zero will change filter response. Source follower or common source amplifier based filter topologies will act closer to the ideal response.

Channel conductances of M2 and M3 transistors in the 4th filter circuit shown in Fig. 1d provide additional signal paths. Channel conductance of M3 provide a direct connection from input node to output node. Channel conductance of M2 connect C2 to ground. These parallel signal paths move the filter zero to a non zero value.

The transfer function for the fourth filter circuit including the channel conductances of M2 and M3 parasitic capacitors is given in Eq. 9. This equations are simplified considering the fact that channel conductances are much smaller than transconductances for saturated transistors.

$$H(s) = \frac{sC_2g_{m3}+g_{ds2}g_{ds3}}{g_{m3}C_1C_2s^2+g_{m2}g_{m3}C_2s+g_{m1}g_{ds2}C_1s+g_{m1}g_{m2}g_{m3}} \quad (9)$$

This equation clearly shows that zero is not at zero frequency. The channel resistances do not change the second order nature of the transfer function as shown by the denominator. Center frequency, zero frequency and quality factor in this non ideal case are shown in Eq. 10.

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \quad \omega_z = \frac{g_{ds2}g_{ds3}}{C_2g_{m3}}$$

$$Q = \frac{g_{m3}\sqrt{g_{m1}g_{m2}C_1C_2}}{g_{m2}g_{m3}C_2+g_{m1}g_{ds2}C_1} \quad (10)$$

Parasitic capacitances will also affect the frequency response. However, filter capacitors are chosen much larger than transistor parasitic capacitances. Thus their effects will not be significant. Gate to drain (C_{gd}) and gate to source (C_{gs}) parasitic capacitances provide signal paths in parallel with transistors while drain to bulk (C_{db}) and source to bulk (C_{sb}) depletion capacitances provide a path from circuit nodes to ground. Effect of C_{db} and C_{sb} is shorting circuit nodes to ground at very high frequency, so they introduce additional poles at very high frequencies. However, the parallel signal paths introduced by C_{gd} and C_{gs} introduce both zeros and poles.

Capacitors in the circuit can be grouped into four capacitors from circuit nodes to ground and 3 capacitors between circuit nodes. These capacitors are given in Eq. 11.

$$C_{n1} = C_{sb1} + C_{db3} \qquad C_{n2} = C_{gd4} + C_{db2}$$
$$C_{n3} = C_{db1} + C_{sb4} \qquad C_{n4} = C_1 + C_{gs2} + C_{sb3}$$

$$C_{n12} = C_2 + C_{gd3} + C_{gs1} \qquad C_{n23} = C_{gd1} + C_{gs4}$$
$$C_{n24} = C_{gd2} + C_{gs3} \tag{11}$$

Since C_{gs1}, C_{gs2} and are in parallel with main filter capacitances, their effect is simply increasing filter capacitor values. Even if transistors M1 and M2 are relatively large and C_{gs1} and C_{gs2} are not negligible compared to filter capacitors, these added parasitic capacitors will not affect the filter response. However, we must keep in mind that increasing transistor sizes will also increase depletion capacitors C_{db} and C_{sb}, ie. C_{n1}, C_{n2} and C_{n3} will increase. When these capacitors increase, the high frequency poles introduced by these capacitors will move to lower frequencies.

The transfer function for the fourth filter circuit when all parasitic capacitances are included is a very complicated function with 3 zeros and 4 poles. Transfer function can be simplified significantly when C_1 and C_2 are assumed to be much larger than all parasitic capacitances. Since all transistors are operating in saturation, gate to drain capacitors are much smaller than other parasitic capacitances. Therefore, equations can be further simplified ignoring C_{gd} capacitors in comparison to other capacitors. C_{n4} and C_{n12} are larger than all other capacitors. This equation can be simplified to the form including the parasitic capacitors is given in Eq. 12.

$$H(s) \cong \frac{sC_{n12}(g_{m3}+sC_{n24})(g_{m4}+s(C_{n3}+C_{n23}))}{a_4s^4+a_3s^3+a_2s^2+C_{n12}g_{m2}g_{m3}g_{m4}s+g_{m1}g_{m2}g_{m3}g_{m4}} \tag{12}$$

where

$$a_4 = C_{n12}C_{n4}\big(C_{n23}(2C_{n1} + 2C_{n2} + C_{n3}) + C_{n24}(C_{n3} + C_{n23})\big)$$

$$a_3 = C_{n12}C_{n4}\big((C_{n3} + C_{n23})g_{m3} + (C_{n1} + C_{n2} + C_{n24})g_{m4}\big)$$

$$a_2 = C_{n12}C_{n4}g_{m3}g_{m4}$$

Resonant angular frequency and quality factor for this circuit are given in Eq. 13. As long as parasitic capacitances are much smaller than filter capacitances, center frequency and quality factor simplifiers to the values given in Eq. 4.

$$\omega_0 \cong \sqrt{\frac{g_{m1}g_{m2}}{C_{n4}C_{n12}}} \cong \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}$$

$$Q \cong \sqrt{\frac{C_{n4}g_{m1}}{C_{n12}g_{m2}}} \cong \sqrt{\frac{C_1g_{m1}}{C_2g_{m2}}} \tag{13}$$

Eq. 12 shows that there are two extra zeros in addition to the filter zero at 0 Hz and 2 additional poles. These extra zeros and poles affect filter response. When the filter is designed for high Q, first two poles will be complex. 3rd and 4th poles will be real. Approximate values of the extra poles and zeros are given in Eq.14.

$$\omega_{z1} \cong g_{m4}/(C_{n3} + C_{n23}) \qquad \omega_{z2} = g_{m3}/C_{n24}$$

$$\omega_{p3} \cong \left(\alpha + \frac{1}{\omega_{z1}} + \frac{1}{\omega_{z3}}\right)^{-1}$$

$$\omega_{p4} \cong \left(\frac{1}{\omega_{z2}} + \beta\right)^{-1} + \left(\frac{\gamma}{\omega_{z1}} + \delta\right)^{-1} \tag{14}$$

where

$$\alpha = \frac{C_{n1}+C_{n2}}{g_{m3}} \qquad \beta = \frac{C_{n23}(2C_{n1}+2C_{n2}+C_{n3})}{g_{m3}(C_{n3}+C_{n23})}$$

$$\gamma = \frac{C_{n24}}{C_{n1}+C_{n2}+C_{n24}} \qquad \delta = \frac{C_{n23}(2C_{n1}+2C_{n2}+C_{n3})}{(C_{n1}+C_{n2}+C_{n24})g_{m4}}$$

From Eq. 14 one can conclude that the extra poles and zeros are created by transistor parasitics. On the other hand 1st and 2nd poles are linked to ω_0 and Q. Therefore, first 2 poles are determined by filter capacitances C_1 and C_2. If parasitic capacitances are negligible compared to main C_1 and C_2, these extra zeros and poles will be at relatively high frequencies compared to the first 2 poles.

Even the simplified pole and zero expressions in Eq. 15 depend on too many parameters. In order to see the sequence of these values in typical cases, we will calculate these frequencies for device sizes and currents in Table 1. We assume source and drain regions have same geometry and ignore voltage dependence of depletion capacitances. Since size and current of M3 and M4 are equal, transconductances g_{m3} and g_{m4} will be equal. Since channel size and length of source and drain regions are equal, bulk capacitors and gate to source capacitors of NMOS transistors M2-M4 are equal. Gate to source capacitance of M1 will be 2.5 times those of NMOS transistors. Depletion capacitance will be approximately 2.5 times if we assume length of source and drain regions also increase 2.5 times. Gate to drain

capacitors can be ignored since they are much smaller than gate to source capacitors. Zero and pole positions under these assumptions are given in Eq. 15. C_b is either C_{db} or C_{sb} of and NMOS transistor and Cgs is gate to source capacitance of NMOS transistors.

$$\omega_{z1} \cong 2\,g_m/(2C_{gs}+7C_b) \qquad \omega_{z2} \cong g_m/C_{gs}$$

$$\omega_{p3} \cong g_m/(2C_{gs}+8C_b)$$

$$\omega_{p4} \cong g_m/2C_{gs} + 3g_m/(2C_{gs}+32C_b) \qquad (15)$$

ω_{p3} is the smallest one. ω_{z1} is approximately $2\omega_{p3}$. ω_{p4} is larger than ω_{z1}. ω_{z2} is larger than ω_{p4} unless C_{gs} is very large compared to C_d. Slope of filter response will increase after each pole and decrease after each zero. It will go back to its ideal value at frequencies larger than ω_{z2} since they neutralize each other. Actual response and ideal response will be parallel at high frequencies, but magnitude of actual response will be smaller than ideal response due to faster role off between 3rd pole and 2nd zero. Eq. 15 is an approximation. Actual pole and zero values will be different, but it is useful for understanding how frequency response behaves.

4. Simulation Results

Bandpass filter circuit is implemented with ideal voltage controlled current sources and real transistors in 180nm TSMC CMOS process in order to compare ideal circuit behavior and simulated behavior. All branches in the circuit are biased with 1 µA current. Core filter consumes 7.36 µW. Biasing branches are sized smaller than core circuit branches in order to minimize power consumption. Filter biasing branches consume 418 nW.

Ideal and simulated frequency responses of the first filter are shown in Fig. 4. Center frequency of ideal response is at 1.1 MHz as anticipated from calculations. Center frequency of simulated response increases to 1.13 MHz and transimpedance gain decreases with real transistors as expected. Peak value of the transfer function decreases 3.5dB compared to ideal response. However, bandpass characteristics are preserved with real transistors. Parasitic capacitances do not have a significant effect because the parasitics associated with the relatively small transistors are negligible compared to C_1 and C_2.

The biggest deviation from ideal behavior is the flat low-frequency response. Circuits act as bandpass filter for a wide range of frequencies, but magnitude roll-off stops at frequencies lower than the zero created by the channel conductances of transistor M2 and M3. However, there is 90 dB roll-off from the peak value and effects of this zero are negligible. Channel conductances

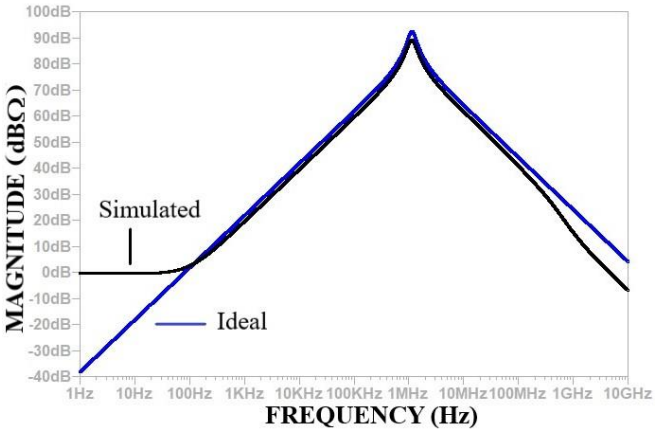

Fig. 4. Frequency Response of the 4th TI Filter

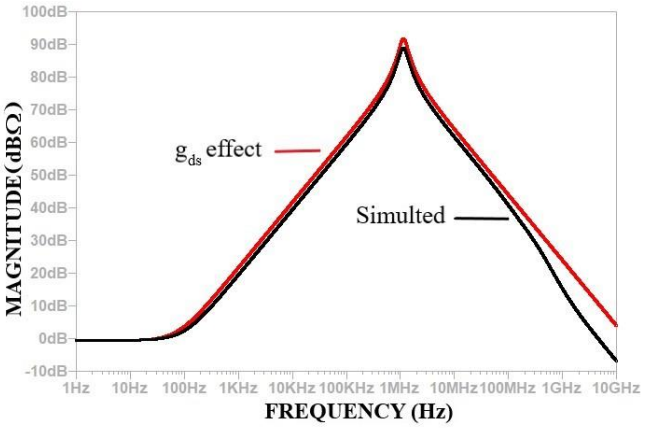

Fig. 5. Frequency Response of the ideal model of 4th TI Filter with channel conductances

of M2 and M3 are added the ideal model to verify the source of low frequency flatting. Fig. 5 shows comparison of this semi ideal model and the actual simulated response. This result clearly shows that the low frequency flatting is the result of channel conductances of M3 and M4. The zero frequency of the model and the actual circuit overlap perfectly.

Parasitic capacitances are responsible for deviations from the ideal behavior at high frequencies as anticipated in Section 3. Fig. 4 shows that simulated response rolls off faster than the expected response. Slope of the simulated response is not constant in the frequency range from 250 MHz to 1.5 GHz. After this frequency range, simulated curve and ideal curve become parallel. This behavior can be explained by 2 poles and 2 zeros positioned in a pole, zero, pole, zero sequence. This exactly what was anticipated from Eq. 15. Simulated response follows the ideal response for more than 2 decades. Since Eq. 15 is just a This means frequency drops more than 40dB before deviations become significant. Moreover, a faster roll off at out of band frequencies is not an undesired property in a filter.

Simulated center frequency shows a good match with ideal response. In fact all analog filters are subject to automatic on chip tuning. Slight deviations in center frequency can easily be compensated.

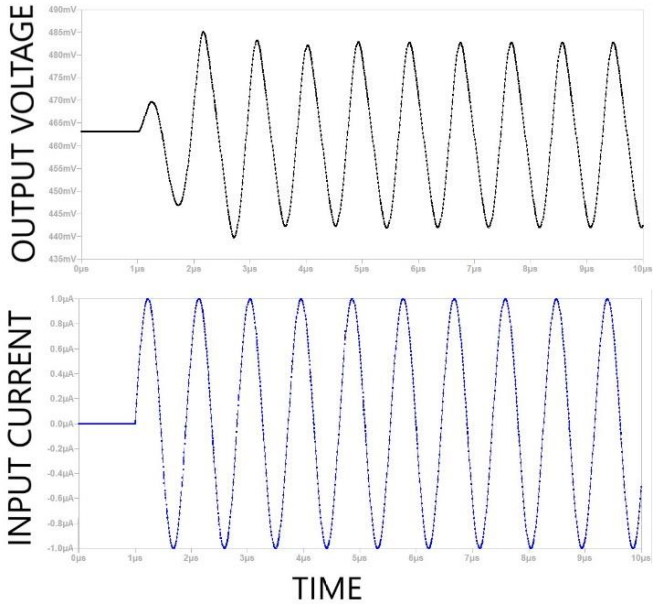

Fig. 6. Time-domain response of 4th TI filter circuit

The time-domain response of the filter circuit to sinusoidal input current is shown Fig. 6. Input current to the circuit is at the center frequency of the circuit. The amplitude of the input current is 1 μA. The filter response settles within two periods after the application of the input signal. Input current and output voltage are in phase as expected since the phase shift is 0° at the center frequency.

5. Conclusions

In this study we presented six core circuits operating as transimpedance filter and are of MOS-C (MOS-only) type. It is shown with ideal and nonideal analyses that these circuits perform as very good filter circuits. To illustrate the functionality and the design procedure one of the selected core circuits is biased properly and simulated with LT SPICE using TSMC 0.18u technology parameters. The presented circuits will be useful in applications where the available signal is current but the signal processing is performed in voltage mode.

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