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New resistorless tunable voltage-mode universal filter using single VDIBA

Norbert Herencsar · Oguzhan Cicekoglu · Roman Sotner · Jaroslav Koton · Kamil Vrba

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Abstract To increase the universality of the recently introduced voltage differencing inverting buffered amplifier (VDIBA), this letter presents a new voltage-mode (VM) multi-input-single-output (MISO) universal filter. The proposed filter contains only single VDIBA, two capacitors, and one nMOS transistor, operated in triode region, and is used for resonance angular frequency tuning. Since in the structure no resistors are needed the filter can be classified as resistorless. The VM MISO filter compared with other active building block-based counterparts is very simple, it contains only few transistors, and has the smallest size area. Moreover, no component matching is required and it shows low sensitivity performance. The theoretical results are verified by SPICE simulations using TSMC 0.18 μm level-7 SCN018 CMOS process parameters with $\pm$0.9 V supply voltages. In addition, the behavior of the proposed VM filter was also experimentally verified using commercially available integrated circuits OPA660 and AD830.

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Keywords Active filter · Multi-input single-output (MISO) · Universal filter · Resistorless filter · Voltage-mode · Voltage differencing inverting buffered amplifier (VDIBA)

1 Introduction

Active filters are widely used as basic building blocks in analog signal processing. They are intended to replace the RLC filters that mainly suffer from the lack of integrability. Such active filter circuits are successfully used in video signal processing, communication systems, computer systems, telephone circuitry, broadcasting systems, control and instrumentation systems, etc. [1]. Recently, several active building block (ABB)-based minimal configuration voltage-mode (VM) multi-input single-output (MISO) universal filter structures have been reported in the literature in which for specific connection both capacitors are used as input terminal [2]–[13]. Unfortunately, the internal structures of ABBs in all of above reported filters suffer from the excessive number of transistors and the complexity of the used ABBs, which results in high silicon area in case of on-chip fabrication. This can be also seen from Table 1, which summarizes the advantages and disadvantages of previously reported VM MISO filters in [2]–[13] based on various relevant criteria. Full nomenclature of referred ABBs is given in Appendix. With the aim to minimize the silicon area on the chip, very recently the new versatile ABB so-called voltage differencing inverting buffered amplifier (VDIBA) has been presented [14]. Its application possibilities have been shown on the design of a resistorless and electronically tunable dual-output VM first-order all-pass filter [14], four-phase quadrature oscillator, second-order all-pass filter [15], single ended

Table 1 Comparison of performance specifications of different VM MISO filters

Ref.	Year	Results	Technology	Power supply	Filter responses	Frequency	No. of ABBs	No. of transistors	No. of passive el.	Passive el. / ABB parameter matching	Total area[e]
[2]	2006	Simul.	CA3080 ICs	±15 V	All, but AP[c]	159.2 kHz	2 OTA	–	2 C	No	–
		Meas.	AD844 ICs	±15 V	All, but AP[c]	159.2 kHz	2 CFA	–	2 C, 2 R	No	–
[3]	2008	Simul.	BJT[b]	±1.5 V	All, but LP[c], BR[c] & AP[c]	56.75 kHz	1 CCCCTA	17 BJT[d]	2 C	Yes	–
[4]	2009	Simul.	BJT[b]	±3 V	All	100 kHz	1 CDTA	23 BJT[d]	2 C, 3 R	No	–
[5]	2009	Simul.	BJT[b]	±3 V	All, but AP[c]	612 kHz	2 CCCDBA	50 BJT[d]	2 C	No	–
[6]	2009	Simul.	BJT[b]	±2 V	All, but AP[c]	1 MHz	1 DBTA	39 BJT[d]	3 C, 2 R	Yes	–
[7][a]	2010	Simul.	TSMC 0.35 μm CMOS	±1.3 V	All, but BR[c] & AP[c]	1.59 MHz	1 FDCCII	60 MOS	2 C, 3 R	Yes	770.65 μm^2
[8]	2010	Simul.	BJT[b]	±3 V	All, but BR[c] & AP[c]	159 kHz	1 CFTA	25 BJT[d]	2 C, 2 R	Yes	–
[9]	2010	Simul.	TSMC 0.35 μm CMOS	±1.65 V	All	1 MHz	1 CCII	24 MOS	2 C, 3 R	Yes	170 μm^2
[10][a]	2010	Simul.	TSMC 0.35 μm CMOS	±1.3 V	All, but BR[c] & AP[c]	1.59 MHz	1 FDCCII	88 MOS	2 C, 2 R	No	1 027.9 μm^2
[11]	2011	Simul.	TSMC 0.35 μm CMOS	±2 V	All, but LP[c], BR[c] & AP[c]	8 MHz	1 DVCC	18 MOS	2 C, 2 R	Yes	199.52 μm^2
[12][a]	2012	Simul.	TSMC 0.35 μm CMOS	±1.5 V	All, but AP[c]	1.19 MHz	2 VDBA	32 MOS	2 C	No	151.9 μm^2
[13]	2013	Meas.	AD830 ICs	±5 V	All	324 kHz	2 DDA	–	2 C, 3 R	No	–
[17]	2011	Simul.	AMS 0.35 μm CMOS	±1.65 V	All	10.7 MHz	No device	7+1 MOS	2 C, 1 R	No	157.29 μm^2
This work	2013	Simul.	TSMC 0.18 μm CMOS	±0.9 V	All	1.59 MHz	1 VDIBA	6+1 MOS[d]	2 C	No	104 μm^2
		Meas.	OPA660 + AD830 ICs	±5 V	All	1.48 MHz	1 VDIBA	–	2 C, 2 R	No	–

Notes:
– Not applicable
[a] [7] Fig. 9(b); [10] Fig. 4; [12] Fig. 3
[b] Transistor parameters NR100N or NR200N (NPN) and PR100N or PR200N (PNP) of bipolar arrays ALA400 from AT&T
[c] For realization additional inverting voltage input needed
[d] Ideal current source(s) assumed
[e] Sum of products of the lengths and widths of each transistors in used CMOS structure incl. VCR area

and differential mode triangle/square wave generators [16].

In this letter we propose a new VM MISO universal filter using the just mentioned VDIBA as active element. The proposed filter structure is an alternative realization to recently published CMOS-RC VM MISO universal filter [17] and compared with other ABB-based counterparts in the literature [2]–[13] and CMOS-RC [17], it shows the following advantages:

(i) compared to circuits in [2], [3], [5]–[8], and [10]–[12] it realizes all five standard filter functions i.e. low-pass filter (LP), band-pass (BP), high-pass (HP), band-reject (BR), and all-pass (AP) without the need of additional inverting voltage inputs, which lead to higher complexity of these solutions,
(ii) proposed filter is resistorless i.e. no external resistor is needed, a useful feature that cannot be found in [2], [4], [6]–[11], [13], and [17],
(iii) it employs only few transistors in total, hence the total transistor area is much smaller than [2]–[13] and [17],
(iv) no passive element or ABB parameter matching is required in the design, which is not available in [3], [6]–[9], and [11],
(v) suitable for low-voltage operation, while circuits [2]–[13] and [17] are supplied with ±1.3 V or higher DC voltages.

SPICE simulation results based on Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 μm level-7 SCN018 CMOS process parameters and experimental measurement results using readily available integrated circuits (ICs) OPA660 and AD830 are included to support the theory.

2 Circuit description

The VDIBA is a recently introduced four-terminal active device with circuit symbol shown in Fig. 1 [15]. It has a pair of high-impedance voltage inputs $v+$ and $v-$, a high-impedance current output z, and low-impedance voltage output $w-$. The input stage of VDIBA can be easily implemented by a differential-input single-output operational transconductance amplifier (OTA), which converts the input voltage to output current that flows out of the z terminal. The output stage can be formed by unity-gain inverting voltage buffer (IVB). Since both stages can be implemented by commercially available

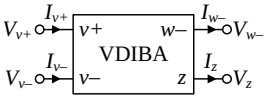

Fig. 1 Circuit symbol of VDIBA.

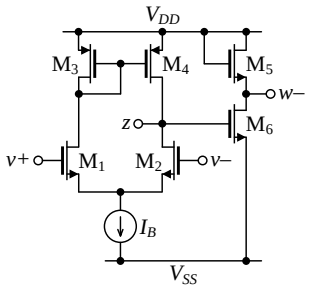

Fig. 2 CMOS implementation of VDIBA.

ICs, and moreover it contains OTA whose g_m can be electronically controllable via DC bias current, the introduced active element is attractive for resistorless and electronically controllable circuit applications.

Using standard notation, the relationship between port currents and voltages of the VDIBA can be described by following hybrid matrix:

$$\begin{bmatrix} I_{v+} \\ I_{v-} \\ I_z \\ V_{w-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & -1 & 0 \end{bmatrix} \begin{bmatrix} V_{v+} \\ V_{v-} \\ V_z \\ I_{w-} \end{bmatrix}, \tag{1}$$

where g_m represents the transconductance of VDIBA.

The CMOS implementation of the VDIBA is shown in Fig. 2. The circuit is composed of an active loaded differential pair (transistors M_1–M_4) followed by a unity-gain IVB (matched transistors M_5 and M_6). The input/output terminal resistances of the CMOS VDIBA shown in Fig. 2 can be found as:

$$R_{ow-} \cong \frac{1}{g_{m5}} \| r_{o6}, \tag{2}$$

$$R_{oz} \cong r_{o4} \| r_{o2}, \tag{3}$$

$$R_{v+} = R_{v-} \cong \infty, \tag{4}$$

where g_{mi} and r_{oi} represents the transconductance and output resistance of the i-th transistor, respectively. From Eqs. (2)–(4) it can be seen that the output terminal ($w-$) can exhibit low resistance by selecting large transistor M_5 (and M_6 due to the matching condition requirement), the input terminals ($v+$ and $v-$), as well as the z terminal, have high resistances.

The proposed VM MISO universal filter is shown in Fig. 3. The circuit employs single VDIBA as active element, two capacitors, and one nMOS transistor working as voltage-controlled resistor (VCR). Although in practice, filters employing only grounded capacitors are preferred, new IC technologies offer floating capacitor realization possibility as a double poly (poly1-poly2) or metal-insulator-metal (MIM) capacitor [18].

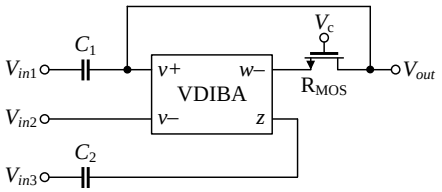

Fig. 3 Proposed VM universal filter.

The nMOS transistor works in triode region and its resistance R_{MOS} for low value of signal amplitudes can be calculated as follows:

$$R_{\mathrm{MOS}} \cong \frac{1}{\mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W}{L} (V_{\mathrm{c}} - V_{\mathrm{THn}})}, \tag{5}$$

where C_{ox} is the gate oxide capacitance per unit area, μ_{n} is the free electron mobility in the channel, W and L are the channel width and length of the nMOS, V_{THn} is the threshold voltage of the transistor, and V_{c} is DC control voltage used for tuning. Using (1), circuit analysis yields the following output voltage V_{out} of the proposed circuit in Fig. 3:

$$V_{out} = \frac{s^2 C_1 C_2 R_{\mathrm{MOS}} V_{in1} - s C_2 V_{in3} + g_m V_{in2}}{s^2 C_1 C_2 R_{\mathrm{MOS}} + s C_2 + g_m}. \tag{6}$$

From Eq. (6) it can be observed that the proper connection of the relevant input terminals yields the five standard types of biquadratic filter functions as follows:

(i) If $V_{in1} = V_{in3} = 0$ (grounded), a second-order LP filter can be obtained with V_{out}/V_{in2};
(ii) If $V_{in1} = V_{in2} = 0$ (grounded), a second-order inverting BP filter can be obtained with V_{out}/V_{in3};
(iii) If $V_{in2} = V_{in3} = 0$ (grounded), a second-order HP filter can be obtained with V_{out}/V_{in1};
(iv) If $V_{in3} = 0$ (grounded) and $V_{in1} = V_{in2} = V_{in}$, a second-order BR filter can be obtained with V_{out}/V_{in};
(v) If $V_{in1} = V_{in2} = V_{in3} = V_{in}$, a second-order AP filter can be obtained with V_{out}/V_{in}.

Thus, the circuit is capable of realizing LP, BP, HP, BR, and AP responses from the same topology without any requirement for component-matching conditions or use of additional inverting voltage inputs. For all filter responses the resonance angular frequency ω_0, quality factor Q, and bandwidth ω_0/Q derived from the denominator of Eq. (6) are:

$$\omega_0 = \sqrt{\frac{g_m}{C_1 C_2 R_{\mathrm{MOS}}}}, \tag{7}$$

$$Q = \sqrt{\frac{C_1 g_m R_{\mathrm{MOS}}}{C_2}}, \tag{8}$$

$$\frac{\omega_0}{Q} = \frac{1}{C_1 R_{\mathrm{MOS}}}. \tag{9}$$

It should be noted that the gain factors for all five filter responses are equal to unity in magnitude.

A sensitivity study forms an important index of the performance of any active network. The active and passive relative sensitivities of the proposed circuit derived from (7)–(9) are given as:

$$S_{g_m}^{\omega_0} = -S_{C_1,C_2,R_{\mathrm{MOS}}}^{\omega_0} = \frac{1}{2}, \quad S_{C_1,g_m,R_{\mathrm{MOS}}}^{Q} = -S_{C_2}^{Q} = \frac{1}{2},$$

$$S_{C_1,R_{\mathrm{MOS}}}^{\omega_0/Q} = -1. \tag{10}$$

From the results it is evident that the sensitivities are low and not larger than unity in absolute value.

3 Stability analysis

Considering the non-idealities of the VDIBA, the matrix relationship of Eq. (1) converts to:

$$\begin{bmatrix} I_{v+} \\ I_{v-} \\ I_z \\ V_{w-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m(s) & -g_m(s) & sC_z + 1/R_z & 0 \\ 0 & 0 & -\beta(s) & R_{w-} \end{bmatrix} \begin{bmatrix} V_{v+} \\ V_{v-} \\ V_z \\ I_{w-} \end{bmatrix}, \tag{11}$$

where the parasitic impedance R_z is ideally infinity as well as C_z and R_{w-} are ideally equal to zero and the β and g_m are non-ideal voltage and transconductance error gains of VDIBA, respectively.

Considering the effects of these non-ideal gains on the proposed filter, the output voltage V_{out} in Eq. (6) turns to:

$$V_{out} \cong \frac{s^2 C_1 C_2 R_{\mathrm{MOS}} V_{in1} - \beta s C_2 V_{in3} + \beta g_m V_{in2}}{s^2 C_1 C_2 R_{\mathrm{MOS}} + s C_2 + \beta g_m}. \tag{12}$$

It should be mentioned that non-ideal gains β and g_m are frequency-dependent parameters that using a single-pole model [19] can be defined as follows:

$$\beta(s) = \frac{\beta_o}{1 + s\tau_\beta}, \tag{13}$$

$$g_m(s) = \frac{g_{mo}}{1 + s\tau_{g_m}}, \tag{14}$$

where $\beta_o = 1 - \varepsilon_{\beta_v}$ and $g_{mo} = g_o(1 - \varepsilon_{g_m})$ are DC voltage and transconductance gains of VDIBA, respectively. Ideally, the voltage gain β_o is equal to unity. Considering the VDIBA implementation using internal structure shown in Fig. 2, at low and medium frequencies these DC gains can be assumed to be constants with following values of tracking errors obtained by SPICE simulations (for $I_B = 100$ μA): $\varepsilon_{\beta_v} = 0.078$ and $\varepsilon_{g_m} = 0.004$, respectively, while $g_o = 600$ μA/V. In addition, $\tau_\beta = 1/\omega_\beta$ and $\tau_{g_m} = 1/\omega_{g_m}$ in which ω_β and ω_{g_m} are -3 dB cut-off frequency of the corresponding gain responses found to be $f_{\beta-3\mathrm{dB}} = 51.93$ GHz and $f_{g_m-3\mathrm{dB}} = 226.32$ MHz. Hence, the maximum operating frequency of the VDIBA is $f_{max} \ll (1/2\pi) \times \min\{\omega_\beta, \omega_{g_m}\} \approx 226.32$ MHz. As it can be seen the τ_β is much smaller than τ_{g_m}. This is due to the fact that the unity-gain IVB stage (M_5 and M_6) can achieve a much higher bandwidth because its output impedance is quite small, ideally equal to zero [20].

The best way to test the stability of the proposed filter characteristics is the use of Routh–Hurwitz stability criterion [21]. Thus, assuming that the single-pole model analysis gives satisfactory result and neglecting the effect of τ_β, by replacing Eq. (14) into (12) its denominator turns into the following third-order polynomial:

$$D(s) = \sum_{i=0}^{3} (a_i s^i). \tag{15}$$

Here, the coefficients of a_i $(i = 0, 1, 2, 3)$ are calculated as:

$$\begin{aligned} a_0 &= \beta_o g_{mo}, \\ a_1 &= C_2, \\ a_2 &= C_2(C_1 R_{\mathrm{MOS}} + \tau_{g_m}), \\ a_3 &= C_1 C_2 R_{\mathrm{MOS}} \tau_{g_m}. \end{aligned} \tag{16}$$

Thus, in order to prevent stability problems, the following condition should be satisfied:

$$\tau_{g_m} < \frac{C_1 C_2 R_{\mathrm{MOS}}}{\beta_o C_1 g_{mo} R_{\mathrm{MOS}} - C_2}. \tag{17}$$

4 Performance verifications

4.1 Simulation results

To verify the theoretical study, the behavior of the proposed VDIBA-based VM filter shown in Fig. 3 has been verified by SPICE simulations with DC power supply voltages equal to $+V_{DD} = -V_{SS} = 0.9$ V. In the design, transistors are modeled by the TSMC 0.18 μm level-7 SCN018 CMOS process parameters ($V_{\mathrm{THn}} = 0.3725$ V, $\mu_{\mathrm{n}} = 259.5304$ cm^2/(V·s), $V_{\mathrm{THp}} = -0.3948$ V, $\mu_{\mathrm{p}} = 109.9762$ cm^2/(V·s), $T_{\mathrm{ox}} = 4.1$ nm) [22]. The aspect ratios of the OTA (M_1–M_4) and the IVB (M_5 and M_6) were chosen as $W/L_{(\mathrm{M1–M4})} = 18$ μm/1.08 μm and $W/L_{(\mathrm{M5,\ M6})} = 54$ μm/0.18 μm, respectively. Note that the bulk of all transistors is connected to their corresponding sources to prevent body effect and W/L ratio of the transistors M_5 and M_6 were selected sufficiently high to decrease the loading effect.

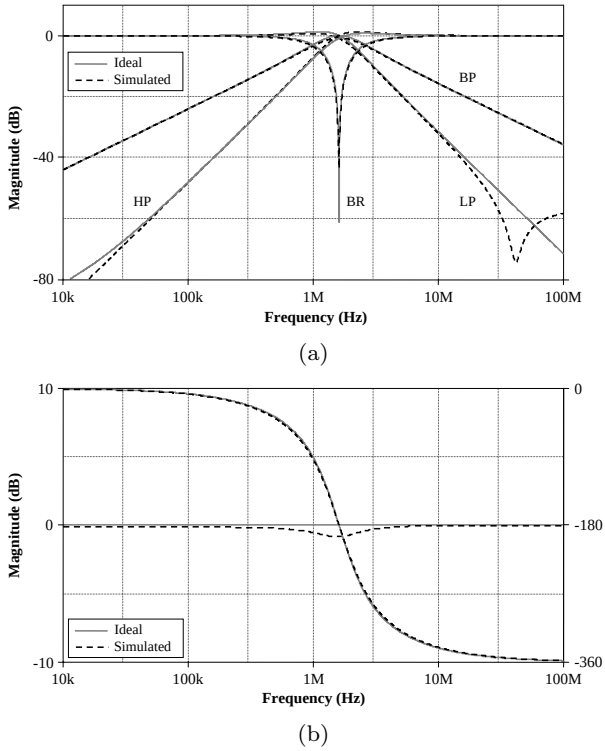

Fig. 4 (a) Ideal and simulated magnitude responses of the low-pass, band-pass, high-pass, and band-reject filters, (b) ideal and simulated magnitude and phase responses of the all-pass filter in Fig. 3.

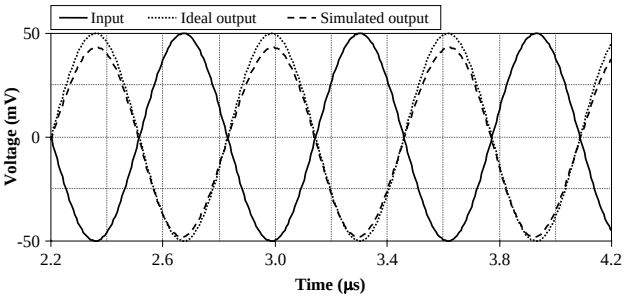

Fig. 5 The output signal of the band-pass response with $Q = 1$ of the filter in Fig. 3 applying a 50 mV (peak) sinusoidal input signal at 1.59 MHz.

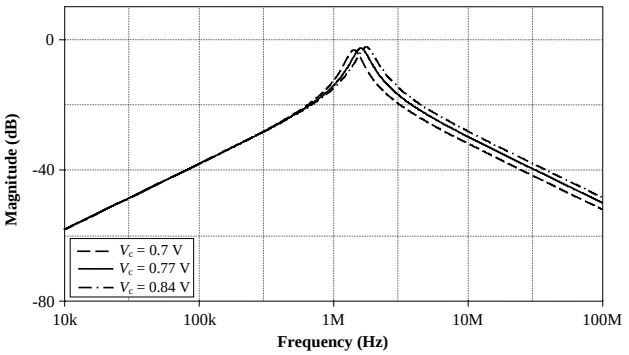

Fig. 6 Electronically tuned high-Q band-pass magnitude responses.

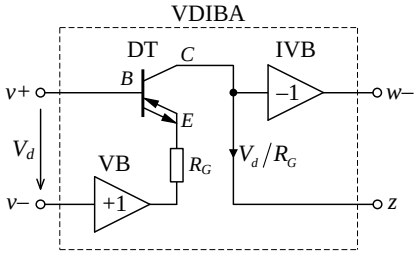

Fig. 7 VDIBA implementation using commercially available ICs.

The proposed filter was designed for $f_0 = \omega_0/2\pi \cong 1.59$ MHz and $Q = 1$ by choosing $C_1 = C_2 = 60$ pF, $I_B = 100$ μA ($g_m = 600$ μA/V), and $R_{\rm MOS} = 1.65$ kΩ obtained with aspect ratio $W/L = 6.3$ μm/1.08 μm and DC control voltage $V_{\rm c} = 0.84$ V. Figure 4(a) shows the ideal and simulated magnitude responses of the low-pass, band-pass, high-pass, and band-reject filters of Fig. 3. Similarly, the ideal and simulated magnitude and phase responses of the all-pass filter are shown in Fig. 4(b). Thus, from Fig. 4(a) and (b) it can be observed that the proposed circuit is capable of realizing all the five standard filter functions as expected. Also, the time-domain response of the proposed filter in Fig. 3 is investigated by applying a sinusoidal input voltage signal with an amplitude of 50 mV peak at $f_0 = 1.59$ MHz. Figure 5 shows the input and output signals of the band-pass response of the proposed filter. The total harmonic distortion (THD) of the output signal is found to be 3.15%.

To demonstrate electronic tunability of the proposed VM filter, pole frequency is tuned around the expected frequency of 1.59 MHz by varying DC control voltage $V_{\rm c}$ of VCR $R_{\rm MOS}$ for a high-Q band-pass response of the filter. In this case, for $Q = 5$ the component values were selected as $C_1 = 250$ pF, $C_2 = 8$ pF, $I_B = 52$ μA ($g_m = 400$ μA/V), and $R_{\rm MOS} = 2$ kΩ obtained with above given aspect ratio and DC control voltage $V_{\rm c} = 0.77$ V. By slightly varying $V_{\rm c}$ as it is demonstrated in Fig. 6, the changes in $R_{\rm MOS}$ will be small. Since the value of the quality factor is proportional to the square root of $R_{\rm MOS}$, its value will not be seriously affected, whereas the resonance angular frequency will be tuned.

4.2 Experimental measurements

In order to confirm the theoretical results, the proposed filter has been developed on printed circuit board

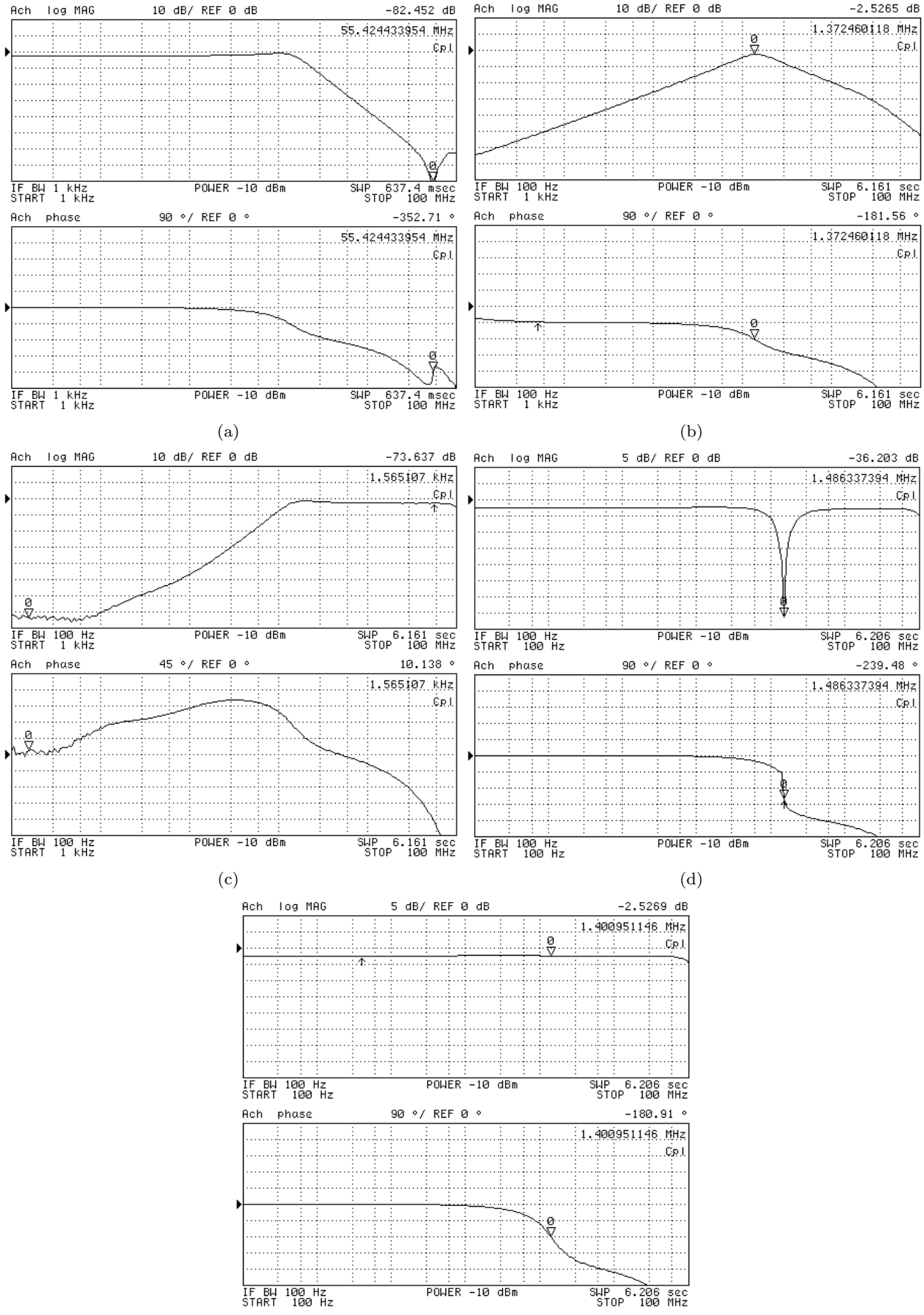

Fig. 8 Measured magnitude and phase responses of (a) low-pass, (b) band-pass, (c) high-pass, (d) band-reject, and (e) all-pass filters.

(PCB) and its behavior has been verified by experimental measurements using network-spectrum analyzer Agilent 4395A. In measurements the VDIBA was implemented based on the structure illustrated in Fig. 7. To realize the input stage of VDIBA the readily available IC OPA660 by BURR BROWN [23] was used, which contains the so-called 'diamond' transistor (DT) and fast voltage buffer (VB). The resistor R_{ADJ} was chosen as 220 Ω [23]. In order to increase the linearity of collector current versus input voltage V_d, the DT is complemented with degeneration resistor $R_G \gg 1/g_{mT}$, added in series to the emitter, where the g_{mT} is the DT transconductance. Then the total transconductance decreases to the approximate value $1/R_G$ [23]. The output stage IVB was realized by IC AD830 produced by Analog Devices [24]. The DC power supply voltages of both ICs were equal to ± 5 V. In all measurements the values of the passive components were selected as $C_1 = C_2 = 100$ pF and $R_G = R_{\mathrm{MOS}} = 1$ kΩ to obtain the designed MISO filter responses with $Q = 1$ at pole frequency $f_0 = \omega_0/2\pi \cong 1.59$ MHz. Measured results of LP, BP, HP, BR, and AP magnitude and phase responses are shown in Fig. 8. From the results it can be observed that due to extra parasitic capacitances of the fabricated PCB the resonance frequency is $f_0 \cong 1.48$ MHz, which, however, is close to the theoretical one.

From the simulation results and experimental measurements it can be seen that the final solution is in good agreement with the theory.

5 Conclusion

This letter presents a new VM MISO universal filter to increase the universality of the recently introduced new 'voltage differencing' device so-called voltage differencing inverting buffered amplifier. The proposed circuit is very simple and realizes all five standard filter functions, i.e. LP, BP, HP, BR, and AP in the same circuit topology without need of additional inverting voltage inputs. The proposed filter achieves easy tuning of the resonance angular frequency without seriously affecting the quality factor. In brief, the new filter offers the following advantages: (i) resistorless circuit, (ii) simple structure containing only few transistors, hence, the total transistor area is much smaller that available circuits in the literature, (iii) no component matching is required, (iv) it shows low sensitivity performance, and (v) suitable for low-voltage operation. SPICE simulations and experimental measurements using commercially available ICs confirm the feasibility of the proposed circuit.

6 Appendix

This section provides full nomenclature of the aforementioned ABBs in Table 1.

OTA	Operational transconductance amplifier
CFA	Current feedback amplifier
CCCCTA	Current controlled current conveyor transconductance amplifier
CDTA	Current differencing transconductance amplifier
CCCDBA	Current-controlled current differencing buffered amplifier
DBTA	Differential-input buffered and transconductance amplifier
FDCCII	Fully differential current conveyor
CFTA	Current follower transconductance amplifier
CCII	Second-generation current conveyor
DVCC	Differential voltage current conveyor
VDBA	Voltage differencing buffered amplifier
DDA	Differential difference amplifier
VDIBA	Voltage differencing inverting buffered amplifier

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