SOLAR POWER INVERTER

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Abstract: Design of a solar power inverter with 1 kW output power capability is discussed in this paper. Interleaved boost topology used in the step-up stage as well as the output full-bridge stage are described. Control block utilizing Field-programmable-gate-array (FPGA) is described as well.

Keywords: FPGA, boost converter, full-bridge converter, MPPT

1. INTRODUCTION

Solar power is becoming more and more important in these days. While there are many MCU-based inverter designs reported in the literature, designs based on FPGAs are rather rare. FPGAs, compared to MCUs (or DSPs), may offer additional advantages like parallel signal processing capability and pin assignment versatility, which may ease the PCB design.

2. POWER CONVERSION PROCESS

Commercially available photovoltaic panels produce DC voltage ranging from few volts to few hundred volts. This DC voltage must be converted to an AC voltage in order to make the power available to the supply network. Furthermore, the power converter serves another purpose - it has to draw maximal power available from the panel. The input voltage and current are measured to determine if the power drawn from the panel is at the highest possible level. In other words, it does source and load impedance matching.

2.1. CONVERTER TOPOLOGY

Transformer-less boost converter was selected for the first (DC-DC) stage. It has some advantages compared to, for example, push-pull topology - the effects of parasitic inductances are not as severe as in transformer-based topologies, there is no "flux walking" problem, which leads to transformer core saturation. Full-bridge topology was selected as the output DC-AC stage. The input voltage is expected to be as low as 45 V. Assuming that the wasted power of the entire converter at maximum output power is 50 W (including losses in transistors, diodes, inductor windings and cores, capacitors), the total input power is 1050 W. Thus, the input current can be approximately calculated:

$$I = \frac{P_{OUT} + P_{LOSS}}{V_{IN(MIN)}} = \frac{1050}{45} = 23{,}3A \quad (1)$$

To decrease switching and conduction losses, the DC-DC stage was divided into four sections, having inductor currents shifted 90 degrees between each phase. This results in average current of 5,83 A through each phase. The output DC-AC stage is single - it does not handle as large current as the boost stage. Output sine voltage is generated by means of pulse width modulation. The switching frequency of both stages has been selected 20 kHz - to keep switching losses at reasonable level and to reduce EMI emissions in the frequency range of interest. PWM modulated signal of each full-bridge converter leg is filtered by LC filter consisting of 1 mH inductor and 0,0047 mF

capacitor, which means cut-off frequency of 2,3 kHz. The block diagram of the system is shown in Figure 1.

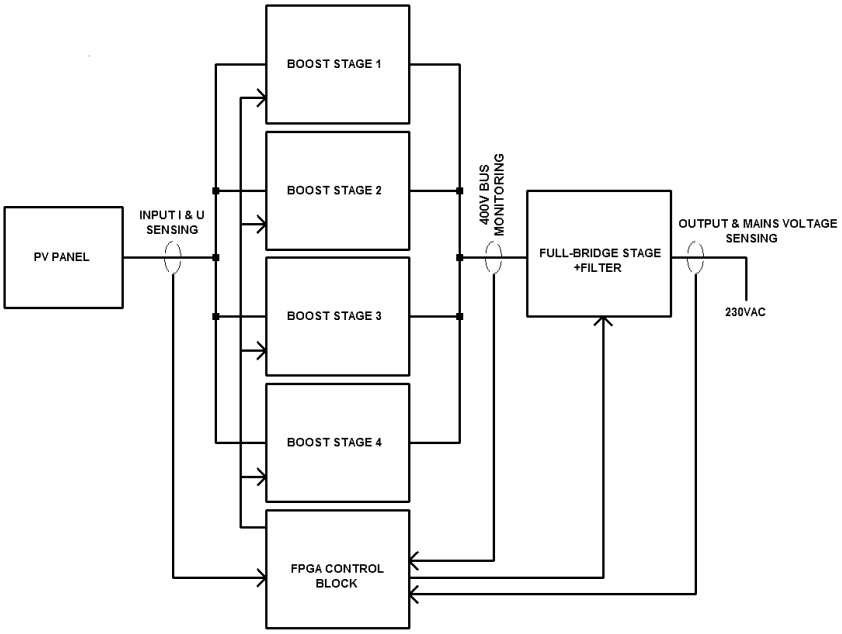

Figure 1: Solar power inverter simplified block diagram

FPGA XC3S200A from Xilinx, together with its power supply DC-DC converters, USB-UART bridge, reference voltage source, ADC converter and current/voltage sensing amplifiers, is placed on a separate six-layer PCB for the purpose of prototyping. Each boost converter phase has its separate double-sided PCB and full-bridge converter has its own double-sided PCB. This approach enables additional features, for example almost arbitrarily increase number of boost phases, or a 3-phase output voltage. Full-bridge stage block diagram is displayed in Figure 2.

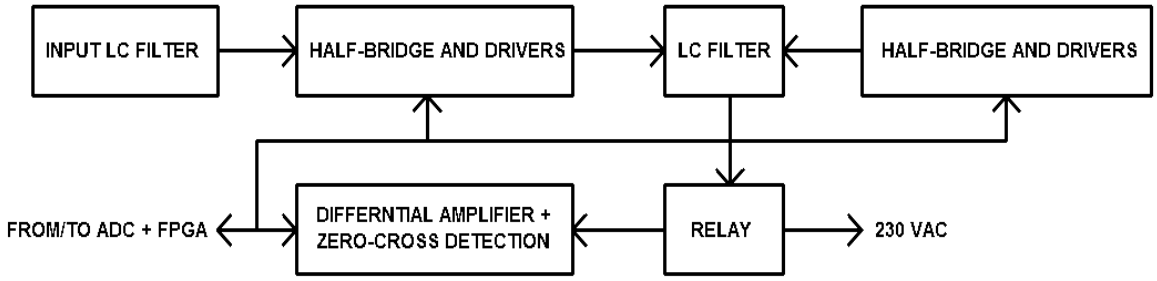

Figure 2: Full-bridge stage simplified block diagram

There are two possible modes of operation - either standalone or connected to the AC mains, in which case the generated sine wave voltage follows the mains voltage. For such case it is very important that the mains and inverter output are separated from each other, until the inverter output is in phase with mains voltage. This is accomplished by power relay. After startup, the phase of the generated voltage is increased, until the difference between mains and generated voltage is zero. Thereafter, the inverter output is connected to the mains and the mains voltage is replicated.

2.2. MAXIMAL POWER POINT CALCULATION (TRACKING)

Assuming constant load connected to the 400 VDC bus, the output voltage of the boost stage is given solely by input power. When lightly loaded, MPPT logic forces maximal duty cycle of the boost stage, in order to keep input power at the maximal level. MPPT logic is based on "Perturb and observe"[1] algorithm. The input current and voltage are multiplied to obtain the input pow-

er. Next a numerical differentiation is conducted to get information if the positive change of duty cycle has caused positive change of the input power. If not, it says that maximal power point has already been reached and the duty cycle is decreased. The duty cycle is decreased as long as the input power rises. After the input power has begun to drop, the duty cycle is increased again and so on.

2.3. SINE WAVE GENERATION

Sine wave samples are stored in the block memory of the FPGA. The principle of Direct digital synthesis was used for this purpose. Phase accumulator (frequency) resolution of 32-bits was selected. This resolution gives output voltage frequency step of approximately 0,0116 Hz (assuming FPGA clock of 50 MHz), which seems adequate. Sine sample resolution is 10-bit amplitude resolution and 10-bit phase resolution - only 10 upper bits of phase accumulator are used to address sine samples in the block memory. The rest of phase accumulator bits, which are not used for sample addressing, is truncated. Then, the sine samples are digitally attenuated (multiplied by factor of 0,85 - multiplied by 205 and 8 upper bits used as the result), which yields maximal amplitude of the generated signal of 330 V, when the inverter input is supplied from the boost stage output, which has nominal voltage of 400 V. The resulting gate drive signal is passed through anti-cross-conduction logic block, which has to avoid that both transistors of a full-bridge leg are switched-on simultaneously.

The resulting sine signal has distortion of approximately 0,7 % as shown in Figure 3, assuming that the most significant high-frequency spectral component (PWM carrier signal in this case) is separated from the 1st harmonic by 42 dB and other harmonics can be neglected as they are too low in magnitude. The converter has been simulated using LTspice IV circuit simulator.

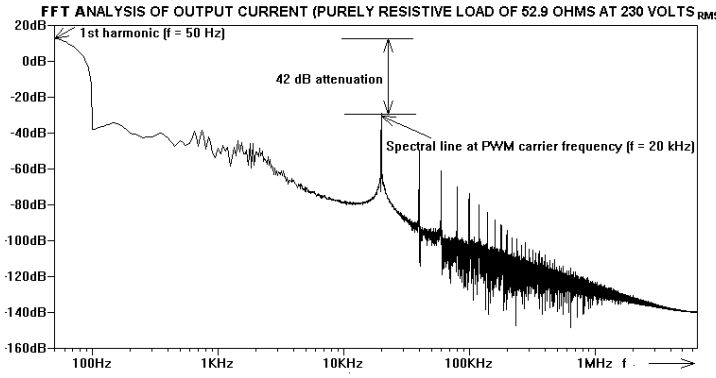

Figure 3: Output current distortion (vertical axis referred to 1 A_{RMS})

3. CONCLUSION

The solar power inverter was designed, simulated and briefly described. The PCBs were designed for the final realization of the project. Simulations have shown theoretical efficiency of 98 %. Nevertheless, the efficiency of the final inverter may vary, due to inherent difficulties of circuit simulations with respect to circuit parasitic elements, which are difficult to model.

REFERENCES

[1] MathWorks. 2010. MPPT Algorithm. [ONLINE] Available at: http://de.mathworks.com/discovery/mppt-algorithm.html. [Accessed 14 March 16].