A Versatile Active Block: DXCCCII and Tunable Applications

Sezai Alper TEKİN [1], Hamdi ERCAN [2], Mustafa ALÇI [3]

[1] Dept. of Industrial Design Engineering, Erciyes University, 38039, Kayseri, Turkey
[2] Dept. of Avionics, Erciyes University, 38039, Kayseri, Turkey
[3] Dept. of Electrical and Electronics Engineering, Erciyes University, 38039, Kayseri, Turkey

satekin@erciyes.edu.tr, hamdiercan@erciyes.edu.tr, malci@erciyes.edu.tr

Abstract. *The study describes dual-X controlled current conveyor (DXCCCII) as a versatile active block and its application to inductance simulators for testing. Moreover, the high pass filter application using with DXCCCII based inductance simulator and oscillator with flexible tunable oscillation frequency have been presented and simulated to confirm the theoretical validity. The proposed circuit which has a simple circuit design requires the low-voltage and the DXCCCII can also be tuned in the wide range by the biasing current. The proposed DXCCCII provides a good linearity, high output impedance at Z terminals, and a reasonable current and voltage transfer gain accuracy. The proposed DXCCCII and its applications have been simulated using the CMOS 0.18 µm technology.*

Keywords

Dual-X current conveyor, low voltage, tunable circuit, controlled oscillator.

1. Introduction

The second-generation current conveyor (CCII) which is the different versions of the current conveyors has achieved to be a functionally usable and accomplished building block for the realization of the analog circuits. Owing to having a variable gain-bandwidth product, high slew rate, wide dynamic range, higher bandwidth and good linearity, these structures have recently become attractive [1].

The current controlled conveyor (CCCII) which is an electronically tunable type of the CCII has been used in many electronic circuit applications as a part of oscillators, inductance simulators, active resistors, filters and multipliers [2-4]. Parasitic resistance seen at the port X of the CCII is fundamentally seen as a drawback in the analog circuit design. Parasitic resistance can be easily tuned by the biasing current. This resistance providing to obtain numerous tunable functions is used to advantage in current controlled conveyors. Furthermore, it provides to reduce the use of passive components in the design.

An active building block combining the main advantages of CCII and inverting second-generation current conveyor (ICCII) is dual-X second generation current conveyor (DXCCII). The dual-X structure of the DXCCII lately popularized by circuit designers helps reducing the number of components used in the same applications. Although the tunability of the DXCCII can be feasible with MOSFET operating triode region, an extra MOS manufacturing process is required for tuning [5]. On the other hand, there are a lot of applications realized using DXCCII such as inductance simulators, oscillators and filters, etc. Some of these circuits suffer from using passive resistors [6-10].

In this work, dual-X controlled current conveyor (DXCCCII) is presented as an active block for tunable applications. The proposed circuit is a new controllable version of the conventional DXCCII. Parasitic resistances of the conveyors, seen at ports X, are controlled by biasing current. However, the proposed circuit does not require external passive or active elements except for DXCCCII to be controlled. The adjustable range of the DXCCIIs is restricted for generally utilized the gate voltage of the MOS transistor as a control argument. The control voltage is limited by supply voltage. The current as a control argument provides facility to tune wider range [2], [11]. Therefore, the current control is more useful than the voltage control for low voltage and low power circuits. Also, DXCCCII operates at low voltage as ±0.75 V. Considering these advantages, the inductance simulators, adjustable oscillator and tunable high pass filter circuits are presented as applications in this work employing the only active elements and the grounded capacitors. The obvious advantage of the proposed oscillator is using less active and passive elements. Also, the grounded and floating active resistors are presented as other applications. Finally, PSpice simulation results are given to validate the theory.

2. Proposed Dual-X Controlled Current Conveyor

The DXCCCII is implemented by using floating gate MOS transistors (FGMOS). The symbol and the equivalent

circuit of an n-type FGMOS transistor with two inputs are shown in Fig. 1. There are several simulation models for the FGMOS transistors in [12-14]. In this proposed circuit, the model is based on connecting capacitors in parallel with the resistors as given in [12].

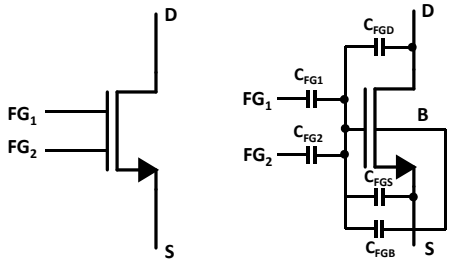

Fig. 1. The n-type FGMOS transistor with three inputs: a) symbol, b) equivalent circuit.

As shown in Fig. 1, FG_1 and FG_2 are the input gate terminals of the FGMOS transistor. The input capacitances are C_{FG1} and C_{FG2} and the input gates are coupled to the floating gate of the FGMOS transistor. C_{FGD}, C_{FGS} and C_{FGB} are the parasitic capacitances between the drain, source, bulk and gate, respectively. Input gate voltages and drain, source and bulk voltages affect an effective floating gate voltage in proportion to the value of the capacitances. When the relation among the capacitances are assumed that $C_{FGD} + C_{FGS} + C_{FGB} << C_{FG1} + C_{FG2}$, the total capacitance C_T is approximately equal to $C_{FG1} + C_{FG2}$. V_{FG} is the effective floating gate voltage and it can be defined as

$$V_{\mathrm{FG}} = \frac{C_{\mathrm{FG1}} V_{\mathrm{FG1}} + C_{\mathrm{FG2}} V_{\mathrm{FG2}}}{C_{\mathrm{T}}}. \tag{1}$$

The drain current of the FGMOS in saturation region can be calculated as

$$I_{\mathrm{D}} = \frac{k_{\mathrm{n}}}{2}\left[V_{\mathrm{FG}} - V_{\mathrm{S}} - V_{\mathrm{TH}}\right]^2 \tag{2}$$

where V_S is the source voltage, V_{FG} is the effective floating gate voltage, V_{TH} is the threshold voltage and I_D is the drain current of the FGMOS transistor. In addition, k_n known as the transconductance parameter is $\mu_n . C_{ox} . (W/L)$ where W/L is the aspect ratio of the FGMOS transistor.

The block diagram of the dual-X second generation controlled current conveyor as a versatile active element is demonstrated in Fig. 2. The proposed circuit has six terminals and principle of the operation is similar to the conventional DXCCII [15]. Y and Z terminals of the DXCCCII have high impedances.

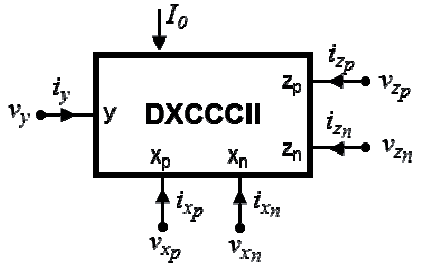

Fig. 2. The symbolic representation of the DXCCCII.

The impedances of the X terminals exhibit a resistance behavior known as a parasitic resistance and its value can be tuned by bias current I_0 of the DXCCCII. The matrix equations of the DXCCCII can be characterized in the following form:

$$\begin{bmatrix} I_Y \\ V_{X_p} \\ V_{X_n} \\ I_{Z_p} \\ I_{Z_n} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_{X_p} & 0 \\ -1 & R_{X_n} & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} V_Y \\ I_{X_p} \\ I_{X_n} \end{bmatrix}. \tag{3}$$

The effective floating gate voltages of M_1 and M_2 transistors are V_{FG1} and V_{FG2}. A loop equation written from floating gate of M_2 to floating gate of M_1 transistor can be expressed as

$$V_{\mathrm{FG2}} - V_{\mathrm{FGS2}} + V_{\mathrm{FGS1}} - V_{\mathrm{FG1}} = 0. \tag{4}$$

If it is supposed that $C_{FG1} = C_{FG2} = C_{FG}$, the total capacitance C_T is equal to $2C_{FG}$. The gate-source voltages in (5) can be given as $V_{FG1} = (1/2)V_Y$ and $V_{FG2} = (1/2)V_{Xp}$. If the related equation is arranged, it can be written as below.

$$V_{\mathrm{FGS2}} - V_{\mathrm{FGS1}} = \frac{1}{2}\left(V_{X_p} - V_Y\right). \tag{5}$$

The drain currents of the transistors M_1 and M_2 can be defined as

$$I_{\mathrm{D1}} = \frac{1}{2} k_{\mathrm{n}} \left(\frac{W}{L}\right)\left(\frac{1}{2}V_{\mathrm{Y}} - V_{\mathrm{TH}}\right)^2. \tag{6.a}$$

$$I_{\mathrm{D2}} = \frac{1}{2} k_{\mathrm{n}} \left(\frac{W}{L}\right)\left(\frac{1}{2}V_{X_P} - V_{\mathrm{TH}}\right)^2. \tag{6.b}$$

I_{D1} and I_{D2} are the drain currents of the transistors M_1 and M_2, respectively. The expression belonging to the difference voltage of the terminals X_p and Y can be defined as $V_{XYp} = V_{Xp} - V_Y$.

The relationship between input voltages is given below.

$$V_{XY_p} = 2 \cdot \left[\sqrt{\frac{I_0 + I_{X_p}}{k_n (W/L)}} - \sqrt{\frac{I_0 - I_{X_p}}{k_n (W/L)}}\right]. \tag{7}$$

where I_0 is the biasing current of the differential pair structures. The current I_{Xp} shown in Fig. 3 can be calculated as shown in (8)

$$I_{X_p} = \frac{1}{2} V_{XY_p} \sqrt{k_n (W/L)} \sqrt{2I_0 - \frac{1}{2} k_n (W/L)(V_{XY_p})^2}. \tag{8}$$

From (8), it is assumed that $2I_0 >> k_n(W/L)(V_{XYp})/2$ for small input voltages. Using this approximation, the output current of the differential pair I_{Xp} is obtained as

$$I_{X_p} \cong \frac{1}{2} V_{XY_p} \sqrt{\frac{1}{2} k_n (W/L)} \sqrt{2I_0}. \tag{9}$$

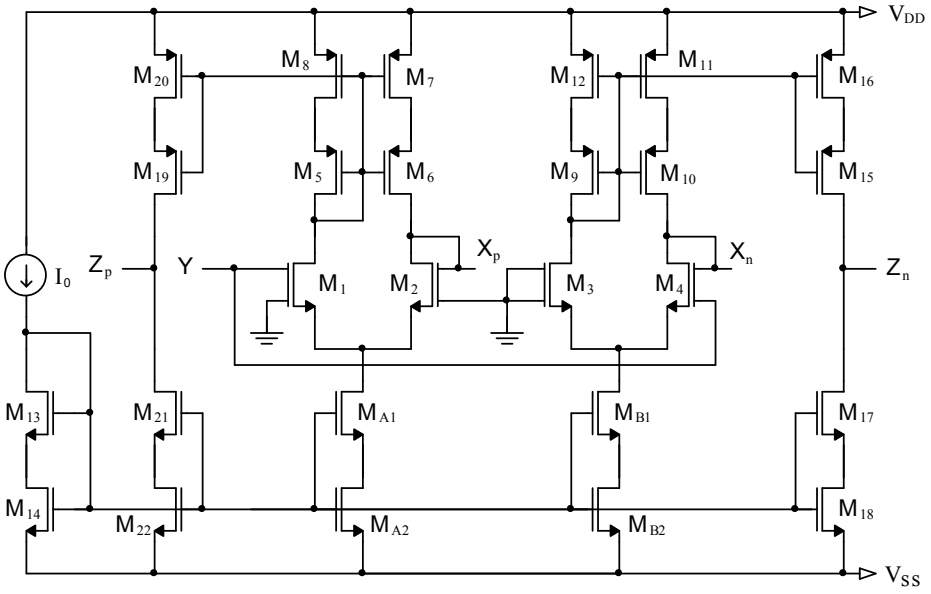

Fig. 3. The circuit structure of the DXCCCII.

From (9), parasitic resistance at terminal X_p of the circuit will be expressed as

$$R_{X_p} \cong \frac{V_{XY_p}}{I_{X_p}} = \frac{2}{\sqrt{I_0 k_n (W/L)}}. \tag{10}$$

As shown in (10), the parasitic resistance of the proposed circuit is easily controlled by biasing current. It is obvious that the electronic adjustability of this resistance is provided by the useful structure. Similarly, the other parasitic resistance at terminal X_n can be described as

$$R_{X_n} \cong \frac{V_{XY_n}}{I_{X_n}} = \frac{2}{\sqrt{I_0 k_n (W/L)}}. \tag{11}$$

In addition, it can be seen that the values of R_{Xp} and R_{Xn} depend on the aspect ratios of M_A and M_B transistors, respectively. If it is desired, each intrinsic resistance value can be changed by the aspect ratio of these transistors or the FGMOS transistors.

The non-ideal model of the DXCCCII is shown in Fig. 4. The real DXCCCII has parasitic resistors and capacitors at the terminal y and z to the ground, and a serial resistor at the terminal x.

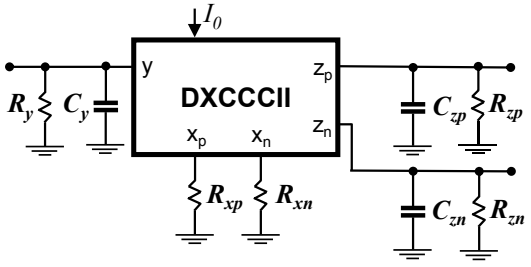

Fig. 4. The non-ideal model of the DXCCCII.

3. Simulation Results

The proposed DXCCCII is simulated using the schematic implementation shown in Fig. 3 with low supply voltages ± 0.75 V. The simulations are based on 0.18 µm level 7 TSMC CMOS process parameters. The dimensions of the transistors used in the DXCCCII implementation are demonstrated in Tab. 1. C_{FG1} and C_{FG2} is selected as 0.02 pF. These capacitances have been known as parasitic capacitances selected for each simulation model of the FGMOS transistor.

Transistor	W/L
$M_1 - M_4$	1.1/0.36
M_{17},M_{18}, M_{21},M_{22},M_{A1},M_{A2},M_{B1},M_{B2}	3.6/0.36
$M_5 - M_{14}$	3.6/0.36
M_{15},M_{16},M_{19},M_{20}	7.2/0.36

Tab. 1. The aspect ratio of the MOS transistors.

Figure 5 shows the changing of the input voltage V_Y versus voltages V_{Xn} and V_{Xp} for the proposed DXCCCII. The curve exhibits a linear characterization approximately between -400 mV and +380 mV. Also, the voltage transfer gain of the DXCCCII is equal to 0.985.

The changing of the input currents I_{Xn} and I_{Xp} versus output current I_Z for the DXCCCII is depicted in Fig. 6. The curve exhibits a highly linear characterization between -60 µA and +60 µA. The current transfer gain of the DXCCCII is equal to 0.99. Considering these findings, this value is highly acceptable and good enough.

Also, the proposed circuit is observed that how the voltage and current ranges depend on the bias current I_0. Voltage and current ranges have been almost decreased as

±200 mV and ±2 μA, respectively. In addition, the voltage and current errors are investigated for the changing biasing current. The findings have proved that voltage and current errors are equal to 0.97 and 0.98, respectively. The changing of I_0 versus R_X has been illustrated in Fig. 7.

Parasitic resistances of the DXCCCII can be approximately tuned between 6.5 kΩ and 400 kΩ by biasing current.

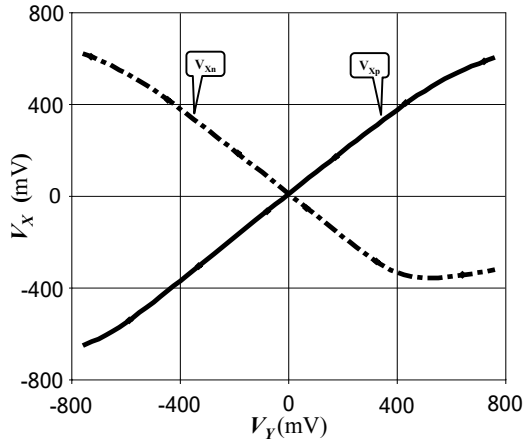

Fig. 5. The voltage transfer curve for the DXCCCII.

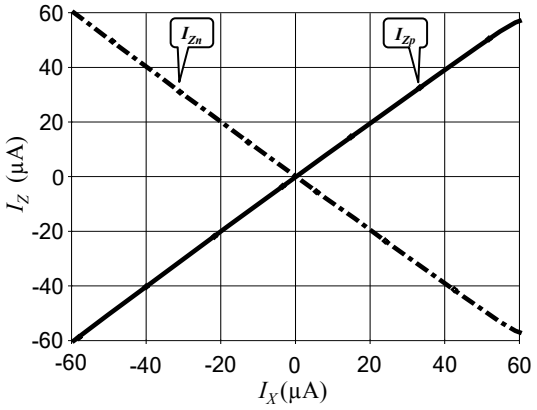

Fig. 6. The current transfer curve for the DXCCCII.

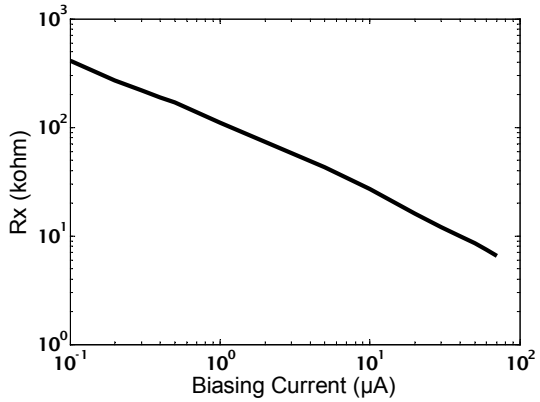

Fig. 7. The parasitic resistance of the proposed DXCCCII for different biasing currents.

The current gains between terminals X and terminals Z are almost 1. The transfer of current is linear from X to Z node. Figure 8 displays the frequency response for the voltage transfer gains and current transfer gains of the DXCCCII. At the same time, Fig. 8 shows the frequency responses of current transfer gains I_{Zp}/I_{Xp}, I_{Zn}/I_{Xn} and voltage gain V_{Xp}/V_Y, the 3 dB cut-off frequencies are 290 MHz, 908 MHz and 265 MHz, respectively. It is investigated that the bandwidth of the voltage and current gains are depended on the bias current. When the biasing

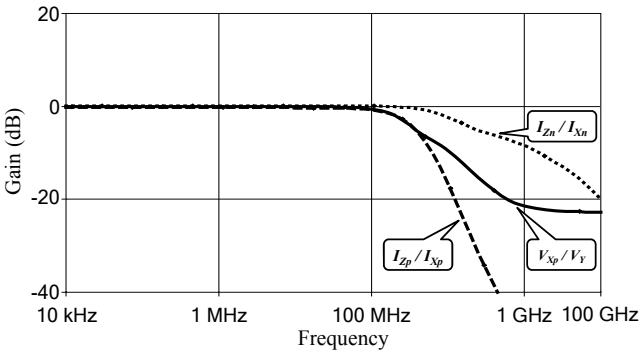

Fig. 8. The frequency response of the voltage transfer gains and current transfer gains of the proposed DXCCCII.

Parameters	DXCCII [14]	DXCCII [16]	Proposed DXCCCII
Supply voltage	±2.5V	±1.5V	±0.75V
Input voltage range	−360 mV, +400mV	−500 mV, +600mV	−400 mV, +380mV
Input voltage / Supply voltage (%)	15,2	36	52
Input current range (I_X)	−60 μA, +60 μA From Fig. 5 in Ref. [16]	−70 μA, +90 μA From Fig. 5 in Ref. [16]	±60μA
Output current range (I_Z)	−90 μA, +110 μA	−100 μA,+125 μA	±60μA
Voltage transfer gain	0.95	0.95	0.985
Current transfer gain	0.97	0.98	0.99
-3 dB bandwidth (I_{Zp}/I_{Xp}, I_{Zn}/I_{Xn})	-	10.35 GHz	290 MHz, 908 MHz
-3 dB bandwidth (V_{Xp}/V_Y, V_{Xn}/V_Y)	580 MHz	1.05 GHz	265 MHz, 350 MHz
R_X (adjustable range) (I_0=0.1μA-70μA)	-	-	400 kΩ-6.5 kΩ
Y input resistance	-	-	10 GΩ
Z output resistance	0.18 GΩ	5.83 GΩ	9.2 GΩ
Parasitic capacitance (C_Y)	-	-	0.02 pF
Parasitic capacitance (C_Z)	-	-	0.017 pF
Power dissipation	-	-	200 μW
Tunability	No	No	Yes
Technology / Number of transistors	0.35 μm CMOS / 20	0.35 μm CMOS / 48	0.18 μm CMOS / 20
* for I_0 = 35 μA			

Tab. 2. The parametric characteristics of the DXCCCII.

current is increased from 0.1 μA to 70 μA, the bandwidth of the voltage and current gains has approximately varied from 8.5 MHz to 800 MHz and 13 MHz to 3 GHz, respectively. As shown in Fig. 3, while terminal X_n is composed of gate and drain of the transistor M_4, terminal Y is connected to the another gate of the transistor M_4. Therefore, taking into consideration Fig. 1, it can be easily seen that frequency performance only depends on the input capacitances C_{FG1} and C_{FG2}, in addition, the frequency behavior of the voltage gain V_{Xn}/V_Y is rather reasonable. Phase difference for gain values below 350 MHz can be accepted zero. Also, the proposed circuit consumes 200 μW for $I_0 = 35$ μA.

The performance parameters of the proposed circuit are depicted in Tab. 2. The proposed circuit offers some advantages. For instance, low-voltage power supply has been required about ±750 mV. Likewise, the circuit which has a simple circuit design consumes power about 200 μW. The main feature of the DXCCCII is that the intrinsic resistance can be usefully tuned in the wide range by biasing current. Also, the output (port Z) and input (port Y) of the DXCCCII has very high resistance and the proposed circuit has reasonable number of transistors. Voltage and current transfer gain of the proposed circuit is more adorable than the other references in Tab. 2

4. Tunable Applications of the DXCCCII

In order to reveal the performance and the usability of the DXCCCII, application examples such as active inductors and tunable oscillator have been introduced using PSpice simulations.

4.1 The Grounded Active Inductor

The proposed circuits for accomplishing grounded inductors are shown in Fig. 9. All of the circuits are constructed with two DXCCCII and one grounded capacitor. It is obviously known that a circuit with grounded capacitors has appreciable advantages in analog integrated circuit implementations.

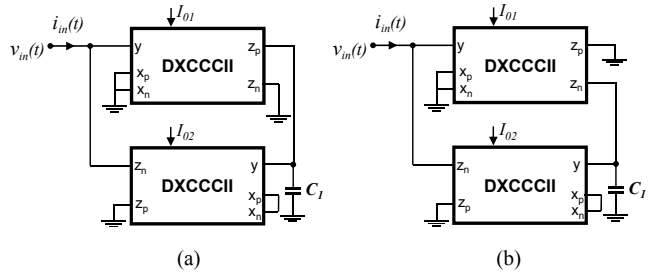

Fig. 9. Inductance simulators realized using DXCCCII: a) positive, b) negative.

The circuits can simulate diverse combinations of the inductances as shown in Fig. 9. These circuits can operate as positive and negative inductances. The previously presented grounded inductance simulators suffer from some disadvantages such as passive component mismatch, use of capacitor that connected in series to the port X of the current conveyor, and eventually operating in lower frequency, use of two or more passive elements [10], [17-20]. Whereas, these drawbacks have partly been overcame by the proposed circuit which has only two grounded capacitors and two DXCCCIIs. The equivalent inductance value of the both positive and negative simulators is given by the following equation

$$L_{eq} \cong \frac{v_{in}}{i_{in}} = \left| R_{X1} R_{X2} C_1 \right| \tag{12}$$

where R_{X1} and R_{X2} are the parasitic resistances of the first and second DXCCCII, respectively. Considering both the voltage and the current tracking errors of the DXCCCII, $\beta_p = 1 - \varepsilon_{Vp}$ and $\beta_n = 1 - \varepsilon_{Vn}$ define the voltage tracking errors from Y terminal to X_p and X_n terminals; $\alpha_p = 1 - \varepsilon_{Ip}$ and $\alpha_n = 1 - \varepsilon_{In}$ define the current tracking errors from X_p and X_n terminals to Z_p and Z_n terminals, respectively. β_p, β_n and α_p, α_n are the voltage and the current transfer gains ; ε_{Vp}, ε_{Vn} and ε_{Ip}, ε_{In} are the voltage and the current transfer errors of the DXCCCII, respectively. Taking into consideration both the voltage and current tracking errors of the DXCCCII, the input current of the inductance simulator as shown in Fig. 9 can be calculated as,

$$i_{in} = \frac{v_{in} \beta_{p1} \alpha_{p1} \alpha_{n2} \left(\beta_{p2} + \beta_{n2} \right)}{sC_1 \left(2R_{X1} R_{X2} \right)} \tag{13}$$

where β_{p1}, β_{n1} and α_{p1}, α_{n1} are the voltage and current transfer gains of the first current conveyor (DXCCCII 1), respectively, and, β_{p2}, β_{n2} and α_{p2}, α_{n2} are the voltage and current transfer gains of the second current conveyor (DXCCCII 2).

Considering tracking errors of the DXCCCII, positive and negative inductance of the simulator can be described respectively as

$$L_{eq}^{+} = \frac{2R_{X1} R_{X2} C_1}{\beta_{p1} \alpha_{p1} \alpha_{n2} \left(\beta_{p2} + \beta_{n2} \right)}, \tag{14.a}$$

$$L_{eq}^{-} = -\frac{2R_{X1} R_{X2} C_1}{\beta_{n1} \alpha_{n1} \alpha_{n2} \left(\beta_{p2} + \beta_{n2} \right)}. \tag{14.b}$$

The frequency response of the impedance value for the inductance simulator is displayed in Fig. 10. The graph is drawn by using different biasing currents. The capacitance value of the C_1 shown in Fig. 9 is equal to 15 pF. When the graph is investigated, it can be seen that the curve exhibits approximately a linear behavior between 100 kHz–7 MHz, 100 kHz–8.5 MHz and 100 kHz–10 MHz for $I_0 = 20$, 30, 40 μA, respectively.

To prove the theoretical validity of the inductance simulator given in Fig. 9, the classical high pass filter shown in Fig. 11 was employed as an application.

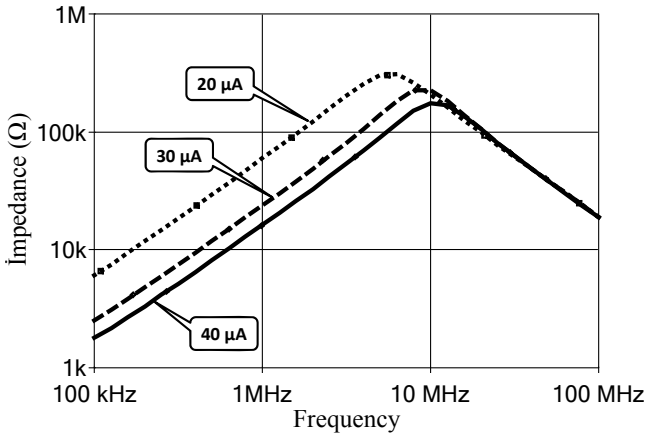

Fig. 10. The impedance values of the simulators for different biasing currents.

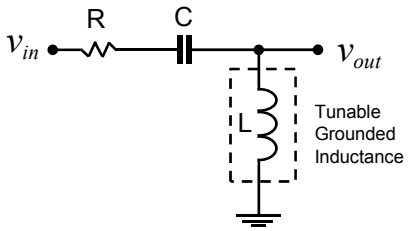

Fig. 11. The classical high pass filter.

Frequency response of the filter is illustrated in Fig. 12. The passive elements are selected as $R = 4$ kΩ, $C = 35$ pF, and $C_1 = 15$ pF, which results in a 3dB frequencies of 267 kHz, 390 kHz, 530 kHz for $I_0 = 20$, 30, 40 µA, respectively. In addition, the 3dB frequencies of the high pass filter is theoretically calculated as 277 kHz, 405 kHz and 569 kHz. The reason of the difference between the calculated and simulated values is the voltage and current tracking errors of the DXCCCII.

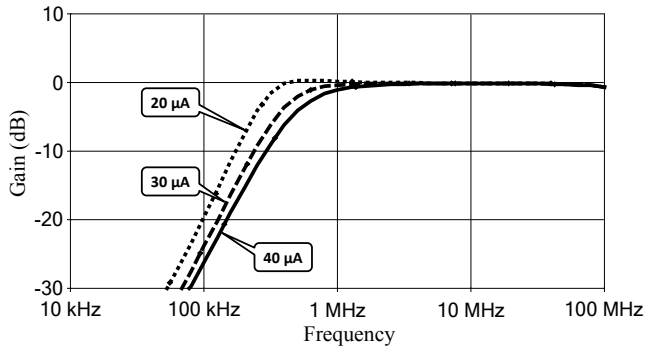

Fig. 12. Frequency responses of the filter.

4.2 Tunable Oscillator

As another application, the tunable oscillator circuit using only two DXCCCII shown in Fig. 13 has been presented. Also, it consists of two grounded capacitors.

Characteristic equation and oscillation frequency of the tunable oscillator shown in Fig. 13 can be obtained

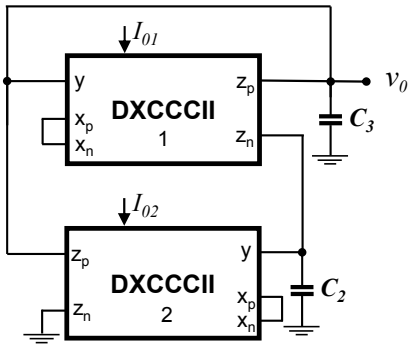

Fig. 13. The tunable oscillator circuit.

doing routine circuit analysis following characteristic equations.

$$s^2 - \frac{1}{R_{X1}C_3}s + \frac{1}{R_{X1}R_{X2}C_2C_3} = 0, \tag{15.a}$$

$$\omega_0 = \frac{1}{\sqrt{R_{X1}R_{X2}C_2C_3}} \tag{15.b}$$

where R_{X1} and R_{X2} are the parasitic resistances of the first and second DXCCCII, respectively. As shown in (15.a), oscillation condition of the oscillator is always provided when the non-ideal effects are ignored. Considering tracking errors of the DXCCCII, characteristic equation and oscillation frequency of the tunable oscillator can be described respectively as

$$s^2 - \frac{\alpha_{p1}(\beta_{p1}+\beta_{n1})}{2R_{X1}C_3}s + \frac{\alpha_{n1}\alpha_{p2}(\beta_{p1}+\beta_{n1})(\beta_{p2}+\beta_{n2})}{4R_{X1}R_{X2}C_2C_3} = 0, \tag{16.a}$$

$$\omega_0 = \sqrt{\frac{\alpha_{n1}\alpha_{p2}(\beta_{p1}+\beta_{n1})(\beta_{p2}+\beta_{n2})}{4R_{X1}R_{X2}C_2C_3}}. \tag{16.b}$$

Oscillation waveform of the oscillator is displayed in Fig. 14. In order to obtain the frequency responses of the oscillator, C_2 and C_3 are set to 1 pF and 3 pF, respectively. The biasing currents for the DXCCCIIs I_{01} and I_{02} are equal to 1 µA and 40 µA, respectively.

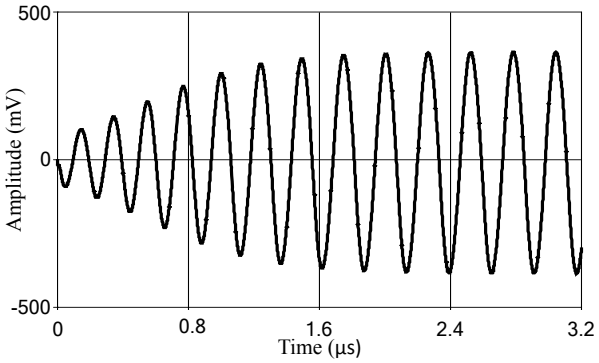

Fig. 14. Voltage waveforms of the oscillator in time domain.

Fig. 15 shows that the calculated results have a good agreement with the simulated results. This figure depicts that the oscillation frequency of the oscillator can be tuned by I_{02}. The oscillation frequency of the oscillator can be varied from 1.83 MHz to 4.79 MHz if the biasing current is tuned from 10 μA to 70 μA.

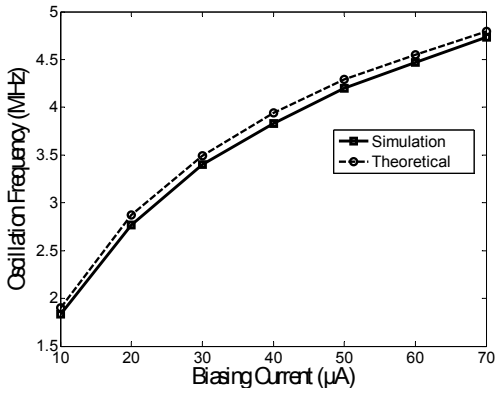

Fig. 15. Oscillation frequency versus biasing current of the second DXCCCII.

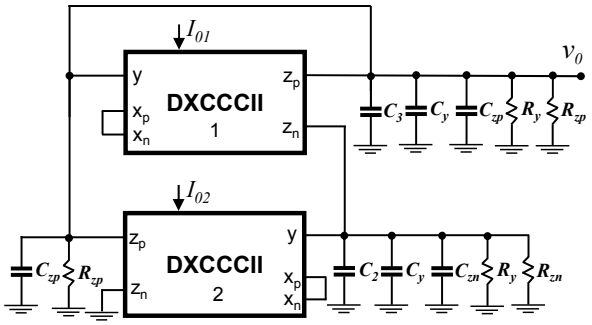

Fig. 16. The non-ideal model of the oscillator.

The non-ideal model of the oscillator is shown in Fig. 16. The real DXCCCII has parasitic resistors and capacitors at the terminal y and z to the ground, and a serial resistor at the terminal x. R_{zp1}, R_{zp2}, R_{zn1}, C_{zp1}, C_{zp2}, C_{zn1} can be defined as the parasitic resistors and capacitors of the z terminals of DXCCII 1 and DXCCII 2 in Fig. 16. R_{y1}, R_{y2}, C_{y1}, C_{y2} are the parasitic resistors and capacitors at the y terminals of DXCCII 1 and DXCCII 2. Because of $C_3 >> C_{y1} + C_{zp1} + C_{zp2}$ and $C_2 >> C_{y2} + C_{zn1}$, the effect of the parasitic capacitances to the total capacitances can be neglected. Considering non-ideal effects of the DXCCCII, oscillation frequency and condition of the tunable oscillator can be expressed respectively as

$$\omega_0 = \sqrt{\frac{1}{R_{X1}R_{X2}C_2C_3} + \frac{1}{R_AR_BC_2C_3} - \frac{1}{R_BR_{X1}R_{X2}C_2C_3}}\,, \quad (17.a)$$

$$\text{CO:}\ \frac{R_AC_3 + R_BC_2}{R_AR_BC_2C_3} - \frac{1}{R_{X1}C_3} \le 0\,. \quad (17.b)$$

where $R_A = R_{y1} // R_{zp1} // R_{zp2}$ and $R_B = R_{y2} // R_{zn1}$. It can be seen that values of the R_A and R_B are approximately GΩs. Thus, the effects of the parasitic resistance to the frequency are highly poor. In (17.b), the condition of oscillation is given as the formulation including non-ideal effects.

Comparison between various oscillators using active element is shown in Tab. 3. Some circuits have no electronical tunability as shown in Tab. 3. Also, the proposed circuit has low power consumption compared to these circuits due to the fact that DXCCCII used in the proposed oscillator has simple structure and low supply voltage. The obvious advantage of the proposed oscillator is using less active and passive elements.

Ref	Supply voltage	Active element	Number of active / passive elements	FO range (MHz)	THD (%)	Technology	Electronical tunability	Power consumption (mW)
21	± 2.5 V	CCCDTA	2 / 2	0.1 – 5	1.14	BJT	Yes	12.1
22	± 5 V	ECCII -, CCII	3 / 5	0.26 – 1.25	0.2 – 1.5	BJT	Yes	N/A
23	± 1.25 V	CDTA	3 / 3	0.4 – 0.8	10	CMOS	Yes	2.87
24	± 1.25 V	DDCC, OTA	2 / 3	1.69	1.75	CMOS	No	1.86
25	± 2 V	OTA	4 / 4	0.2 – 21.5	1	CMOS	Yes	1.52
26	± 1.25 V	DX-MOCCII, MOS	2 / 5	1.59	3.5	CMOS	No	N/A
27	± 2.5 V	DVCC	1 / 5	0.096	3.76	CMOS	No	N/A
28	± 2.5 V	OTA, CDTA	2 / 4	0.053	1.17	CMOS	No	N/A
29	± 1.5 V	MCCCDTA	1 / 6	0.076	0.13	BJT	No	N/A
30	± 5 V	CCII	2 / 2	0.035	3	BJT	No	N/A
Prop.	± 0.75 V	DXCCCII	2 / 2	1.83 – 4.79	2.4 – 4.4	CMOS	Yes	0.28

Tab. 3. Comparison between various oscillators.

4.3 The Grounded and Floating Active Resistors

DXCCCII based grounded positive and negative active resistor structures have been displayed in Fig. 17.

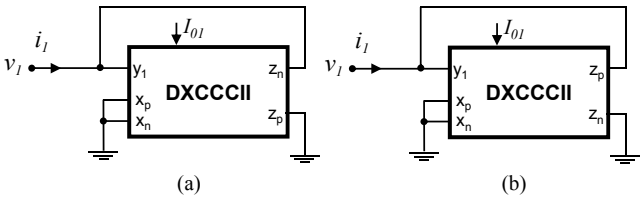

Fig. 17. DXCCCII based grounded resistors a) positive resistor, b) negative resistor.

From (10) and (11), it can be seen that R_{Xn} is equal to R_{Xp}. So, all parasitic resistances can be represented as R_X. The resistance value of the DXCCCII based grounded resistors will be expressed as,

$$R_1 \cong \frac{v_1}{i_1} = \left|R_X\right|. \tag{18}$$

Floating positive and negative active resistor structure based on DXCCCII have been depicted in Fig. 18. This figure demonstrates two types of an active resistor designed by using only two DXCCCIIs. The proposed active resistors might be tuned by the biasing currents. So, the resistance value of the resistors is calculated as,

$$R_{12} = \frac{v_1 - v_2}{i_1} = 2 \cdot \left|R_X\right| \tag{19}$$

where all biasing currents are equal to I_0 and $i_2 = -i_1$.

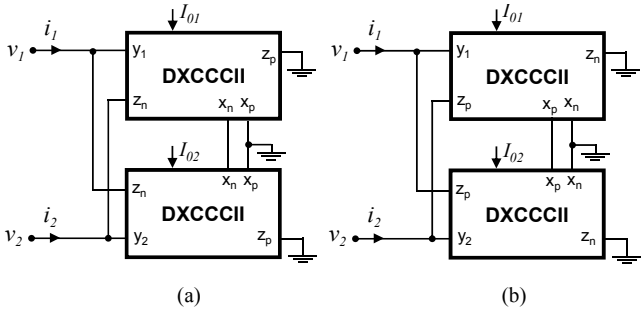

Fig. 18. DXCCCII based floating resistors a) positive resistor, b) negative resistor.

The I-V characteristics of the proposed resistors are shown in Fig. 19. The behaviors of the resistors are fairly linear between -400 mV and +400 mV. Additionally, the estimation of the proposed circuit's dynamic-range is calculated as

$$\left|v_1 - v_2\right| \le 2\left(\frac{I_0}{k_n W / L}\right)^{1/2}. \tag{20}$$

The dynamic range highly depends on the biasing current as shown in (20). Thus, the dynamic range will be expanded for the high values of the biasing current. Considering both the voltage and the current tracking errors of the DXCCCII, the resistance values of the floating active resistors can be calculated as

$$R_{12}^{+} = \frac{v_1 - v_2}{i_1} = 2\alpha_p \beta_p R_X, \tag{21.a}$$

$$R_{12}^{-} = \frac{v_1 - v_2}{i_1} = -2\alpha_n \beta_n R_X. \tag{21.b}$$

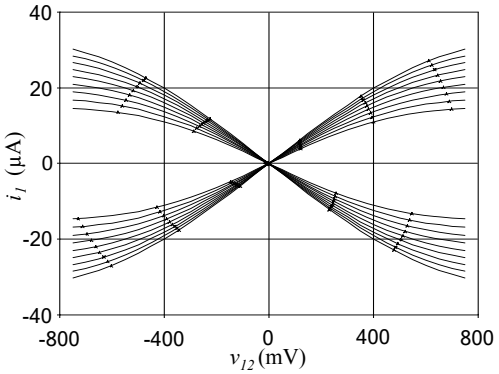

Fig. 19. The I-V characteristics of the floating positive and negative active resistor.

5. Conclusion

In this paper, dual-X controlled current conveyor (DXCCCII) as a versatile active block is presented and its applications to pure inductance simulators has been tested. Also, high pass filter application using DXCCCII based inductance simulator has been simulated to prove the theoretical validity. In addition, DXCCCII based oscillator with flexible tunable oscillation frequency and active resistors are presented as other applications. Only grounded capacitor and DXCCCII have been employed in the all designed applications. The adjustment capability of the proposed circuits is the functional feature in electronic circuit designs. In this context, the proposed circuits are rather convenient for IC realizations. The proposed circuits have been simulated using a PSpice simulation program, and its simulation results were compared with the theoretical approaches and the other DXCCIIs. Theoretical analyses of these circuits were achieved, and the performances of the proposed circuits have been verified by the simulation results. For the proposed DXCCCII, the parasitic resistance value can be tuned from 6.5 kΩ to 400 kΩ if the biasing current is changed from 0.1 μA to 70 μA with a good coherence between the theoretical and simulation results. Besides this good coherence, the proposed circuit is required a low voltage as well as ±0.75 V. As a consequence, we believe that it is absolutely an admirable design because of having low power dissipation.

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About Authors ...

Sezai Alper TEKİN was born in Kayseri, Turkey. He received the B. Engineering degree from Erciyes University, Kayseri, Turkey, in 2000, the M.S. degree from Niğde University, Niğde, Turkey, in 2005 and the Ph.D. in Electrical and Electronics Engineering from Erciyes University, Kayseri, Turkey in 2012. From 2006 to 2012 he was a member of academic staff with the Erciyes University, Engineering Faculty, Electrical and Electronics Dept., Kayseri, Turkey. Since 2012, he has been a member of academic staff with the Erciyes University, Engineering Faculty, Industrial Design Dept., Kayseri, Turkey. His current research interests include free space optics, current mode circuits, current conveyors, electronic circuit design and solar cells.

Hamdi ERCAN received the B. Engineering and M.S. degrees from Erciyes University, Kayseri, Turkey, in 2004

and 2007, respectively, all in Electronic Engineering. He received the Ph.D. in Electrical and Electronics Engineering from Erciyes University, Kayseri, Turkey in 2012. Since 2005, he has been a member of academic staff with the Erciyes University, Civil Aviation School, Avionics Dept., Kayseri, Turkey. His current research interests include current mode circuits, current conveyors and electronic circuit design.

Mustafa ALÇI was born in Kayseri, Turkey, in 1957. He graduated Electronic Dept. of Technology Faculty from Gazi University, Ankara in 1979. Then he received the B. Sc. degree from Erciyes University, Kayseri, in 1983, M. Sc. degree from Middle East Technical University, Ankara, in 1986 and Ph.D. degree from Erciyes University, Kayseri, in 1989, respectively, all in Electrical & Electronics Engineering. Since 1979, he is a member of academic staff with Erciyes University Engineering Faculty, Electronic Engineering Dept., Kayseri, Turkey. His current research interests include image processing, noise and coding artifacts suppression, fuzzy systems, medical electronics, chaotic systems and circuit design.