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Power-Efficient Electronically Tunable Fractional-Order Filter

Sadaf Tasneem [1], Rajeev Kumar Ranjan [1], Sajal K. Paul [1] and Norbert Herencsar [2,*]

[1] Department of Electronics Engineering, Indian Institutes of Technology Dhanbad, Dhanbad 826004, India; sadaf.18dr0119@ece.iitism.ac.in (S.T.); rajeev@iitism.ac.in (R.K.R.); sajal@iitism.ac.in (S.K.P.)
[2] Department of Telecommunications, Brno University of Technology, Technicka 12, 61600 Brno, Czech Republic
* Correspondence: herencsn@ieee.org

Abstract: This article describes a low-voltage, low-power fractional-order low-pass filter (FO-LPF) of order 1 + α, which is implemented using a voltage differencing differential difference amplifier (VDDDA). The VDDDA structure is implemented using the bulk-driven metal oxide semiconductor transistor technique. The transistors operate in the subthreshold region to maintain low-supply voltage and low-power consumption. The FO-LPF structure implemented using this VDDDA structure is compact. It includes three VDDDAs and three grounded capacitors along with two active resistors implemented using MOS transistors. In addition, this filter structure provides electronic tuning of its order and cut-off frequency through the bias current of the active component used. The effects of tracking error and parasitics on the functionality of the proposed FO-LPF were investigated. The VDDDA and filter operate at ±300 mV and dissipate only 207 nW and 663 nW of power, respectively. Thus, the VDDDA structure and filter are suitable for low-voltage and low-power operation. Layouts of the proposed VDDDA as well as the FO-LPF were designed in the Cadence Virtuoso environment. Post-layout simulation results of the designed circuits imply that they are suitable for fabrication. Noise, total harmonic distortion, Monte-Carlo, and PVT analyses were also performed.

Keywords: bulk-driven technique; current-mode; electronically tunable; fractional-order; low-voltage; low-power; low-pass filter

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1. Introduction

The utilization of fractional calculus (FC) is being observed increasingly within the engineering domain due to its ability to provide a more precise representation of natural phenomena and physical entities compared to integer-order (IO) models, making their study and control easier. Fractional-order (FO) systems offer greater design flexibility compared to IO systems. FO systems provide more design adaptability than IO systems. Although the mathematical basics of FC evolved around 200 years ago, this topic remained restricted only to mathematicians until it found its importance in diverse engineering fields, such as material theory, diffusion theory, control theory, bioengineering, circuit theory and design, electromagnetics, and robotics. In the case of circuit theory, fractional-order systems find applications in transmission media, power electronics, multivibrator circuits, integrator–differentiator circuits, chaotic systems, oscillators, resonators, filters, memristive elements, and many more [1–4]. The demand for active filters in diverse fields, including analog signal processing, is experiencing a significant surge. The order of a filter is a significant attribute, which is determined by its slope in the transition band. Order is generally a real number, but while designing a filter using traditional methods, it is rounded off to the nearest integer. Therefore, accurate requirements for frequency response are not achieved. Nevertheless, the FO design methodology enables researchers to have precise control over the various parameters of the filter. IO filters have a slope of $-20 \times$ n dB/decade, where n is a positive integer. Fractional order filters (FOFs), a generalized case of IO filters, have a slope of $-20 \times (n + \alpha)$ dB/decade for an FOF of order $(n + \alpha)$, where n is a positive integer and α is a real number between 0 and 1 [4,5].

The successful implementation of FOFs necessitates the use of fractional-order passive elements (FOEs). These FOEs can be fractional-order capacitors (FOCs) or fractional-order inductors (FOIs). The commercial viability of FOEs has yet to be achieved, despite numerous attempts to manufacture them [3,4]. Because of the above-stated reason, for designing FOFs, integer-order approximations are used. There are two design techniques [3,6]. One approach involves approximation of integer-order capacitors and integer-order inductors by FOCs and FOIs, and thus, a generalized form of conventional filters in the fractional domain is obtained. The approximation mentioned above can be achieved by approximating FOEs by building RL or RC networks [3,4,7]. Using this approach, several structures are present in the literature where operational amplifier (OPAMP) [8,9], second-generation current conveyor (CCII) [10], operational transconductance amplifier (OTA) [11], and differential voltage current conveyor (DVCC) [12,13] are used as active elements. Nevertheless, the utilization of this approximation to create FOFs is accompanied by the disadvantage of incorporating floating resistors and capacitors during the implementation of FOEs [4,7]. Additionally, the obtained filter does not provide tuning of its order. The second approach is to approximate properly the transfer function (TF) of FOFs through a suitable integer-order approximation. To implement this technique, the Laplacian variable $(\tau s)^{\alpha}$, is approximated using continued fraction expansion (CFE), a commonly used approximation technique. Several filter structures that use this approach are available in the literature. These implementations are achieved by utilizing OPAMP [14], current feedback operational amplifier (CFOA) [15,16], OTA, current follower (CF), and adjustable current amplifier (ACA) [17,18], differential difference current conveyor (DDCC) [19], current differencing buffered amplifier (CDBA) [20], and universal voltage conveyor (UVC) [21] as their active building blocks.

The voltage differencing differential difference amplifier (VDDDA) block, first described in [22], is a truly versatile analog building block that has a combined feature of OTA and differential difference amplifier (DDA). Therefore, the VDDDA block proves to be advantageous in situations where the tuning of filter parameters and summing of voltages are required simultaneously, as it makes the design compact. A literature survey of VDDDA-based filters reveals several available structures, such as multifunction filters [23], universal filters [24,25], or all-pass filters [22]. Out of all these filters, only [25] presents VDDDA based on the LV-LP technique, and it is also observed that until now, VDDDA has not been employed for the implementation of FOF.

Among the existing works, only [19] provides a filter structure that is capable of operating at low-voltage supply (LV) and low-power consumption (LP), because the DDCC structure is implemented using the bulk-driven quasi-floating gate (BD-QFG) technique. Generally, fractional-order filters are meant to be utilized in the processing of biological signals. Therefore, the utilization of the LV-LP technique would yield significant advantages in the implementation of such filters. The bulk-driven (BD) technique is considered a viable strategy for operating analog circuit designs in LV-LP conditions. This technique eliminates the barrier posed by the threshold voltage in the signal path. However, BD MOSFET offers bulk transconductance, which is three to five times lower than that of gate-driven MOSFET. This low transconductance value of the BD MOSFET leads to a lower intrinsic voltage gain and a reduced bandwidth for the resulting circuit. However, these limitations can be leveraged as a desirable characteristic for applications such as biomedical, as biological signals typically exhibit a frequency range of 0.05 to 10 kHz and amplitude levels ranging from 0.015 to 5 mV, and also because their prime requirements are low-voltage operation and lower power consumption. Operating BD MOSFET in the subthreshold region seems to be a great option to attain low power and low-frequency operation in electronic gadgets.

A fractional-order low-pass filter (FO-LPF) is often used in the detection of sleep apnea syndrome [26]. Due to sleep apnea, there is a prolongation of cardiac inter-beat intervals. These prolongations are detected by applying the energy signal obtained from an electrocardiogram (ECG) to an FO-LPF. In the realm of wearable biomedical systems, the utilization of low-power systems becomes imperative due to the critical significance of minimizing dissipation power. For instance, in an electrocardiogram (ECG) acquisition system, a low-pass filter (LPF) is employed to eliminate noise [27,28].

The aforementioned studies show that only a few structures of FOF are available for its operation in the LV-LP domain and that the mentioned benefits of VDDDA have not been explored in designing FOF. Therefore, this study presents the implementation of the proposed VDDDA using bulk-driven MOSFETs and operated in the subthreshold region. The CMOS structure has a power supply range of ±300 mV and power dissipation of 207 nW, rendering it well-suited for applications that require low voltage and low-power consumption. Subsequently, the FOF structure is implemented using the proposed VDDDA. The CFE method is employed as an approximation technique for the fractional operator, and the resulting circuit is realized using IFLF topology. The proposed FOF structure utilizes a minimal configuration consisting of three VDDDAs, six MOS transistors, and three grounded capacitors. The filter circuit operates with a power supply of only ±300 mV and has a power consumption of 663 nW. These values are the least among the compared literature studies. Additionally, the filter also offers electronic and independent tuning of its order and pole frequency. The remainder of the article is organized as follows. Section 2 analyzes VDDDA behavior, its proposed structure using the LV-LP technique, and simulation results. Section 3 presents the proposed VDDDA-based fractional order low-pass filter, its non-ideality analysis, and simulation results. A comparison of the proposed filter with the FOFs available in the literature is given in Section 4, followed by conclusions in Section 5.

2. Voltage Differencing Differential Difference Amplifier: VDDDA

2.1. Proposed VDDDA

A VDDDA is the active building block (ABB) that provides the advantages of both OTA as well as the differential difference amplifier (DDA). Figure 1a,b, shows the circuit symbol and behavioral model of VDDDA, respectively. VDDDA is a six-terminal block. Out of six terminals, there are four high-impedance voltage input terminals, V_+, V_-, n, and p, a high-impedance auxiliary current output terminal z, and a low-impedance voltage output terminal w. The terminal relationships for an ideal VDDDA are characterized as follows [22]:

$$I_z = g_m(V_{V+} - V_{V-}),\ V_w = V_z - V_n + V_p, \tag{1}$$

In (1), g_m represents transconductance, and its relationship with bias current (I_b) is given as $g_m = I_b/(\eta V_t)$. Here, $V_t = KT/q$ is the thermal voltage and η is the subthreshold slope parameter which is a technology-dependent constant.

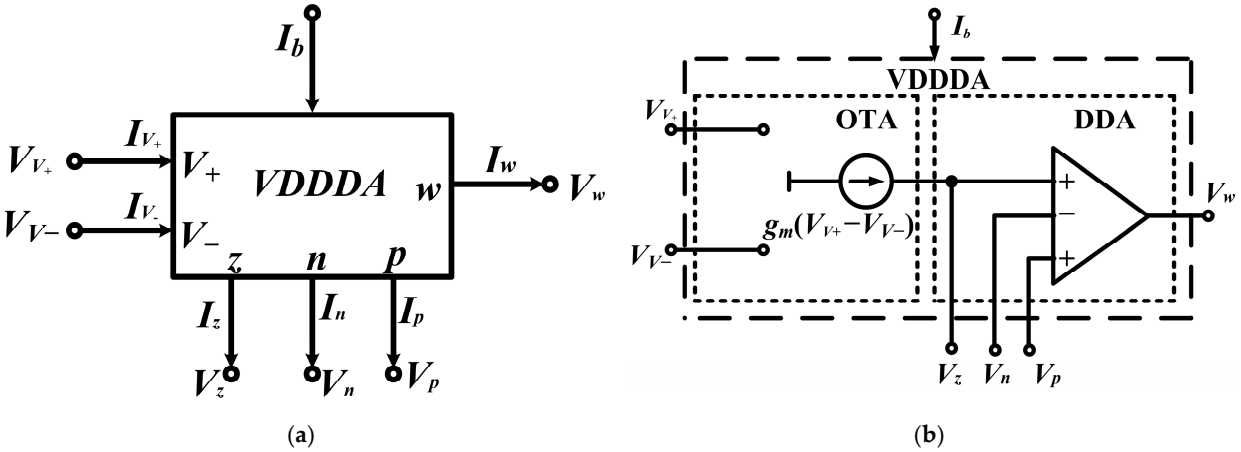


Figure 1. VDDDA: (**a**) symbol; (**b**) behavioral model.

The CMOS structure for the proposed BD-VDDDA capable of operating at low voltage is shown in Figure 2. The first stage is the OTA stage, composed of MOSFETs M_1–$M_{10,}$ where MOSFETs M_1 and M_2 are the bulk-driven PMOS input transistors, and MOSFETs M_7 and M_8 act as an active load. MOSFETs M_5, $M_{10,}$ and M_4, M_9 act as a current mirror to obtain the output current and its copy at the z_c terminal, respectively. For MOSFETs M_1 and M_2, input is applied at the bulk terminal, and the gate terminal is biased using a constant voltage source,

V_G. The second stage is the differential-difference stage comprising MOSFETs M_{11}–M_{19}. The two differential stages at the output are implemented using bulk-driven PMOS transistors M_{15}–M_{16} and M_{17}–M_{18}. The output terminal, i.e., the drain of MOSFET M_{19}, is shorted to the bulk terminals of MOSFETs M_{19} and M_{18} to create a negative feedback loop to improve the accuracy of the gain of the resulting voltage follower. The optimal aspect ratio of the MOSFETs used for the CMOS implementation of VDDDA is mentioned in Table 1. A detailed analysis of structure presented in Figure 2 is available in Appendix A.

Table 1. Aspect ratio of transistors of VDDDA.

Transistor	W (μm)/L (μm)
M_1, M_2	12/0.6
M_3–M_5, M_{b1}, M_{b2}, M_{dc1}, M_{dc2}	10/0.6
M_6, M_9, M_{10}	7/0.6
M_7, M_8	4/0.6
M_{11}–M_{14}	4/0.3
M_{15}–M_{18}	10/0.3
M_{19}	20/0.3

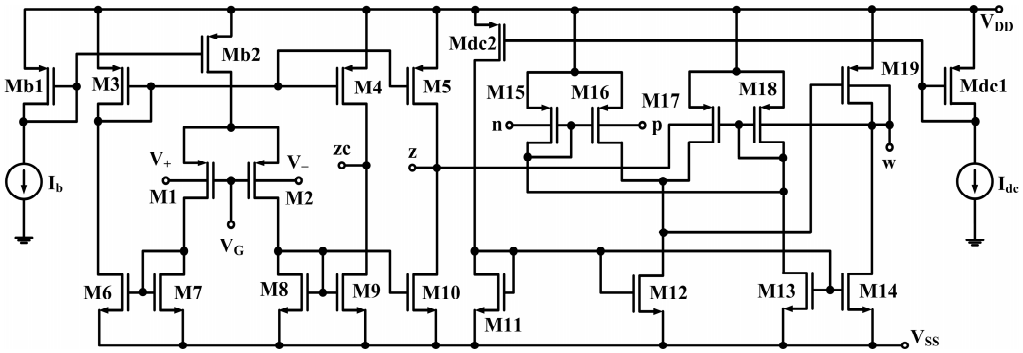


Figure 2. CMOS structure of proposed VDDDA.

2.2. Simulation Results of VDDDA

The bulk-driven CMOS circuit of LV-LP VDDDA operating in the subthreshold region, as shown in Figure 2, is simulated in the Cadence Virtuoso design tool using a 0.18 μm TSMC process parameter with supply voltages, $V_{DD} = -V_{SS} = 300$ mV and $V_G = -300$ mV. The bias currents I_b and I_{dc} are set to 14 nA and 55 nA, respectively. All the MOS transistors are operated in the subthreshold region, to derive the complete circuit at the lowest possible supply voltage for obtaining low power consumption. The proposed layout of the BD VDDDA circuit covers an overall area of 1208 μm^2 (43.8 μm × 27.6 μm) and is shown in Figure 3.

DC and AC analyses were carried out to verify the performance of VDDDA, and the corresponding simulation results are plotted in Figures 4 and 5. From the DC analysis, shown in Figure 4a,b, it can be concluded that the maximum values of terminal voltages without producing significant distortion are up to ±200 mV for the OTA and −240 mV to +200 mV for the DDA, respectively. From the AC analysis shown in Figure 5a, showing pre-layout and post-layout results, it can be observed that the value of g_m at a bias current (I_b) of 14 nA is approximately 200 nA/V. It can be seen that the pre-layout and post-layout results differ slightly from each other due to the impact of parasitic. Figure 5b shows the frequency response of the DDA. The value of gains at low frequency and −3 dB frequency for V_w/V_z, V_w/V_n, and V_w/V_p are found to be −9.1 mdB, 30 mdB, −718 mdB and 158 kHz, 141 kHz, 158 kHz, respectively. The power consumption of the BD-VDDDA circuit is observed to be 207 nW. Hence, a low power consumption value makes this circuit appropriate for low-power applications. The output noise of VDDDA is shown in Figure 6. It is 202 nV/$\sqrt{}$Hz and 282 nV/$\sqrt{}$Hz at 10 Hz for pre-layout and post-layout and after that, it follows an exponential decay and decreases to a value of 21.5 nV/$\sqrt{}$Hz and 30.9 nV/$\sqrt{}$Hz at 1 kHz for pre-layout and post-layout.

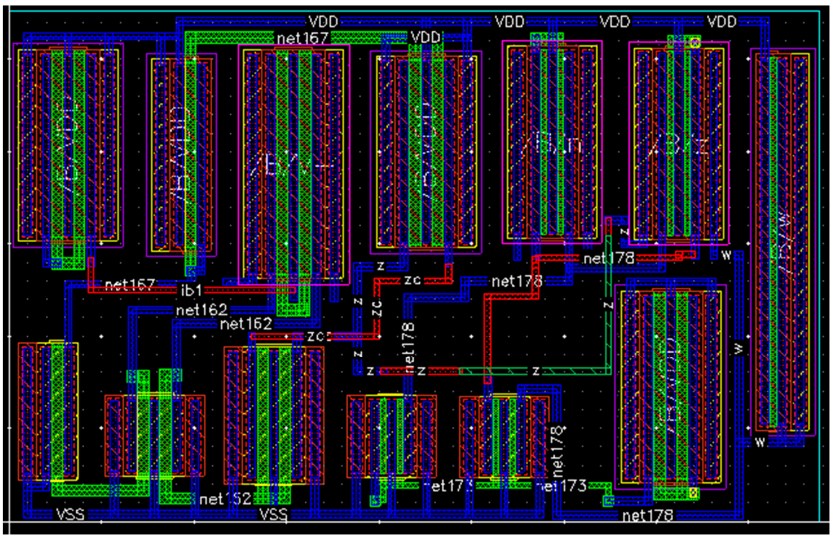
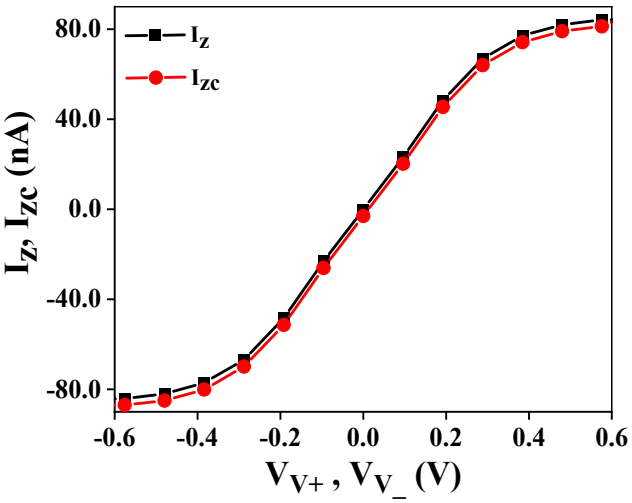
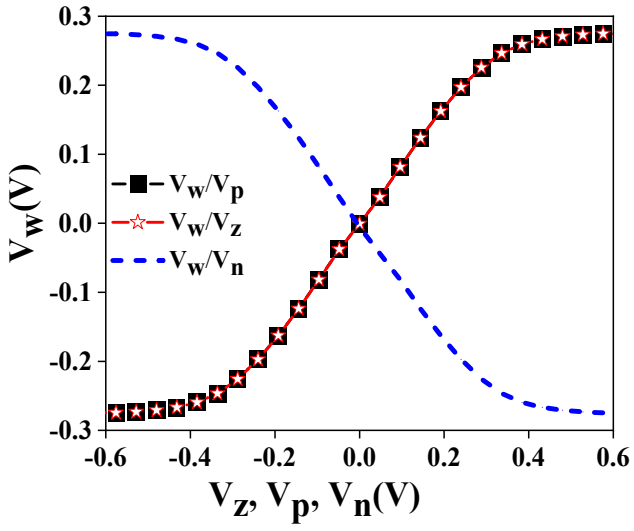


Figure 3. Layout of BD-VDDDA.



(**a**)



(**b**)

Figure 4. DC analysis: (**a**) OTA section; (**b**) DDA section.

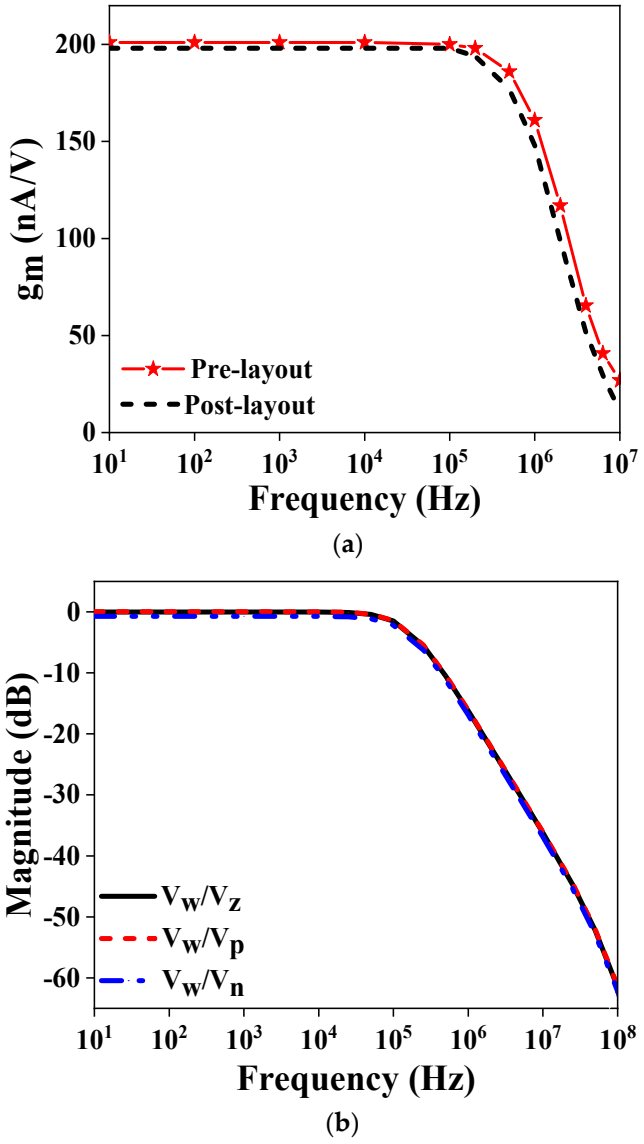


Figure 5. AC analysis: (**a**) OTA section; (**b**) DDA section.

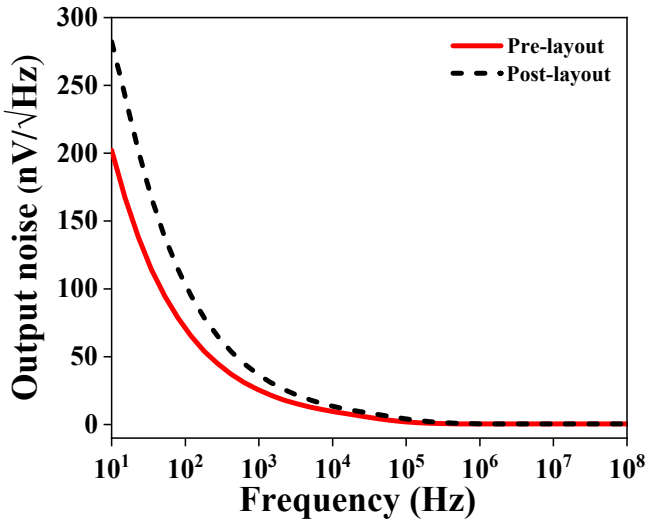


Figure 6. Output noise of VDDDA.

Another compact structure of VDDDA suitable for low-voltage applications was presented in [25]. When the proposed VDDDA was compared with the existing structure, we found that in the existing structure, 17 multiple-input gate-driven MOSFETs are being used in contrast to 19 bulk-driven MOSFETs in the proposed structure. Although the transistor count is low in the existing structure, multiple-input gate-driven MOSFETs are being used which will automatically increase the chip area and thus power dissipation as the multiple-input gate-driven MOSFETs require capacitors at their inputs. Also, the existing circuit uses a power supply of ±900 mV and the power dissipation is 0.99 mW in contrast to ±300 mV and 207 nW for the power supply and power dissipation, respectively, of the proposed circuit. So, in the context of the CMOS structure, the proposed VDDDA is a novel solution and is suitable for low-voltage and low-power applications.

3. Fractional-Order Low-Pass Filter (FO-LPF)

3.1. Basics of FO-LPF of Order 1 + α

The Laplacian operator, s^{α}, is used to design fractional-order filters. An easy way to use s^{α} is to use a fractance element, but despite various efforts, most of them are now still in their development stage [29,30]. Because fractance devices are commercially unavailable, physical realizations of these filters are not possible. Neverthless, using continued fraction expansions (CFEs), the obtained second-order approximation for the Laplacian operator is given below:

$$(\tau s)^{\alpha} = \frac{(\alpha^2+3\alpha+2)\tau^2 s^2 + (8-2\alpha^2)\tau s + (\alpha^2-3\alpha+2)}{(\alpha^2-3\alpha+2)\tau^2 s^2 + (8-2\alpha^2)\tau s + (\alpha^2+3\alpha+2)}. \tag{2}$$

The TF of a FO-LPF of order 1 + α, where (0 < α < 1), with Butterworth characteristics and cut-off frequency $\omega_0 = 1/\tau$, is given below:

$$H_{1+\alpha}^{LP}(s) = \frac{K_1}{(\tau s)^{1+\alpha} + K_3(\tau s)^{\alpha} + K_2}. \tag{3}$$

Here, K_1, K_2, and K_3 are constants whose values are obtained through an algorithm to achieve the required filter characteristics. Using (2), the TF of the IO low-pass filter is given by the following:

$$H_{1+\alpha}^{LP}(s) \cong \frac{a_2 s^2 + a_1 s + a_0}{s^3 + b_2 s^2 + b_1 s + b_0}. \tag{4}$$

The values of coefficients a_i (i = 0, 1, 2) and b_i (i = 0, 1, 2) in (4) are given as follows:

$$a_2 = \frac{1}{\tau}\left(\frac{\alpha^2-3\alpha+2}{\alpha^2+3\alpha+2}\right)K_1, \tag{5}$$

$$a_1 = \frac{1}{\tau^2}\left(\frac{8-2\alpha^2}{\alpha^2+3\alpha+2}\right)K_1, \tag{6}$$

$$a_0 = \frac{1}{\tau^3}K_1. \tag{7}$$

$$b_2 = \frac{1}{\tau}\left(\frac{(K_2+K_3-2)\alpha^2 - 3(K_2-K_3)\alpha + (8+2K_2+2K_3)}{\alpha^2+3\alpha+2}\right), \tag{8}$$

$$b_1 = \frac{1}{\tau^2}\left(\frac{(1-2K_2-2K_3)\alpha^2 - 3\alpha + (2+8K_2+8K_3)}{\alpha^2+3\alpha+2}\right), \tag{9}$$

$$b_0 = \frac{1}{\tau^3}\left(\frac{(K_2+K_3)\alpha^2 - 3(K_2-K_3)\alpha + 2(K_2+K_3)}{\alpha^2+3\alpha+2}\right). \tag{10}$$

For the filter to have Butterworth characteristics, constants K_1, K_2, and K_3 were derived by the computation of the cumulative error, and particularly, the values that resulted in the smallest cumulative band-pass error were utilized in [31]. K_1, K_2, and K_3 are given by the following expressions:

$$K_1 = 1, \tag{11}$$

$$K_2 = 0.2937\alpha + 0.71216, \tag{12}$$

$$K_3 = 1.068\alpha^2 + 0.161\alpha + 0.3324. \tag{13}$$

The functional block diagram (FBD) of inverse follow-the-leader feedback (IFLF) is depicted in Figure 7. It is used to realize the IO TF of (4) [3]. Analysis of this block diagram yields the following TF:

$$\frac{V_{out}}{V_{in}} = \frac{s^2\frac{A_2}{\tau_2} + s\frac{A_1}{\tau_2\tau_1} + \frac{1}{\tau_2\tau_1\tau_0}}{s^3 + s^2\frac{1}{\tau_2} + s\frac{1}{\tau_2\tau_1} + \frac{1}{\tau_2\tau_1\tau_0}}. \tag{14}$$

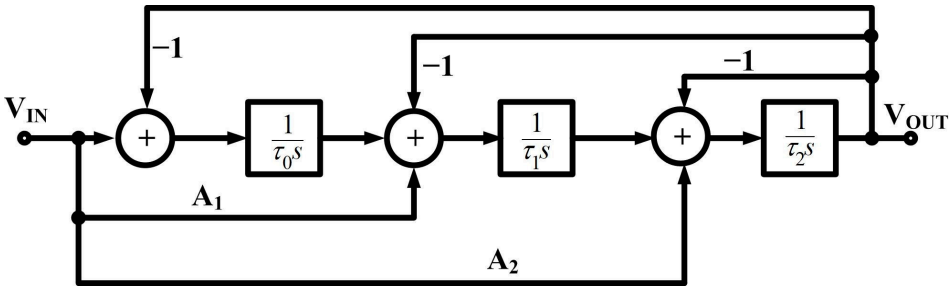


Figure 7. FBD IFLF [3].

The values of forward gain (A_1, A_2), and time constants (τ_0, τ_1, and τ_2) could be computed by equating the respective coefficients in (4) and (14) while using the expressions in (5)–(13).

3.2. Proposed FO-LPF Using LV-LP VDDDA

In this sub-section, the FO-LPF of order (1 + α) is implemented using the proposed BD-VDDDA. The FBD shown in Figure 7 is implemented using VDDDA as ABB. The filter implementation is shown in Figure 8. At the z-terminal of VDDDA$_1$, an input voltage V_{in} is applied, while a scaled version of V_{in} is applied to the z-terminal of VDDDA$_2$ and VDDDA$_3$. These connections allow for the implementation of the forward path with gain. The output node is connected to the n-terminal of each VDDDA, implementing the feedback path. The p-terminal of VDDDA$_1$ is connected to the ground, while the remaining p-terminals receive the signals that have been integrated by the preceding block. The integrators used in the FBD are implemented using VDDDA$_1$–VDDDA$_3$ along with capacitors C_1 to C_3. The forward paths with gains A_1 and A_2 are implemented using PMOS common gate amplifiers M_{a1} and $M_{b1,}$ where $A_1 = g_{ma}R_A$ and $A_2 = g_{mb}R_B$. Here g_{ma} and g_{mb} are the transconductances of transistors M_{a1} and M_{b1}, respectively, and R_A and R_B are the resistances connected at the output node of M_a and M_b, respectively. In Figure 8, the implementation using transistors M_{R1}–M_{R2} and M_{R3}–M_{R4} represents an active resistor R_A and R_B, which provides a resistance value controllable through external voltages V_{g2} and V_{g3}, respectively. Thus, this implementation provides a variable resistor whose value can be adjusted according to the required forward gain by changing the external voltages. The benefit of using active resistors in place of the physical resistor is that it reduces the chip area. Transistors M_{R1}–M_{R4} are operated in the triode region, therefore the obtained grounded resistance value can be expressed as $R_A = \frac{1}{k_n(V_{g2}-2V_{tn})}$ and $R_B = \frac{1}{k_n(V_{g3}-2V_{tn})}$ where $k_n = \mu_n C_{ox}\left(\frac{W}{L}\right)$, V_{g2} and V_{g3} are the externally applied voltages, and V_{tn} is the threshold voltage of the NMOS transistor. The TF of the FO-LPF depicted in Figure 8 is

given by (9). Various parameters, such as the capacitances and transconductances values of the filter, can be calculated by equating respective coefficients in (4) and (15) along with using (5)–(13).

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{s^2 g_{m3} A_2}{C_3} + \frac{s g_{m2} g_{m3} A_1}{C_2 C_3} + \frac{g_{m1} g_{m2} g_{m3}}{C_1 C_2 C_3}}{s^3 + \frac{s^2 g_{m3}}{C_3} + \frac{s g_{m2} g_{m3}}{C_2 C_3} + \frac{g_{m1} g_{m2} g_{m3}}{C_1 C_2 C_3}}. \tag{15}$$

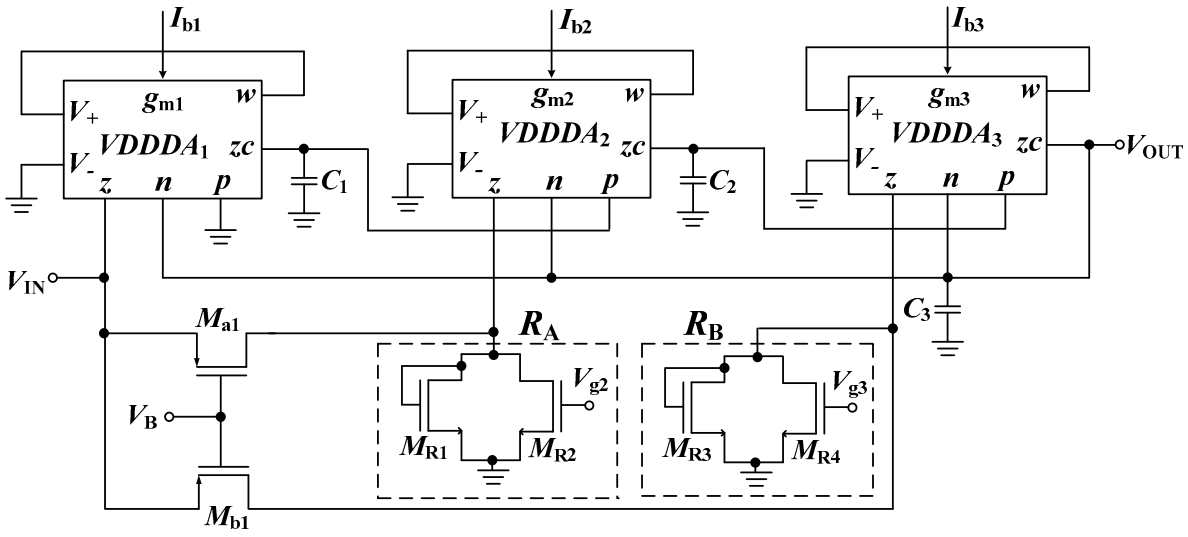


Figure 8. Proposed FO-LPF using VDDDA.

3.3. Effect of Non-Idealities on FO-LPF

In this subsection, the non-ideality effect of VDDDA on the presented FO-LPF is studied. Here, two types of non-idealities are covered, i.e., non-ideality due to tracking error and parasitic. Terminal relationships in (1) are valid for the ideal VDDDA. While considering non-idealities in VDDDA, its characteristics are as follows:

$$I_Z = g_m(\alpha_p V_{V+} - \alpha_n V_{V-}), V_w = \beta_z V_z - \beta_n V_n + \beta_p V_p. \tag{16}$$

where α_p and α_n are tracking errors in transconductance from V_+ and V_- terminals to z terminal, respectively, β_z, β_n, and β_p, are the errors in the respective voltage gain from z, n, and p terminals, respectively to the w terminal of VDDDA. Ideally, tracking errors α_i and β_i are considered to be unity. Taking into account the above-mentioned errors, the voltage at the zc terminal of 1st VDDDA will be as follows:

$$V_{ZC1} = \frac{\alpha_{p1} g_{m1} (\beta_{Z1} V_{in} - \beta_{n1} V_{out})}{sC_1} \tag{17}$$

Similarly, the voltage at the zc terminal of 2nd VDDDA is found to be as below:

$$V_{ZC2} = \frac{\alpha_{p2} g_{m2}}{sC_2} \left[V_{in} \left(\frac{\alpha_{p1} \beta_{Z1} \beta_{p2} g_{m1}}{sC_1} + \beta_{Z2} \mathrm{A}_1 \right) - V_{out} \left(\frac{\alpha_{p1} \beta_{n1} \beta_{p2} g_{m1}}{sC_1} + \beta_{n2} \right) \right] \tag{18}$$

The voltage at the w terminal of 3rd VDDDA is realized as the following:

$$\begin{aligned} V_{w3} = \Bigg[& V_{in} \left(\frac{\alpha_{p1} \alpha_{p2} \beta_{Z1} \beta_{p2} \beta_{p3} g_{m1} g_{m2}}{s^2 C_1 C_2} + \frac{\alpha_{p2} g_{m2} \beta_{p3} \beta_{Z2} \mathrm{A}_1}{sC_2} + \beta_{Z3} \mathrm{A}_2 \right) \\ & - V_{out} \left(\frac{\alpha_{p1} \alpha_{p2} \beta_{n1} \beta_{p2} \beta_{p3} g_{m1} g_{m2}}{s^2 C_1 C_2} + \frac{\alpha_{p2} \beta_{n2} \beta_{p3} g_{m2}}{sC_2} + \beta_{n3} \right) \Bigg] \end{aligned} \tag{19}$$

V_{out}, which is the voltage developed at the *zc* terminal of 3rd VDDDA will be as follows:

$$V_{out} = \frac{\alpha_{p3} g_{m3} V_{w3}}{sC_3} \tag{20}$$

After putting the value of V_{w3} in (20) and solving the equation, the TF of the filter under the parasitic effect is given by the following:

$$\frac{V_{OUT}}{V_{IN}} = \frac{s^2\beta_{z3}X_1A_2 + s\beta_{z2}X_1Y_1A_1 + \beta_{z1}X_1Y_1Z_1}{s^3 + s^2\beta_{n3}X_1 + s\beta_{n2}X_1Y_1 + \beta_{n1}X_1Y_1Z_1}. \tag{21}$$

where, α_{pi}, β_{zi}, β_{pi} and β_{ni} (i = 1, 2, 3) are the errors of the i^{th} block, $X_1 = \frac{\alpha_{p3} g_{m3}}{C_3}$, $Y_1 = \frac{\alpha_{p2}\beta_{p3} g_{m2}}{C_2}$ and $Z_1 = \frac{\alpha_{p1}\beta_{p2} g_{m1}}{C_1}$. Transconductance error between V_+ and z terminal and voltage gain errors between z, n, p to w terminal will affect the magnitude and phase response of the filter. The shift in pole frequency and slope value in the transition band will also be observed.

Considering the effect of parasitic impedances of VDDDA, the corresponding circuit is presented in Figure 9. The high impedance terminals V_+, V_-, n, p, and z of VDDDA exhibit parasitic impedance in the form of shunt-connected resistances and capacitances, and at w terminal, a series resistance (R_w) is present. When considering these parasitic impedances, $C_{T1} = C_1 \| C_{ZC1} \| C_{p2}$, $C_{T2} = C_2 \| C_{ZC2} \| C_{p3}$, $C_{T3} = C_3 \| C_{ZC3} \| C_{n3} \| C_{n2} \| C_{n1}$, $G_1 = G_{ZC1} + G_{p2}$, $G_2 = G_{ZC2} + G_{p3}$, $G_3 = G_{ZC3} + G_{n1} + G_{n2} + G_{n3}$, $G_{ZC1} = \frac{1}{R_{ZC1}}$, $G_{Z2} = \frac{1}{R_{ZC2}}$, $G_{p2} = \frac{1}{R_{p2}}$, $G_{p3} = \frac{1}{R_{p3}}$, $G_{n1} = \frac{1}{R_{n1}}$, $G_{n2} = \frac{1}{R_{n2}}$, and $G_{n3} = \frac{1}{R_{n3}}$. Also, assuming $A_2^* = \frac{g_{mB}}{Z_B}$ and $A_1^* = \frac{g_{mA}}{Z_A}$ where $Z_B = G_B + G_{Z2}$, $Z_A = G_A + G_{Z3}$, $G_B = \frac{1}{R_B}$, $G_A = \frac{1}{R_A}$, $G_{Z2} = \frac{1}{R_{Z2}}$ and $G_{Z3} = \frac{1}{R_{Z3}}$. After analyzing the circuit, the voltage at the *zc* terminal of 1st VDDDA will be as follows:

$$V_{ZC1} = \frac{g_{m1}(V_{in} - V_{out})}{sC_{T1} + G_1} \tag{22}$$

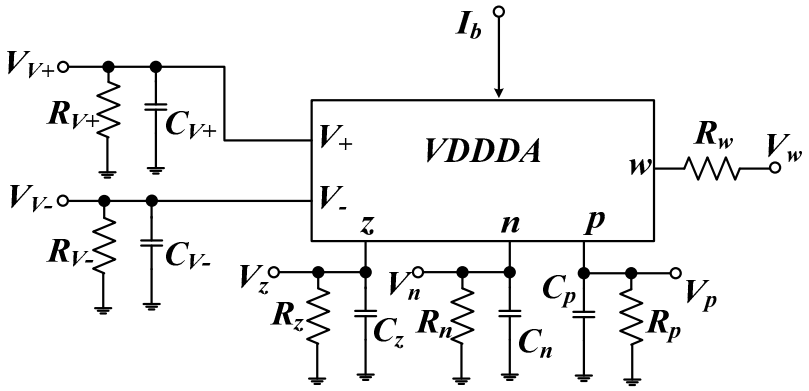


Figure 9. VDDDA model considering parasitic impedances.

Similarly, the voltage at the *zc* terminal of 2nd VDDDA is found to be as below:

$$V_{ZC2} = \frac{g_{m2}}{sC_{T2} + G_2}\left[V_{in}\left(\frac{g_{m1}}{sC_{T1} + G_1} + A_1^*\right) - V_{out}\left(\frac{g_{m1}}{sC_{T1} + G_1} + 1\right)\right] \tag{23}$$

The voltage at the w terminal of 3rd VDDDA is realized as below:

$$\begin{aligned} V_{w3} = \Bigg[& V_{in}\left(\frac{g_{m1}g_{m2}}{(sC_{T1}+G_1)(sC_{T2}+G_2)} + \frac{A_1^* g_{m2}}{(sC_{T2}+G_2)} + A_2^*\right) \\ & - V_{out}\left(\frac{g_{m1}g_{m2}}{(sC_{T1}+G_1)(sC_{T2}+G_2)} + \frac{g_{m2}}{(sC_{T2}+G_2)} + 1\right)\Bigg] \end{aligned} \tag{24}$$

V_{out}, which is the voltage developed at the *zc* terminal of 3rd VDDDA will be the following:

$$V_{out} = \frac{g_{m3}V_{w3}}{sC_{T3} + G_3} \tag{25}$$

After putting the value of V_{w3} in (25) and solving the equation, the TF of the filter under the parasitic effect is given by the following:

$$\frac{V_{OUT}}{V_{IN}} = \frac{s^2AA_2^* + s\left(ABA_1^* + ACA_2^* + ADA_2^*\right) + \left(G_MC_T + ABCA_1^* + ACDA_2^*\right)}{s^3 + s^2\begin{pmatrix}A + C+\\ D + E\end{pmatrix} + s\begin{pmatrix}AB + AC + AD\\ +CD + CE + DE\end{pmatrix} + \begin{pmatrix}G_MC_T + ABC\\ +ACD + CDE\end{pmatrix}}, \tag{26}$$

where $A = \frac{g_{m3}}{C_{T3}}$, $B = \frac{g_{m2}}{C_{T2}}$, $C = \frac{G_1}{C_{T1}}$, $D = \frac{G_2}{C_{T2}}$, $E = \frac{G_3}{C_{T3}}$, $G_M = g_{m1}g_{m2}g_{m3}$, and $C_T = \frac{1}{C_{T1}C_{T2}C_{T3}}$. When considering the parasitic model of VDDDA in the proposed filter, parasitic capacitances and resistances present at the terminals where a passive element is connected should be considered and may affect the magnitude and phase response of the filter at high frequency. These parasitics will also cause a shift in pole frequency and slightly change the slope value in the transition band. Nevertheless, the impact of the parasitic capacitances could be decreased by adjusting the magnitude of $C_1 >> C_{ZC1}$ & C_{p2}, $C_2 >> C_{ZC2}$ & C_{p3}, $C_3 >> C_{ZC2}$, C_{n3}, C_{n2}, & C_{n1}, $R_A >> R_{Z2}$ and $R_B >> R_{Z3}$.

3.4. Simulation Results

The proposed LP FO-LPF of order (1 + α), as shown in Figure 8, is simulated in the Cadence Virtuoso design tool using a 0.18 µm TSMC process parameter. The supply voltage used for filter simulation is, $V_{DD} = -V_{SS}$ = 300 mV, and V_B is kept at −250 mV. The layout of the proposed LV-LP fractional-order LPF circuit is shown in Figure 10. It covers an overall area of 36,600 µm^2 (200.38 µm × 183.79 µm). Note that the MOS capacitor occupies a significant area in the layout. The proposed filter offers electronic tuning of its order and pole frequency by adjusting the bias current of the three VDDDAs used. Also, this electronic tuning of order and pole frequency is independent of each other. For changing the order of the filter, it is necessary to adjust the parameter α. All the parameters, such as forward gain (A_1, A_2), and time constants (τ_0, τ_1, and τ_2) are dependent on the value of α. Consequently, all the transconductance values are also reliant on α. So, in order to obtain the desired transconductance value for each individual order, it is necessary to establish a distinct bias current for each VDDDA block as well as it is also necessary to change the value of resistors connected in the forward path. Figure 11 demonstrates the pre-layout and post-layout magnitude and phase response of the proposed filter, which highlights the tunability of the filter's order. The values of capacitances, resistances, transconductances, and corresponding bias currents for different filter orders are summarized in Table 2. The bias current values are set accordingly to obtain the simulation results in Figure 11. The pole frequency selected for the simulation is 1 kHz. In Figure 11, it is evident that the attenuation in the stopband changes according to −20 × (1 + α) dB/dec, where (1 + α) is the order of the proposed filter. In Table 3, the attenuation obtained by simulation and theoretical calculation is compared for different orders. From Table 3, it is clear that the simulated result closely follows the theoretical values obtained mathematically. Also, the power consumption of the proposed FO-LPF is only 663 nW, which makes the proposed filter design suitable for the low-power application.

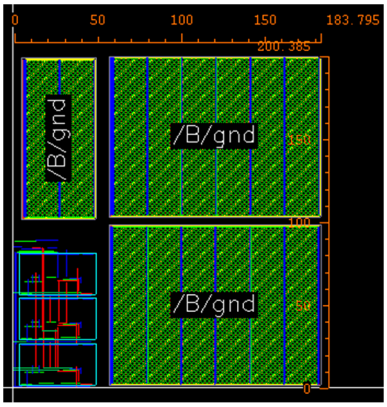
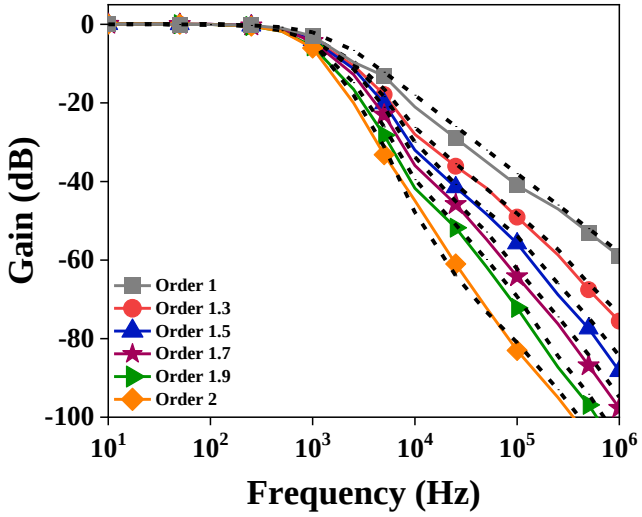
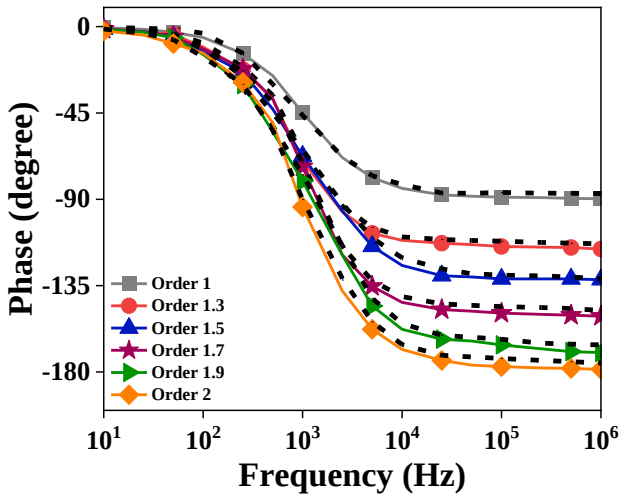


Figure 10. Layout of proposed FOF.



(**a**)



(**b**)

Figure 11. LP filter characteristics for different orders: (**a**) magnitude; (**b**) phase. (Pre-layout: solid line; post layout: dotted line).

Table 2. Parameter values for different values of orders for f_0 = 1 kHz.

Order of Filter	1.3	1.5	1.7	1.9
C_1 [pF]	90	90	90	90
C_2 [pF]	90	90	90	90
C_3 [pF]	30	30	30	30
R_A [kΩ]	2	1.67	1	0.5
R_B [kΩ]	4.6	4	3.4	2.8
g_{m1} [nS]	150	172	190	210
g_{m2} [nS]	619	650	652	607
g_{m3} [nS]	643	537	485	475
I_{b1} (nA)	12.3	12.5	12.9	14.5
I_{b2} (nA)	72	74	74.1	65
I_{b3} (nA)	75	53	47	46

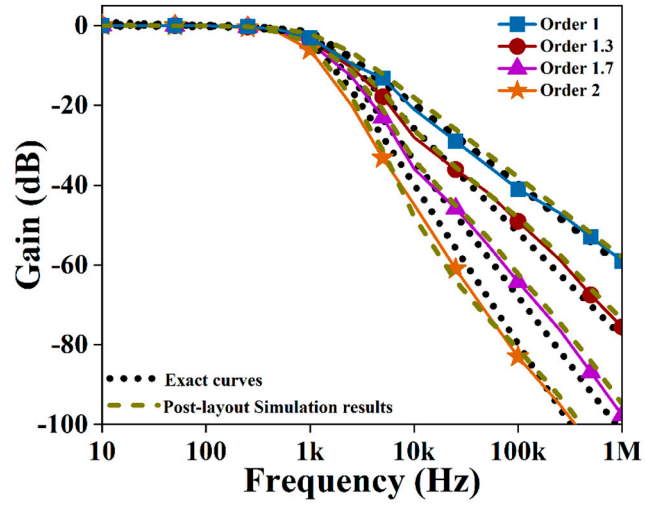
Table 3. Theoretical and simulated slope of attenuation for different values of orders for f_0 = 1 kHz.

Order of Filter	Slope of Attenuation [dB/dec]	
	Theoretical	Simulated
1.3	26	26.04
1.5	30	30.57
1.7	34	33.64
1.9	38	37.61

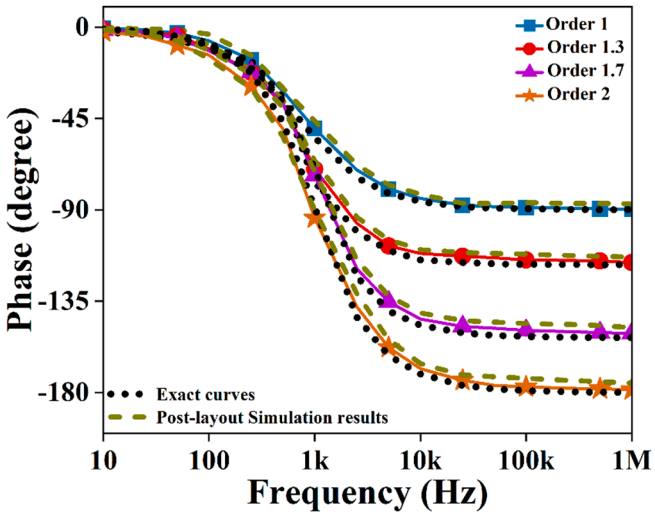
Figure 12 illustrates the magnitude and phase response of a FO-LPF for orders 1.3 and 1.7. The graphs provide a comparative analysis between the simulation results and the exact curves, as determined by (3). The resemblance between the simulated result and the exact curves is evident. The suggested filter design allows for the adjustment of the pole frequency without changing the filter's order. This can be accomplished by modifying the transconductances of the VDDDAs that implement the integrators, while maintaining the forward current gain values as the same. In order to achieve tunability, the filter's selected order is set to 1.5. The capacitance values, as well as the g_{m4} and g_{m5} parameters, remain unchanged from those specified in Table 2 for the purpose of this simulation. Table 4 provides a compilation of transconductances and biasing currents that were used. The simulated pre-layout and post-layout magnitude and phase response of the proposed filter showing the tunability feature for order 1.5 are shown in Figure 13. The theoretical pole frequencies chosen to illustrate the controllability are 500 Hz, 1 kHz, and 2 kHz. Pole frequency values obtained by post-layout simulations are 502 Hz, 1.003 kHz, and 2.007 kHz, which confirm the workability of the proposed design, as summarized in Table 5.

Table 4. Parameter values for different values of frequencies with order 1.5.

Pole Frequency	500 Hz	1 kHz	2 kHz
C_1 [pF]	90	90	90
C_2 [pF]	90	90	90
C_3 [pF]	30	30	30
R_A [kΩ]	1.67	1.67	1.67
R_B [kΩ]	4	4	4
g_{m1} [S]	85.8 n	172 n	343 n
g_{m2} [S]	325 n	650 n	1.3 µ
g_{m3} [S]	269 n	537 n	1.07 µ
I_{b1} (nA)	5	12.5	29
I_{b2} (nA)	26	74	150
I_{b3} (nA)	20	53	145



(**a**)



(**b**)

Figure 12. Filter characteristics showing exact curves, pre-layout, and post-layout simulation results: (**a**) magnitude; (**b**) phase. (Pre-layout: solid line).

The output noise of the FO-LPF is plotted in Figure 14. The pre-layout and post-layout noise of FOF is found to be 691 nV/$\sqrt{}$Hz and 767 nV/$\sqrt{}$Hz at 10 Hz, and after that, it observes an exponential decay and decreases to a value of 134 nV/$\sqrt{}$Hz and 186 nV/$\sqrt{}$Hz at 1 kHz for pre-layout and post-layout respectively. The linear performance of the FOF for orders 1.5 and 1.7 was tested by an input signal of a single tone at 100 Hz with variable amplitude. The total harmonic distortion (THD) results are displayed in Figure 15. It is apparent that up to 250 mV of input amplitude, the THD value is below 4%, which is quite low. In Figure 16, the time domain response of FO-LPF is presented for voltage signals having amplitude of 200 mV and frequency of 100 Hz.

Table 5. Theoretical and post-layout simulated pole frequency values for order 1.5.

Theoretical Pole Frequency	Simulated Pole Frequency
500 Hz	502 Hz
1 kHz	1.003 kHz
2 kHz	2.007 kHz

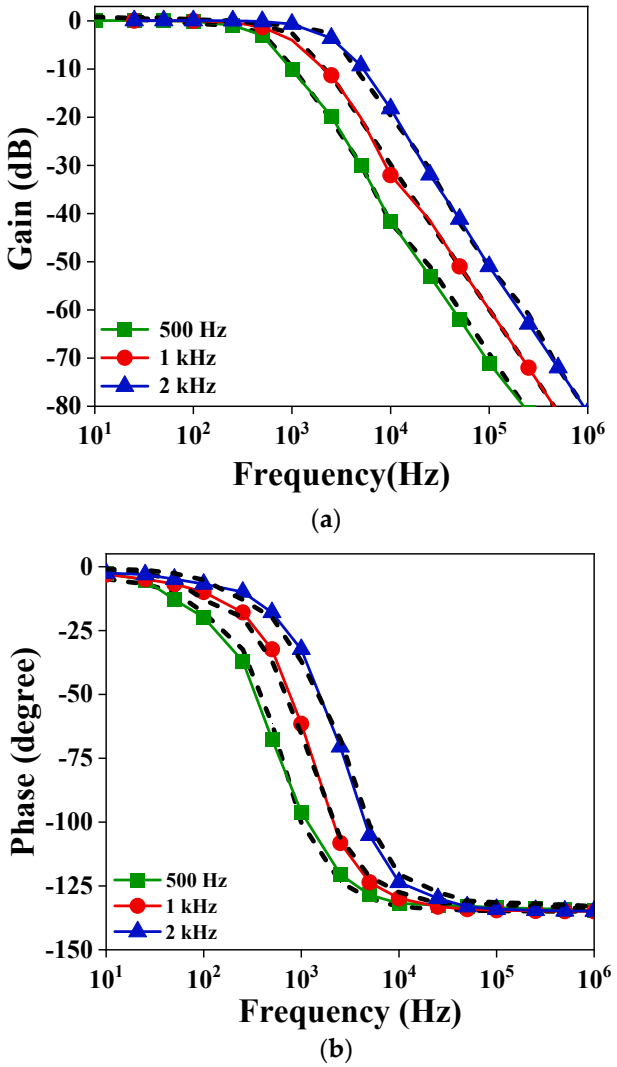


Figure 13. LP filter characteristics at different pole frequencies for order 1.5: (**a**) magnitude; (**b**) phase. (Pre-layout: solid line; post layout: dotted line).

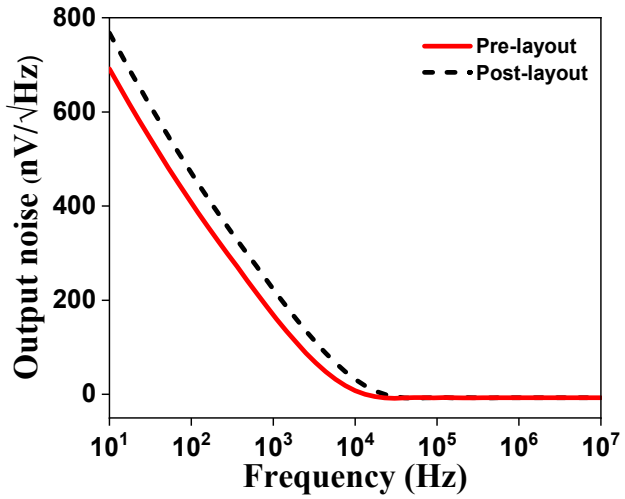


Figure 14. Output noise of low-pass FOF.

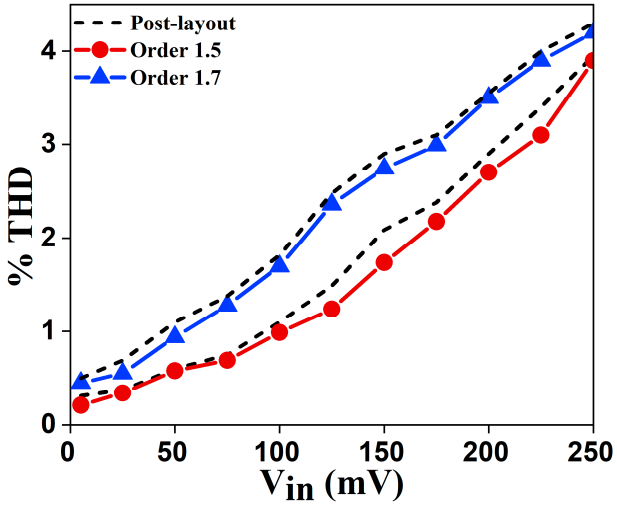


Figure 15. Linearity plot for low-pass FOF.

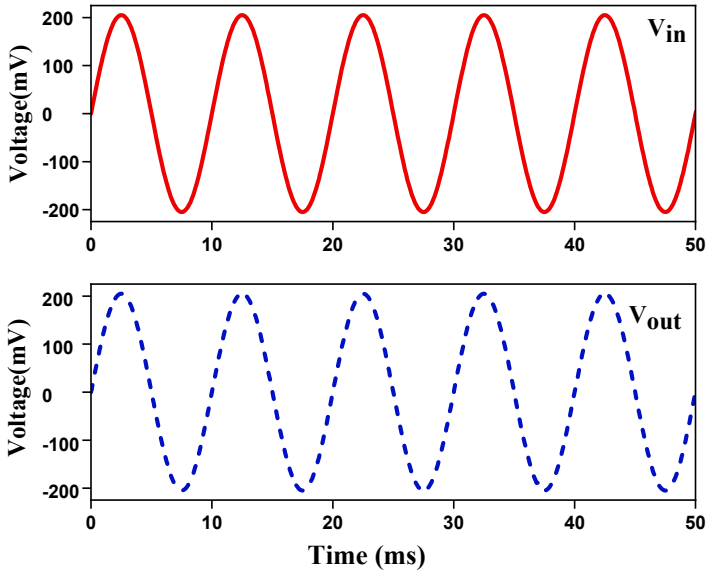


Figure 16. Time-domain responses of FO-LPF.

Transistor corners as SS, TT, and FF, voltage supply corners as ±10% of V_{DD}, and temperature corners as −40 °C, 0 °C, 27 °C, and 80 °C were used in the analysis of process, voltage and temperature (PVT) corners. Figures 17–19 display the outcomes of the proposed filter's magnitude characteristics with process, voltage, and temperature corner analysis, respectively. From Figure 17, it is clear that as anticipated, the response of the process corner exhibits limited variation. Based on the magnitude curve illustrated in Figure 18, it can be inferred that the FO-LPF design does not exhibit significant variations across different temperatures. Thus, the proposed circuit demonstrates satisfactory performance throughout a broad spectrum of temperature variations. From Figure 19, FO-LPF characteristics are satisfactory for up to 10% variation in V_{DD}. Through the use of the Monte-Carlo analysis for N = 600 samples, the sensitivity of the pole frequency with regard to the impact of transistor mismatching and process parameter fluctuations was assessed. The magnitude characteristics and statistical plots, obtained at $\alpha = 0.5$, are shown in Figure 20. The standard deviation of the pole frequency is 12.94 Hz. Given that the desired pole frequency value is 1 kHz, it is possible to draw the conclusion that the filter has acceptable sensitivity characteristics.

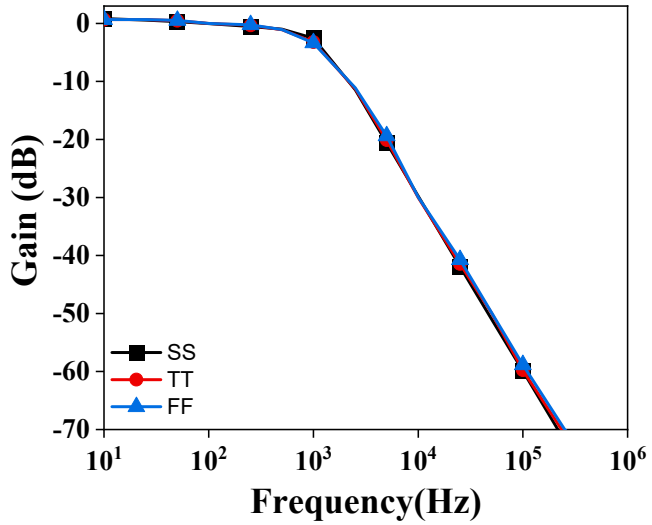


Figure 17. Magnitude characteristics for process variations.

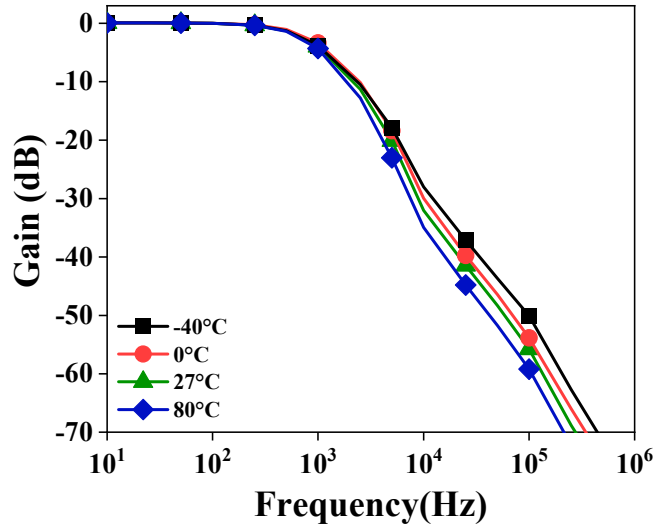


Figure 18. Magnitude characteristics for temperature variations.

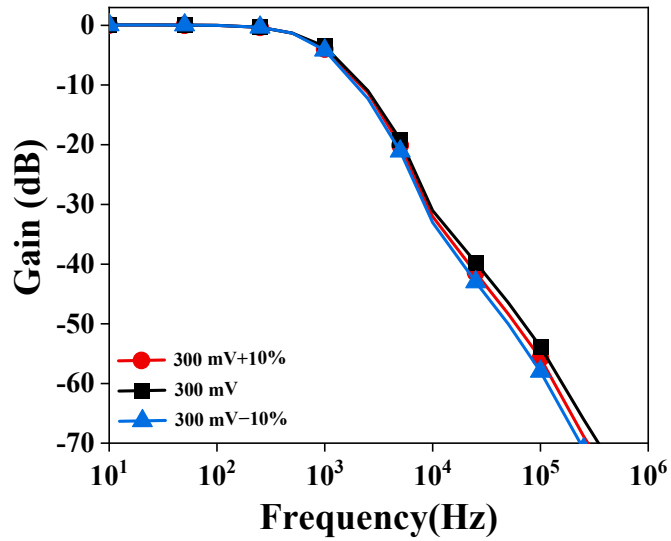


Figure 19. Magnitude characteristics for voltage variations.

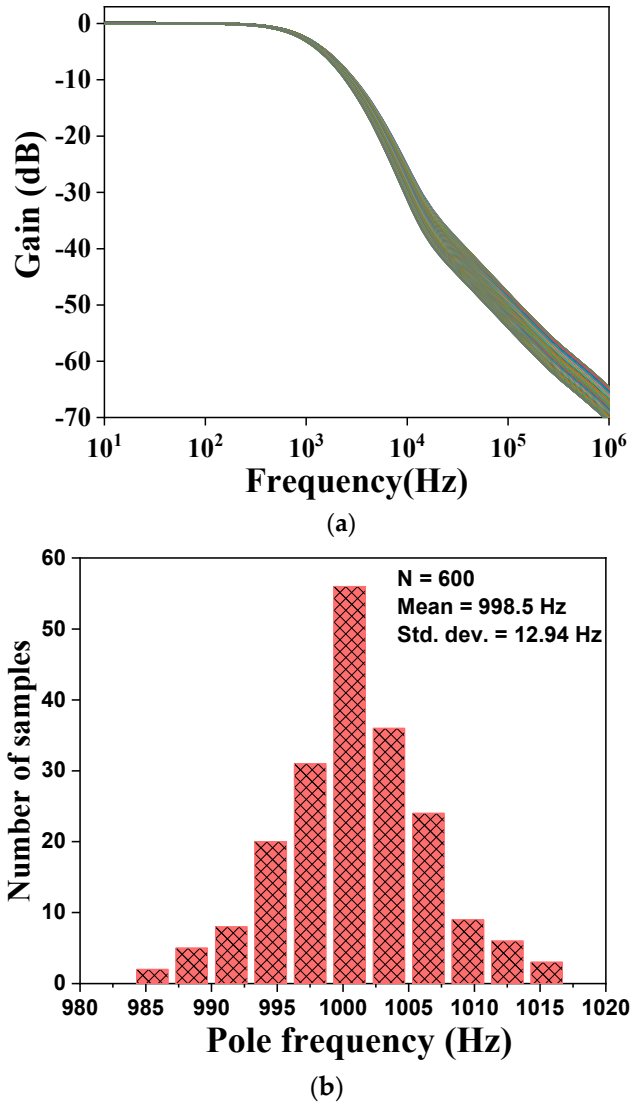


Figure 20. (**a**) Monte-Carlo analysis of FO-LPF, (**b**) Histogram plot for 600 run cycles.

The transfer function given in (21) represents filter characteristics when the filter is affected by tracking-error parameters. To observe the effect to these parameters, the sensitivity analysis was performed for the obtained transfer function in (21), with respect to the tracking-error parameters. The objective of sensitivity analysis is to assess the impact of changes in these parameters on the performance of the filter. The given expression comprises a total of eleven tracking-error parameters that are α_{p1}, α_{p2}, α_{p3}, β_{z1}, β_{z2}, β_{z3}, β_{n1}, β_{n2}, β_{n3}, β_{p2}, and β_{p3}. Through simulation, there values were obtained as follows: $\alpha_p = 0.98$, $\beta_z = 0.99$, $\beta_n = 1.003$, $\beta_p = 0.92$. Generally speaking, the relative sensitivity to each parameter is characterized as follows:

$$S_x^{TF} = \frac{x}{TF}\frac{dTF}{dx} \tag{27}$$

where, TF represents the transfer function of the filter and x represents the parameter that affects this transfer function. This analysis was conducted for order 1.5 at $f_0 = 1$ kHz. The remaining parameter values, such as capacitance, resistance, and transconductance are presented in Table 2. The sensitivity obtained for these tracking-error parameters were a function of parameter values and frequency and thus the magnitude of sensitivity versus frequency curve, in terms of the aforementioned tracking-error parameters, is depicted in

Figure 21. The graph demonstrates the variation in sensitivity as a function of frequency and parameters β_{n1}, and β_{z1} show highest sensitivity in the pass band range of FO-LPF.

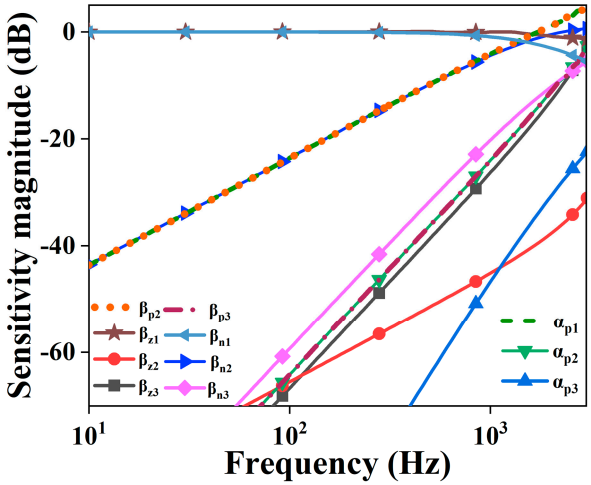
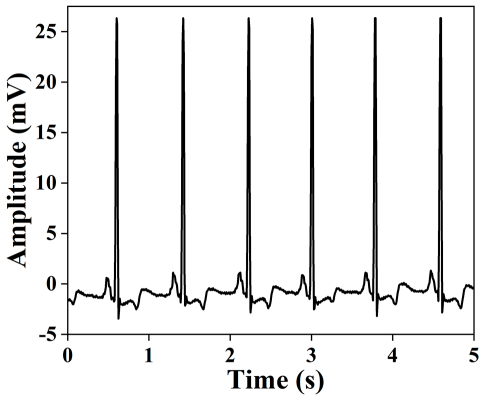
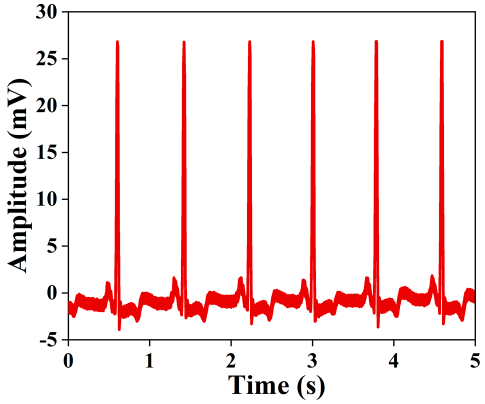


Figure 21. Sensitivity plot of the proposed filter with respect to tracking-error parameters.

To demonstrate the practical significance of the proposed circuit, an assessment of the filter's efficiency in processing the electrocardiogram (ECG) signal is performed. The input ECG signal exhibits an amplitude of 25 mV, and it was mixed with a sinusoidal signal of 1 kHz frequency and an amplitude of 50 µV. The noisy ECG signal was passed through the FO-LPF of pole frequency 2 kHz. Figure 22 displays the actual ECG, the ECG with added noise, and the ECG that was restored after passing through the filter. This demonstrates that the suggested filter is well-suited for practical applications such as ECG filtering.

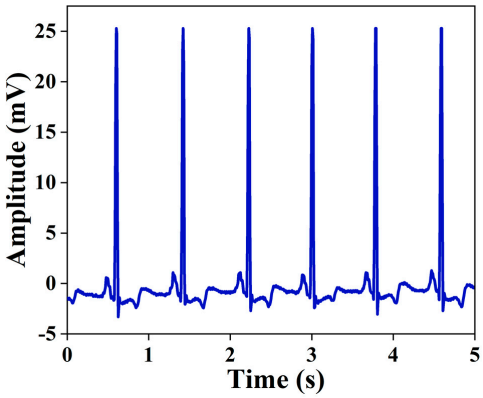


(**a**)



(**b**)

Figure 22. *Cont.*



(**c**)

Figure 22. (**a**) The original ECG signal; (**b**) the noisy ECG signal; (**c**) the filtered ECG signal.

4. Comparison

Given that the integer-order approximation technique is utilized for designing FO-LPF, the state-of-the-art in Table 6 incorporates FOFs that are designed using the same approximation technique. While comparing the proposed FOF with other FOFs available in the literature, several observations were made as outlined below.

The table reveals that the number of active blocks employed in the references [6,15–21,32–37] exceeds the number of blocks utilized in the proposed FOF. Additionally, the implementation of the FOF in [6,14–16,19–21,32,33,36,37] involves the utilization of a significant quantity of resistors. It is worth noting that the majority of these resistors are floating. Conversely, the proposed FOF incorporates a grounded active resistor that is implemented using MOSFET, making the design well-suited for the fabrication process. In addition, it should be noted that the designs, with the exception of the ones referenced as [17,18,32–34,36,37], do not offer tunability of order and pole frequency.

Regarding the utilization of passive components, it is seen that only [17,18,34,35] exhibit an equivalent or lesser quantity of passive components compared to the design under consideration. However, upon analysing the number of active components, it is evident that [17,18,34,35] exhibit a significantly greater number of active components in comparison to the proposed design. Additionally, the design of [35] incorporates the utilization of five fractional capacitors (FC). The functions performed by [20,34,36] encompass LPF along with additional functionalities. However, [20] employs floating passive components and lacks electronic tuning capabilities. On the other hand, [34] utilizes a significant number of active components, operates at a higher supply voltage, and exhibits high power dissipation. Ref. [36] employs floating passive components and incorporates five FCs in its design. The DC supply voltage employed for the operation of the suggested filter circuit is $\pm$300 mV, which is the smallest value when compared to the other designs. It is comparable only to [19], where the supply voltage is $\pm$0.5 V. However, it should be noted that [19] utilizes resistors in the implementation of the filter. The LV-LP methodology is utilized in the filter implementation only in [19] and the proposed method. Consequently, none of the other circuits can be considered suitable for operation in the LV-LP domain. Furthermore, the power consumption of the suggested circuit is the lowest among the designs that were studied.

Thus, the proposed circuit is beneficial in terms of its use of only three active building blocks, six MOS transistors, and three grounded capacitors for implementing fractional-order LPF, which is suitable for its operation in the LV-LP domain since it uses only $\pm$300 mV as its power supply and consumes only 663 nW. The proposed filter offers electronic and independent order and pole frequency tuning. Furthermore, this is the only circuit apart from [19] to be used in the low-voltage and low-power domain.

Table 6. Relative studies of the proposed FO-LPF with fractional filters available in the literature.

[Ref.] (Year)	Type (Number) of ABB Used	Function Realized	No. of Passive Elements (R, C)	Grounded/Floating Elements	Supply Voltage	Electronic Tunability	Use of LV-LP Technique	Total Power Dissipation (W)
[6] (2016)	CCII (4), DDCC (1)	LPF	7, 3	G	NA	No	No	NA
[14] (2011)	OPAMP (2)	LPF	10, 3	F	NA	No	No	NA
[15] (2018)	CFOA (4)	LPF	9, 3	F	±10 V	No	No	NA
[16] (2016)	CFOA (4)	LPF	10, 3	F	±10 V	No	No	NA
[17] (2018)	OTA (3), MOCF (1), ACF (2)	LPF	0, 3	G	±1 V	Yes	No	NA
[18] (2017)	OTA (3), CF (1), ACA (3)	LPF	0, 3	G	NA	Yes	No	NA
[19] (2016)	DDCC (5)	LPF	7, 3	G	±0.5 V	No	Yes	0.185 m
[20] (2020)	CDBA (5)	LPF, BPF	11, 3	F	±10 V	No	No	NA
[21] (2017)	UVC (4)	LPF	10, 3	F	NA	No	No	NA
[32] (2018)	MOCF (2), DOCF (1), ACA (5)	LPF	3, 3	F	NA	Yes	No	NA
[33] (2017)	ACA (5), FD-CF (3)	LPF	6, 3	F	NA	Yes	No	NA
[34] (2019)	OTA (8), CF (1)	LPF, HPF, BPF, BRF	0, 3	G	±0.75 V	Yes	No	8.74 µ
[35] (2021)	OTA (6), CF (3), ACA (1)	LPF	0, 1 *	G	±1.65 V	No	No	72.6 m
[36] (2022)	CDBA (4)	APF	11, 3	F	NA	Yes	No	NA
[37] (2023)	CFTA (5)	LPF	2, 3	G	±0.9 V	Yes	No	6.8 m
Proposed	VDDDA (3), MOS (6)	LPF	0, 3	G	±0.3 V	Yes	Yes	663 n

* Uses 5 fractional-order capacitors.

5. Conclusions

In this paper, a VDDDA and a low-pass fractional-order filter structure capable of operating at low voltage and in low-power applications were presented. The VDDDA structure is implemented using the bulk-driven metal oxide semiconductor (BD-MOS) transistor technique and is operated in the subthreshold region. VDDDA uses $V_{DD} = -V_{SS} = 300$ mV and dissipates only 207 nW of power for its operation. Furthermore, this block is used to implement a FO-LPF of order $(1 + \alpha)$. The filter structure comprises three VDDDAs, three grounded capacitors, and two active resistors. Also, the electronic tuning feature of the proposed filter design offers independent tuning of its order and frequency through the bias current of the active component used. The effects of tracking errors and parasitics on the performance of the proposed FO-LPF were analyzed. This filter is capable of LV-LP operation because it is operated at ±300 mV and dissipates only 663 nW of power. The layout of the proposed VDDDA, as well as the FO-LPF, were laid out in a Cadence environment using 0.18 µm CMOS technology parameters and covered a chip area of 1208 μm^2 and 36,600 μm^2, respectively. Post-layout simulation results are also included, which imply that they are suitable for fabrication. Noise, total harmonic distortion, Monte-Carlo and PVT analyses were also performed.

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Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

The drain current of a long-channel PMOS transistor operating in a weak inversion region is given by [38]:

$$I_{out} = I_s \left(\frac{W}{L}\right) e^{\left(\frac{V_{SG}-V_{th}}{nV_T}\right)} \left[1 - e^{\left(\frac{-V_{SD}}{V_T}\right)}\right]. \tag{A1}$$

where $I_s = \left(2nV_T^2\right) \times (\mu C_{ox})$, V_T is the thermal voltage having a value of 25 mV at room temperature, and n is the slope factor. If $V_{SD} > 3V_T$, then input transistors are in the saturation region of weak inversion. By considering $V_{th} = V_{TO} - (n-1)\, V_{SB}$ and $V_{SD} > 3V_T$, (A1) is simplified to the following:

$$I_{out} = I_s \left(\frac{W}{L}\right) e^{\left(\frac{V_{SG}-V_{T0}+(n-1)V_{SB}}{nV_T}\right)}. \tag{A2}$$

Since, $I_{out} = I_Z = I_{D1} - I_{D2}$, using values of I_{D1} and I_{D2} from (A2), I_{out} can be written as below:

$$I_{out} = I_s \left(\frac{W}{L}\right) \left[e^{\left(\frac{V_{SG1}-V_{T0}+(n-1)V_{SB1}}{nV_T}\right)} - e^{\left(\frac{V_{SG2}-V_{T0}+(n-1)V_{SB2}}{nV_T}\right)}\right],$$

$$I_{out} = I_s\left(\frac{W}{L}\right)e^{(-V_{T0}/nV_T)}\left[\underbrace{e^{\left(\frac{V_{SG1}+(n-1)V_{SB1}}{nV_T}\right)}}_{\alpha} - \underbrace{e^{\left(\frac{V_{SG2}+(n-1)V_{SB2}}{nV_T}\right)}}_{\beta}\right]. \quad \text{(A3)}$$

Multiplying the above equation by $\frac{\alpha+\beta}{\alpha+\beta}$, and then assuming $I_x = I_{D1} + I_{D2}$, (A3) can be rewritten as follows:

$$I_{out} = I_X\frac{\left[e^{\left\{\frac{(V_{SG1}-V_{SG2})+(n-1)(V_{SB1}-V_{SB2})}{2nV_T}\right\}} - e^{\left\{\frac{(V_{SG2}-V_{SG1})+(n-1)(V_{SB2}-V_{SB1})}{2nV_T}\right\}}\right]}{\left[e^{\left\{\frac{(V_{SG1}-V_{SG2})+(n-1)(V_{SB1}-V_{SB2})}{2nV_T}\right\}} + e^{\left\{\frac{(V_{SG2}-V_{SG1})+(n-1)(V_{SB2}-V_{SB1})}{2nV_T}\right\}}\right]}. \quad \text{(A4)}$$

Now, from Figure 2, we deduce the following:

$V_{SG1} = V_{S1} - V_G$, $V_{SG2} = V_{S2} - V_G$, $V_{SB1} = V_{S1} - V_+$, $V_{SB2} = V_{S2} - V_-$

Now, putting these values in (A4), and using $\tanh(x) = \frac{e^x - e^{-x}}{e^x + e^{-x}}$, (4) can be simplified as follows:

$$I_{out} = I_X\tanh\left(\frac{-(n-1)(V_+ - V_-)}{2nV_T}\right),$$

$$I_{out} = I_B\tanh\left(\frac{(n-1)(V_{in})}{2nV_T}\right). \quad \text{(A5)}$$

Using Taylor series expansion, (A5) can be decomposed and considering $(n-1) = \eta$, the transconductance of the input differential pair can be given as below:

$$G_m = \frac{I_{out}}{V_{in}} = \frac{I_B(n-1)}{2nV_T} = (n-1)\left(\frac{I_B}{2nV_T}\right) = (n-1)g_{m1,2},$$

$$G_m = g_{mb1,2}.$$

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