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35th International Conference Radioelektronika

pages: 1-5

eISBN: 979-8-3315-4447-8

eISSN: 2767-9969

DOI: https://doi.org/10.1109/RADIOELEKTRONIKA65656.2025.11008405

Accepted manuscript

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High-Matching Current-Starved Inverter for Two-Dimensional Vernier Time-to-Digital Converter

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***Abstract*—This paper proposes a novel improved Current-Starved Inverter (CS-INV) for application in a ring oscillator, integral to a 2D Vernier time to digital converter. Through the comparative analysis of two prevalent CS-INV topologies, we introduce a novel topology aimed at minimizing delay variation within the ring oscillator (caused by mismatches between CS-INVs in the ring oscillator), which is essential for ensuring good Integral and Differential Nonlinearity. The primary objectives were to achieve minimal delay variation and to reduce current consumption, while ensuring functionality at the slowest PVT corners. The ring oscillator operates at 640 MHz and comprises 26 CS-INVs. The design, implemented in 65 nm CMOS technology, demonstrated a delay matching variation of 2.03 ps with a current consumption of 384 µA. The performance metrics were substantiated through simulations using a high-sigma verification tool.**

***Index Terms*—current-starved inverter, delay cell, low power, matching, time-to-digital converter, Vernier**

I. Introduction

A Time-to-Digital Converter (TDC) is a device that can convert a measured time interval into a digital word, similar to how an Analog-to-Digital Converter (ADC) converts a voltage or current level into a digital word. Its performance is typically utilized in systems where precise measurement of time intervals is required, with resolutions in the order of picoseconds. Examples include All-Digital Phase Locked Loops (AD-PLL) [1], [2], Light Detection and Ranging (LiDAR) [3], [4], and Positron Emission Tomography (PET) [5].

Most TDC designs use Delay Cell (known also as Time Acquisition Position - TAP) structures as basic building blocks for Tapped Delay Lines (TDLs) or Ring Oscillators (ROs). The resolution of a TDC is usually derived from the TAP delay. In the simplest TDCs based on TDLs, the resolution is determined by twice the intrinsic delay of a self-loaded inverter [6]. If a smaller resolution is needed (known as subgate resolution), the Vernier principle (one-dimensional, 1D) can be employed [7]. For further performance improvements in Vernier TDCs, a two-dimensional (2D) structure can be used [8]. However, both mentioned Vernier-based TDCs are sensitive to the matching of delays between TAPs in the TDL or RO, which is critical for achieving good Differential and Integral Nonlinearity (DNL and INL) of the converter.

Research described in this paper was supported by the Internal Grant Agency of the Brno University of Technology under project no. FEKT-S-23-8191

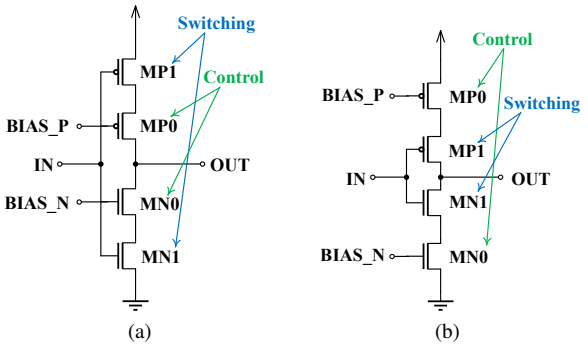


Fig. 1: (a) DRAIN-side control CS-INV; (b) SOURCE-side control CS-INV

The paper is organized as follows: First, we discuss two fundamental existing current-starved Inverters (CS-INVs), which serve as the foundational building blocks for delay cell construction. Next we introduce, a new CS-INV topology. The subsequent section presents results based on simulation analysis, and finally, the paper concludes with a summary of the findings.

II. Existing Current-Starved Inverters

Delay cell tunability, which is very important for Process-Voltage-Temperature (PVT) variation compensation, can be implemented in several ways. A very intuitive approach is to limit the bandwidth of a simple inverter to make it slower. This limitation can be achieved by tuning transistors added to current-flowing branches. In this section we briefly discuss the important properties of the two most common CS-INVs shown in Fig. 1.

A. DRAIN-side controlled CS-INV

In general, when attempting to achieve component matching, scaling up transistors is a common approach. Increasing the length of the switching transistors, MN1 and MP1, results in a slower inverter, while increasing their width raises C_{LOAD}. Therefore, to maintain high-speed performance, it is essential to keep their dimensions within acceptable limits, particularly when the OUT node is additionally loaded by metalization and sensing arbiters (e.g., D-Flip Flops) in the TDC. Scaling the control transistors, MN0 and MP0, may offer

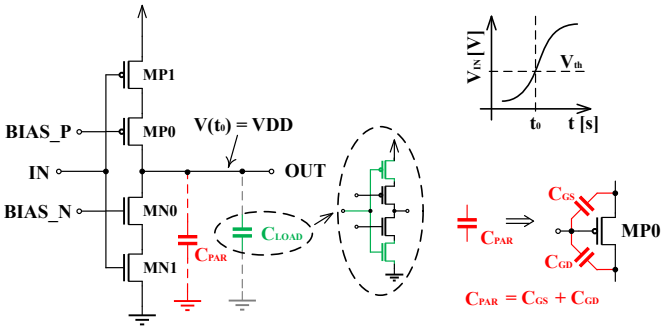


Fig. 2: Load and parasitic capacitances of DRAIN-side control CS-INV: explanation by rising edge at IN node

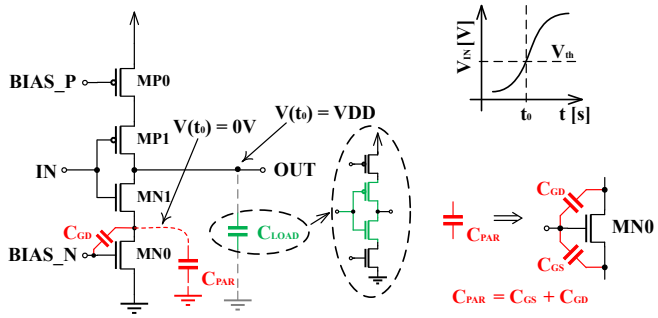


Fig. 3: Load and parasitic capacitances of SOURCE-side control CS-INV: explanation by the rising edge at the IN node

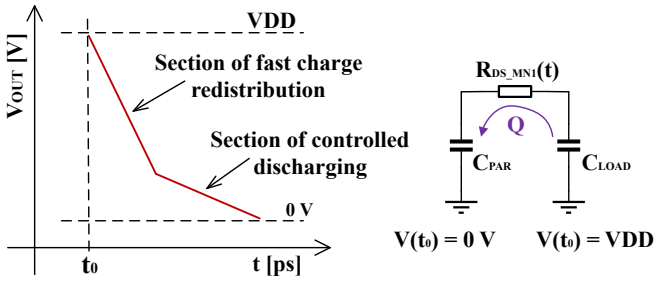


Fig. 4: Illustration of the falling edge distortion caused by large C_{PAR} capacitance

a more advantageous solution; however, this approach also has inherent limitations - some balance should be found. In our analysis, we will focus on optimizing the sizing of control transistors, while ensuring that the switching transistors are only as large as necessary to handle the required (dis)charge current efficiently.

For the analysis of the CS-INV shown in Fig. 1a, we assume the model presented in Fig. 2. This model contains the basic parasitic capacitance C_{PAR} in parallel with C_{LOAD}. Let us assume that t_0 is the time when the rising edge at the IN node reaches approximately the threshold voltage V_{th} of the switching transistor MN1. After this point, the inverter, consisting of MN1 and MP1, starts switching to the opposite state. Capacitances C_{LOAD} and C_{PAR} were charged to VDD from the previous state, and the NMOS branch of the CS-INV begins discharging both capacitances to 0 V.

It is evident that scaling up the control transistor MP0 increases its parasitic capacitances, the most significant of which is the gate-to-source capacitance C_{GS}, which represents a large capacitance between the gate and the formed channel [9]. Consequently, MN1 must discharge the total charge from both C_{LOAD} and C_{PAR}. This makes the entire DRAIN-side control CS-INV slower and more power-hungry, particularly when MN0 and MP0 are large to achieve the required matching.

This phenomena can also be observed on the opposite edge, where MP1 must charge both C_{LOAD} and C_{PAR} (which is now formed by the scaled-up MN0).

B. SOURCE-side controlled CS-INV

One possible solution to mitigate this problem is to reconfigure the CS-INV to a SOURCE-side control - Fig. 1b. For the analysis we assume the model presented in Fig. 3, which contains the main parasitic capacitance, C_{PAR}, which is located at the drain of the control transistor MN0. It is primarily formed by the capacitance between the gate and the formed channel. Another parasitic capacitance is C_{GD}, caused by the overlap between the gate and the drain diffusion area.

Firstly, we define the initial conditions in the same way as in the case of the DRAIN-side controlled CS-INV. Figure 3 shows the rising edge at the IN node and the initial voltages of the most important nodes (voltages from the previous state). Sizing of the control transistors can affect switching performance in two ways:

1) If the value of C_{PAR} is comparable to C_{LOAD}, the following effect can be observed: as the input voltage reaches roughly V_{th}, the inverter starts switching to the opposite state. Due to the different initial voltages of C_{PAR} and C_{LOAD}, after MN1 turns on, a fast redistribution of charge stored in C_{LOAD} occurs. As the channel of MN0 charges up, the controlled discharging phase begins. This leads to a distortion in the edge shape, which can be divided into two parts: the charge redistribution phase and the discharging phase. This is illustrated in Fig. 4. It is evident that during the fast charge redistribution, delay is not under control, and the length of this phase depends on the capacitance ratio and MN1 R_{ON}. This effect may limit or even disable our ability to control the delay effectively.
2) If the control nodes BIAS_N and BIAS_P are not driven by a low-impedance source, the capacitive coupling caused by the fast switching through C_{GD} may momentarily bias up the gate of MN0, distorting the delay control and temporarily speeding up the switching. This effect can also be observed in DRAIN-side controlled CS-INV, but in the opposite manner, where the control node BIAS_N is pulled low due to the C_{GS} of MN0. However, this issue is mitigated by the cascode-effect of both control transistors in the DRAIN-side control topology.

By carefully tuning the sizes of the components, we can

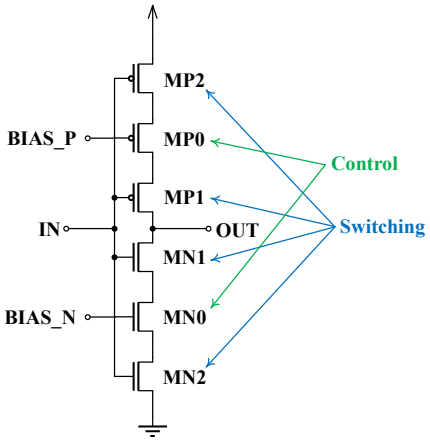


Fig. 5: Proposed novel CS-INV with switching transistors in both current branches

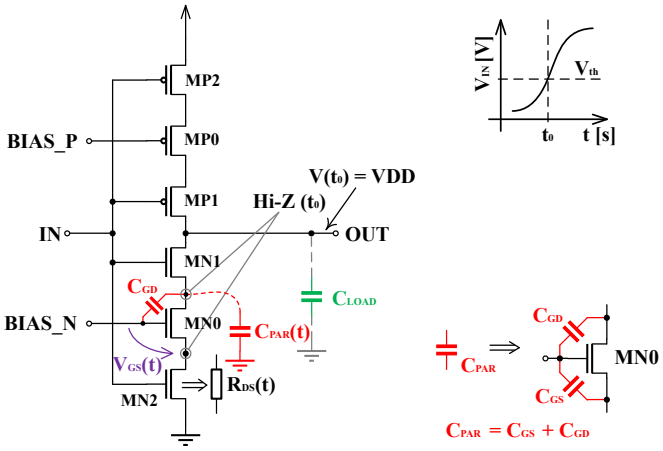


Fig. 6: Model of proposed CS-INV: explanation by the rising edge at the IN node

minimize both of the aforementioned effects and achieve very good delay matching (within 2 ps). Unfortunately, during our research, we found that the power demands of the well-matched SOURCE-side control CS-INV were too high for our intended applications, or its tunability across the entire PVT space was limited.

Based on previous analysis, we propose a new type of CS - INV which has very good delay matching as well as low power consumption. This novel topology will be discussed in the next section.

III. Proposed Current-Starved Inverter

Deriving analytical expressions for the design relationships governing delay and its matching is nearly infeasible due to the high-speed nature of the circuit, which requires detailed knowledge of all parasitic elements, their nonlinearities, and the fact that all transistors operate across their full range of operating modes. The design of the proposed topology was conducted iteratively, as was the case for the other two topologies, and was informed by insights gained during the development of standard current-starved inverters shown in Fig. 1. These inverters were optimized for delay matching, low power consumption, and tunability, even under the slowest PVT corner. The performance of this novel topology is thoroughly discussed in this section.

A. Purpose of Topology

The DRAIN-side control of the CS-INV, as previously mentioned, suffers from higher power demands. However, due to the cascode-like behavior of the control transistors (cascoding MN1 and MP1), the effect of control node entrainment is mitigated. To preserve this mitigation effect while maintaining low power consumption, we decided to "distribute" the switching transistor across both sides of the control transistor, as illustrated in Fig. 5. This approach results in two key effects that enhance overall performance. For simplicity we describe it in the same way as for traditional topologies, with rising edge on the IN node inline with Fig. 6:

1) As discussed in the analysis of the SOURCE-side control CS-INV, delay controllability can be influenced by C_{GD} during the fast switching phase. In the proposed CS-INV, the switching transistor MN2 acts as a time-dependent resistance, which helps stabilize the V_{GS} of MN0 through a cascode effect.
2) A similar effect occurs when, due to sizing, a fast charge redistribution phase (see Fig. 4) is introduced. This charge redistribution causes a voltage drop across the R_{DS} of MN2, which reduces the V_{GS} of MN0, thereby stabilizing the controllability during the discharging phase.

The switching transistors MN1 and MP1 act as shields for the large V_{GS} capacitances of MN0 and MP0, helping to mitigate the effects discussed in the section on DRAIN-side controlled CS-INV, while also preserving the low power requirements of the proposed CS-INV.

B. Target Application

The target application of the proposed CS-INV is a fully differential ring oscillator-based 2D Vernier TDC. To maintain the differential nature of the RO in a straightforward manner, small and weak "injection" inverters were added, as illustrated in Fig. 7. Each node of the RO is loaded by six data inputs of D-Flip Flops, which serve as arbiters for capturing the RO state.

The phase noise of the RO plays a crucial role in the performance of the target application, particularly in terms of single-shot precision. Even in cases where the RO exhibits poor phase noise characteristics, systems can be designed to mitigate its effects—for example, by injection locking [10], [11]. However, this topic lies beyond the scope of this paper and will be addressed in future research.

IV. Simulation Results

The red-circled section of Fig. 7 also illustrates the simulation testbench. The RO nodes are appropriately wired to generate an "infinite" sequence of rising and falling edges

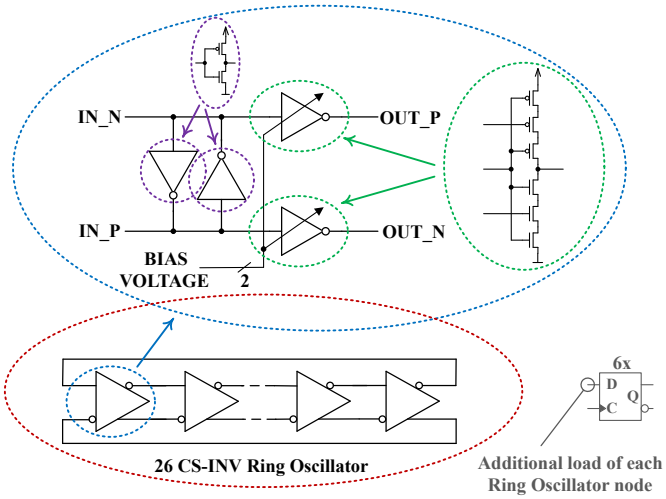


Fig. 7: Illustration of proposed CS-INV target application

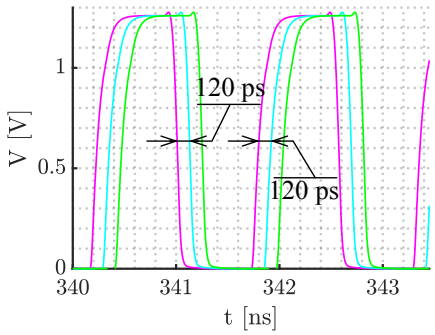


Fig. 8: Example of three nodes in time domain at the end of trimming

(the specific connection details of the RO are outside the scope of this paper). Control nodes were driven by low-impedance sources to mitigate unwanted effects. Our TDC concept involves capturing both the rising and falling edges, and thus, our goal is to achieve delay matching for both. For delay matching evaluation, we utilized Siemens' high-sigma verification tool, Solido™PVTMC software, across the entire PVT range:

- Supply voltage: 1.26 V
- Temperature: $-40\,°\text{C}$ to $+175\,°\text{C}$ ($27\,°\text{C}$ @nom)
- Process: 5-sigma corners.

In each simulation run, the RO was trimmed to the target frequency f_0, and the delays between rising and falling edges were extracted. An example of such a time-domain simulation is shown in Fig. 8. After simulating all PVT corners, the results were exported and post-processed in MATLAB. Histograms of rising and falling edge delays are presented in Fig. 9.

To ensure consistency in the comparison of the listed CS-INVs, we adopted the following approach: after determining the optimal sizes for the proposed CS-INV shown in Fig. 5, we applied the same sizing methodology to the remaining CS-INVs. We maintained the total area of the switching transistors consistent across all topologies to ensure a comparable C_{LOAD}, as well as consistent "channel length" in the current branches. Table I presents the specific sizing values used for the comparative analysis.

TABLE I: CS-INVs sizing for comparison analysis

	Fig. 1a		Fig. 1b		Fig. 5	
	W [μm]	L [nm]	W [μm]	L [nm]	W [μm]	L [nm]
MN0	15	65	15	65	15	65
MN1	2	160	2	160	2	80
MN2	—	—	—	—	2	80
MP0	15	65	15	65	15	65
MP1	2	160	2	160	2	80
MP2	—	—	—	—	2	80

TABLE II: Results of comparison analysis between CS-INVs

	Delay (τ)		I_{CC} [μA]	$f_{\max}$ [MHz]	FoM [-]
	$\mu_{\tau\,[ps]}$	$\sigma_{\tau\,[ps]}$ (1)			
Fig. 1a	120.2	3.78	354	1227	0.97
Fig. 1b	240.4	3.12	385	368	0.31
Fig. 5	120.2	2.03	384	981	1.26

(1) The worse of the two matchings (rising/falling edge) is presented

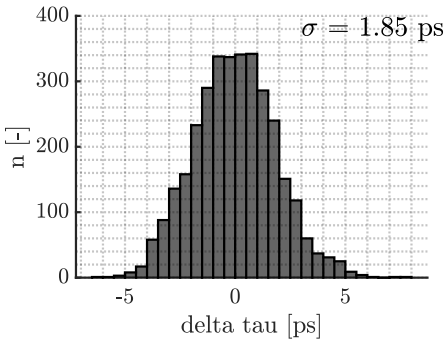
Table II presents the simulation results with transistor sizing in accordance with Table I. As observed, the DRAIN-controlled CS-INV can operate only at 368 MHz, preventing us from evaluating its matching at the required frequency of $f_0 = 640\,\text{MHz}$. The high power consumption of this topology is evident from column I_{CC}, which details the current consumption at f_0—notably, the power demands are similar even at half of the target frequency.

The comparison metric used is the Figure of Merit (*FoM*), defined as $FoM = \frac{f_{\max[MHz]}}{\sigma_{\tau[ps]} \cdot I_{\text{CC}[\mu A]}}$. Our objective was to maximize $f_{\max}$, minimize I_{CC}, and reduce σ_τ as much as possible. The Figure of Merit value confirms the performance of the proposed CS-INV relative to our design goals.

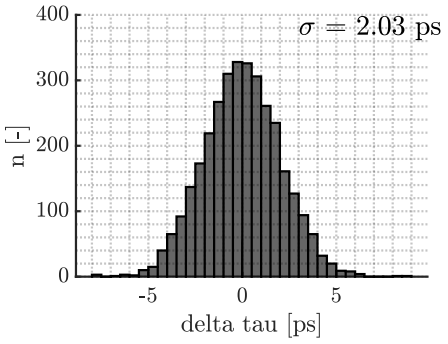
V. Conclusion

This paper presents a novel Current-Starved Inverter topology designed for use in a Ring Oscillator-based two-dimensional Vernier Time-to-Digital Converter. Special attention was given to matching of both rising and falling edges, power consumption, and tunability across the entire PVT space. Through optimization, we improved the delay matching by approximately 50 %, achieving a value of 2.03 ps, with a comparable current consumption of 384 μA at an oscillation frequency of $f_0 = 640\,\text{MHz}$ for a 26 CS-INV fully differential Ring Oscillator. The proposed design was implemented using a 65 nm CMOS technology.

It must be noted that properly laying out the presented oscillator remains a challenging task. All RO nodes must be equally loaded to ensure an equidistant distribution of delays along the oscillator. For this reason, it may be necessary to add extra loads to the RO, which can increase power consumption and reduce tunability. Even though post-layout simulation results are favorable, such a high-speed circuit must ultimately be evaluated on silicon, as certain effects occurring in fabricated transistors may not be accurately modeled (frequency deviations of up to 50 % from the nominal value can occur).



(a)



(b)

Fig. 9: Proposed CS-INV edge matching: a) Rising edge, b) Falling edge; X-axis represents the difference between simulated and required delay τ = 120.2 ps.

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