

Article

1-V Mixed-Mode Universal Filter Using Differential Difference Current Conveyor Transconductance Amplifiers

Montree Kumngern ¹, Fabian Khateb ^{2,3,*} and Tomasz Kulej ⁴

¹ Department of Telecommunications Engineering, School of Engineering, King Mongkut's Institute of Technology Ladkrabang, Bangkok 10520, Thailand; montree.ku@kmitl.ac.th

² Department of Microelectronics, Brno University of Technology, Technická 10, 601 90 Brno, Czech Republic

³ Department of Electrical Engineering, Brno University of Defence, Kounicova 65, 662 10 Brno, Czech Republic

⁴ Department of Electrical Engineering, Czestochowa University of Technology, 42-201 Czestochowa, Poland; kulej@el.pcz.czest.pl

* Correspondence: khateb@vutbr.cz

Abstract: This paper presents a mixed-mode universal filter using differential difference current conveyor transconductance amplifiers (DDCCTA). Despite using a minimum number of MOS differential pairs, the proposed DDCCTA is a multiple-input, multiple-output device, that was achieved using the multiple-input bulk-driven MOS transistor (MIBD-MOST) technique, multiple-output current followers and transconductance gains. A subthreshold technique is used to achieve minimum power consumption of the DDCCTA. Thanks to the multiple-input and multiple-output of DDCCTA, the mixed-mode universal filter based on the proposed element can realize five standard filter responses, i.e., low-pass, high-pass, band-pass, band-stop, and all-pass responses, of four modes, i.e., voltage-mode, current-mode, transadmittance-mode, and transimpedance-mode, thus providing 194 filter responses from a single circuit. The natural frequency and quality factor of the filter response can be controlled electronically and orthogonally. The proposed DDCCTA and mixed-mode universal filter are simulated and designed using 0.18 μm CMOS technology to confirm the functionality of the new circuit. The mixed-mode universal filter uses ± 0.5 V of supply voltage and consumes 0.374 mW of power when operating at a natural frequency of 10 kHz.

Keywords: differential difference current conveyor transconductance amplifier; active filter; analog integrated circuit; bulk-driven MOS transistor; low-voltage low-power



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1. Introduction

The current conveyor transconductance amplifier (CCTA) was introduced in [1,2]. This active building block incorporates the advantages of the second-generation current conveyor (CCII) [3], such as wide signal bandwidth, high linearity, wide dynamic range, and the advantages of the operational transconductance amplifier (OTA), such as electronic tuning capability, and its circuit is easy to implement as a single building block. However, the CCII, which is placed in the first stage of CCTA, has a single voltage input y , which requires additional passive resistors if addition/subtraction of voltage signals are required. Usually, to realize analog circuits such as filters or oscillators, feedforward and feedback techniques are used to create closed loop systems, that require an addition/subtraction function, especially for voltage-mode circuits. To address this limitation, a differential difference current conveyor transconductance amplifier (DDCCTA) was introduced [4]. This device has a differential difference current conveyor (DDCC) in the first stage, which is cascaded by OTA in the second stage. Thus, the DDCCTA has the voltage addition/subtraction property of the DDCC at the input (i.e., $V_x = V_{y1} - V_{y2} + V_{y3}$) and the transconductance property of the OTA at the output (i.e., $I_o = g_m V_x$). DDCCTA has been used to realize a number of analog circuits such as universal filters [4–8], sinusoidal wave oscillators [9,10], wave generator [11], memristor emulator [12] and many other. Unfortunately, the DDCCTA

structures applied in these applications are not designed to operate at low supply voltage and low power consumption, for example, the voltage supply is 2.5 V in [5], 4 V in [5,6,10], 1.8 V in [7,8], 3 V in [9]. Therefore, in this paper, it is interesting to present a DDCCTA that is able to operate with much lower supply voltage and low power consumption.

The mixed-mode universal filters are the circuits that can realize multiple modes of operation, i.e., voltage-mode (VM), current-mode (CM), transadmittance-mode (TAM) and transimpedance-modes (TIM), from the same topology, under appropriate conditions. If the transfer function is a voltage ratio, it can be classified as a VM filter, if the transfer function is a current ratio, it can be classified as a CM filter, if the input signal is a voltage and the output signal is a current, it operates as a TAM filter, and if the input signal is a current and the output signal is a voltage, it operates as a TIM filter. Therefore, the mixed-mode universal filter can be a useful interface between the voltage- and the current-mode blocks of an electronic system, without the need for additional voltage-to-current converter (V/I) and current-to-voltage converter (I/V) converters [13]. For full versatility of a mixed-mode universal filter, each mode should provide five standard filter responses, namely, a low-pass (LPF), high-pass (HPF), band-pass (BPF), band-stop (BSF), and all-pass (APF) responses. Thus, a mixed-mode universal filter can provide a total of 20 transfer functions in the same topology. In addition, it is desirable to have both non-inverting and inverting filter responses in each mode, which avoids additional inverting amplifiers from being required. Therefore, the versatile universal filter will provide 40 filter responses.

A number of versatile mixed-mode filters have been presented in the literature, based on various active devices, such as DDCC [13–15], four-terminal floating nullor (FTFN) [16], fully differential current conveyor (FDCCII) [17,18], differential voltage current conveyors (DVCC) [19,20], or current feedback operational amplifiers (CFOA) [21,22]. However, the natural frequency and/or quality factor of these filters cannot be electronically controlled, as it is required to compensate for process and temperature variations and is available for many other universal mixed-mode filters in the literature [23–46].

The electronic tunability of the filters was achieved using various tunable elements such as current-controlled second-generation current conveyor (CCCII) [23–25], OTA [26–32], voltage differencing transconductance amplifier (VDTA) [33], current-controlled current conveyor transconductance amplifier (CCCCTA) [34,35], modified current conveyor transconductance amplifier (MCCTA) [36], extra X current conveyor transconductance amplifier (EXCCTA) [37,38], voltage differencing extra X second generation current conveyor (VD-EXCCII) [39–41], voltage differencing buffered amplifier (VDBA) [42,43], voltage differencing differential voltage current conveyor (VD-DVCC) [44], differential difference transconductance amplifier (DDTA) [45,46], voltage differencing gain amplifier (VDGA) [47] and differential voltage current conveyor transconductance amplifier (DVCCTA) [48]. It should be noted that the above-mentioned filters do not provide non-inverting and inverting versions of the realized transfer functions. In addition, no mixed-mode universal filter using DDCCTA is available in the open literature.

In this paper, a new mixed-mode universal filter using DDCCTA is proposed. The DDCCTA offers full functionality in one compact structure. The circuit complexity and power consumption were decreased using the so-called MIBD-MOST technique. This technique also allows for obtaining a large input voltage range even for very low supply voltages. The same applies to a linear transconductor present in the structure of the proposed element, which was realized using the bulk-driven technique. Consequently, the proposed active element is well-suited for low-voltage and low-power applications.

In order to show the advantages of the proposed DDCCTA, it was used to realize a mixed-mode universal filter. The proposed filter provides 194 transfer functions of LPF, HPF, BPF, BSF, APF of VM, CM, TAM, and TIM into the same topology. The natural frequency and quality factor of the filters can be electronically and orthogonally controlled. The VM filter offers a high-input impedance, and the CM filter offers high-output impedance that simplifies cascade connections and allows for avoiding additional buffering stages. The proposed DDCCTA and the filter are simulated using SPICE and parameters of a 0.18 μm CMOS technology.

The paper is organized as follows: Section 2 presents the DDCCTA structure, realized using the MIBD-MOST technique, the proposed mixed-mode universal filters, and the non-ideality analysis. Section 3 shows the simulation results of the DDCCTA and the filter. Finally, Section 4 concludes the paper.

2. Proposed Circuit

2.1. The Multiple-Input DDCCTA

Figure 1a shows the CMOS implementation of the proposed DDCCTA, and Figure 2b shows its electrical symbol. The port characteristics of the ideal DDCCTA in Figure 2a can be given by

$$\left. \begin{aligned} V_x &= V_{y+1} + V_{y+2} - V_{y-1} - V_{y-2} \\ I_z &= I_x \\ I_{z\pm} &= I_x \\ I_{o\pm} &= \pm g_m (V_z - V_1) \end{aligned} \right\} \quad (1)$$

where g_m is the transconductance gain of the DDCCTA. This building block can provide multiple-input differential y - terminals, multiple-output plus/minus y - and o -terminals, compared to conventional DDCCTAs [4]. The multiple inputs of the DDCCTA can be implemented using the MIBD-MOST technique, as shown in Figure 2 [49]. Figure 2a shows the MIBD-MOST symbol and Figure 2b shows the implementation of the MIBD-MOST technique. In this technique, the input signal can be fed into the bulk-terminal (back-gate) of the MOS transistor.

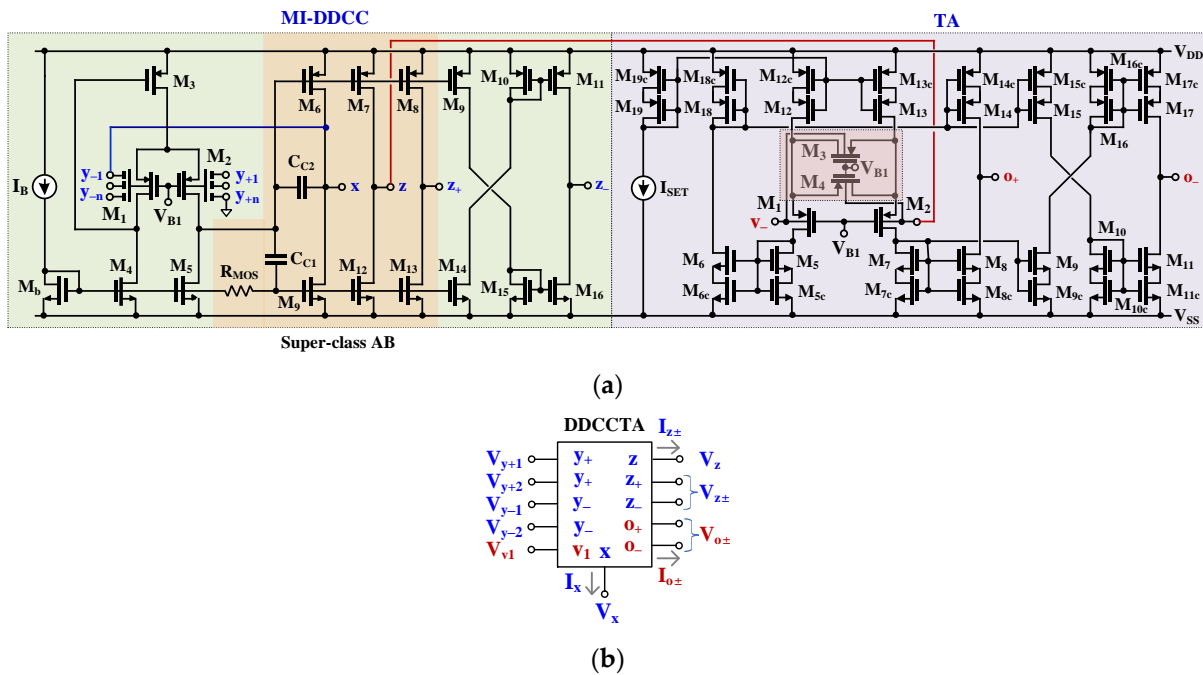


Figure 1. Proposed DDCCTA: (a) CMOS structure, (b) its electrical symbol.

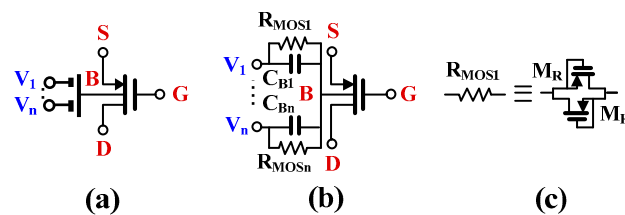


Figure 2. MIBD-MOST: (a) symbol, (b) implementation of MIBD-MOST, (c) implementation of large resistance RMOS.

The MIBD-MOST can be obtained by paralleling the $C_B(1-N)$ capacitances, which are shunted by large $R_{MOS}(1-N)$ resistances, as shown in Figure 2b. The large resistance R_{MOS} can be realized by antiparallel coupling of two MOSTs operating in the cut-off region, as shown in Figure 2c. The use of a parallel resistance R_{MOS} and capacitance C_B allows the MIBD-MOST to handle both DC and AC signals. The input capacitance C_B and the large resistance R_{MOS} create a high-pass filter at the input terminal with a very low cutoff frequency ≤ 1 Hz, therefore, its influence on the proposed application is negligible. The MOS differential pairs M_1, M_2 in Figure 1a will be implemented using this MIBD-MOST technique.

The operation of the proposed DDCCTA in Figure 1a can be explained by dividing it into two parts, DDCC and TA. The DDCC consists of transistors M_1-M_{16}, M_b, I_B . Transistors M_1, M_2 form a differential MOS pair, while transistors M_1, M_3 form a flipped voltage follower to achieve a minimum supply requirement, i.e., to keep V_{DD} as low as $V_{GS} + V_{DSsat}$, which is specially suitable for LV designs. The current sources M_4, M_5 act as loads for the input differential pair M_1, M_2 and also serve to supply the necessary quiescent current for M_1, M_2 . It should be noted that the MOS differential pairs M_1, M_2 are implemented using the MIBD-MOST technique and, therefore, increasing the number of input terminals will not increase the bias current and power consumption of the input differential pair, which is the main advantage of the MIBD-MOST technique.

To improve the power efficiency at the output stage, which consists of M_6, M_9, R_{MOS} , the super class-AB output stage from [50] is used. The drain voltage of M_2 controls the gate of M_6 and via capacitor C_{C1} the gate of M_9 . The quiescent current of M_9 is determined by the biasing current I_B , transistor M_b , and large resistor R_{MOS} . The large resistance R_{MOS} can be implemented as shown in Figure 2c. The capacitance C_{C1} and the large resistance R_{MOS} create a high-pass filter with a cutoff frequency of about 1 Hz. For AC signals with a frequency greater than 1 Hz, the AC voltages at the gates of M_9 and M_6 are nearly identical, therefore, class AB output stage operation is achieved. To compensate for the frequency characteristic of the two-stage internal amplifier, Miller frequency compensation was applied using the capacitance C_{C2} .

The voltage at the x-terminal, neglecting the impact of the common-mode rejection ratio (CMRR) limitation of the internal amplifier, can be expressed as

$$V_x = K_v(V_{y+1} + V_{y+2} - V_{y-1} - V_{y-2}) \quad (2)$$

The voltage gain K_v by assuming identical capacitances C_{C1} can be expressed as

$$K_v = \frac{\left(\frac{g_{mb1,2}}{3}\right) \left(\frac{r_{ds2}r_{ds5}}{r_{ds2}+r_{ds5}}\right) (g_{m6} + g_{m9})(r_{ds6} + r_{ds9})}{1 + \left(\frac{g_{mb1,2}}{3}\right) \left(\frac{r_{ds2}r_{ds5}}{r_{ds2}+r_{ds5}}\right) (g_{m6} + g_{m9})(r_{ds6} + r_{ds9})} \quad (3)$$

The transconductance of the transistors M_1 and M_2 expressed by (3) is divided by 3 due to the input capacitive divider. However, due to the two-stage structure of the internal op-amp, the value of K_v can be close to unity, with its gain error typically less than 1%. The resistance at the x-terminal can be expressed by

$$r_x = \frac{1}{\left(\frac{g_{mb1,2}}{3}\right) \left(\frac{r_{ds2}r_{ds5}}{r_{ds2}+r_{ds5}}\right) (g_{m6} + g_{m9})} \quad (4)$$

Because the gates of the transistors M_7, M_8, M_9 (M_{12}, M_{13}, M_{14}) are controlled with a voltage identical to the voltage at the gate of M_6 (M_9), the currents at the z_- and z_+ -terminal by neglecting second-order effects are equal to the current at the x-terminal. The minus-type output (z_- -terminal) of the DDCC can be obtained using the cross-coupled current mirrors

M₉, M₁₀, M₁₁ and M₁₃, M₁₄, M₁₆. Thus, the current I_x can be conveyed to the terminals z , z_+ , and z_- . The output resistances at the z -, z_+ -, z_- -terminals are expressed, respectively, by

$$\left. \begin{aligned} r_z &= \frac{r_{ds7} + r_{ds12}}{r_{ds7}r_{ds12}} \\ r_{z+} &= \frac{r_{ds8} + r_{ds13}}{r_{ds8}r_{ds13}} \\ r_{z-} &= \frac{r_{ds11} + r_{ds16}}{r_{ds11}r_{ds16}} \end{aligned} \right\} \quad (5)$$

The multiple-output z_+ , and z_- terminals can be obtained using multiple-output current mirrors.

The second building block of the proposed DDCCTA is the transconductance amplifier (TA). The circuit consists of a differential amplifier and current mirrors. The input differential stage of TA is realized using a linearized MOS differential transconductance amplifier operating in strong inversion, which was proposed in [51]. In this work, the same technique is modified to the input differential amplifier operating in weak inversion. This technique can improve the linearity of input differential pairs. The transistors M₃ and M₄ work as source degeneration resistors since they operate in a triode region with $V_{DS} = 0$ at the operating point. It should be noted that the gates of M₃ and M₄ are connected to the input terminals, thus this source degeneration resistor can operate as a voltage-controlled resistor to linearize the TA transconductance for a wider range of input voltages.

If the current mirrors around the input differential amplifier TA are identical and have unity current gain, the transconductance of TA can be expressed as follows

$$g_m = \frac{4k}{4k + 1} \cdot \frac{I_{SET}}{n_p U_T} \quad (6)$$

where n_p is the subthreshold slope factor for a p-channel transistor, U_T is the thermal potential (≈ 25 mV at 27 °C), I_{SET} is the biasing current, and k is the ratio of the aspect ratios of M_{3,4} to M_{1,2} given by

$$k = \frac{(W/L)_{3,4}}{(W/L)_{1,2}} \quad (7)$$

The coefficient k will affect the circuit linearity, and the optimum linearity can be achieved for $k = 0.5$ [52].

The self-cascode transistors are used in the current mirrors to obtain a larger output resistance of the circuit and consequently larger DC voltage gain of the transconductance amplifier. Using the self-cascode transistors, the voltage gain of the transconductance amplifier can be approximated as

$$A_v \cong g_{mb} \{ (g_{m8} r_{ds8} r_{ds8c}) || (g_{m14} r_{ds14} r_{ds14c}) \} \quad (8)$$

From (2), the output current I_o of the TA can be controlled by the difference of voltage at z -terminal (V_z) and the voltage V_1 . The minus-type output terminal o_- of the TA can be obtained using the cross-coupled current mirrors, and the multiple-output plus/minus o_{\pm} of the TA can be obtained using multiple-output current mirrors.

2.2. Proposed Mixed-Mode Universal Filter

Figure 3 shows the proposed second-order mixed-mode universal filter employing three DDCCTAs, two grounded capacitors, and three grounded resistors. The V_1 to V_7 are the input voltages, I_1 to I_5 are the input currents, V_{o1} to V_{o7} are the output voltages, and I_{o1} to I_{o6} are the output currents. Thanks to the multiple-input and the multiple-output of the DDCCTA, a multiple-input and a multiple-output of the mixed-mode universal filter can be achieved. It should be noted that the inputs V_1 to V_7 are applied to the high impedance level of the DDCCTAs while the outputs I_{o1} to I_{o6} are supplied from the high impedance level of the DDCCTAs. Thus, the proposed mixed-mode universal filter offers high-input impedance of voltage input terminals, and high-output impedance of current

output terminals, which is required for VM and CM circuits. Under appropriate conditions, many filtering functions can be obtained.

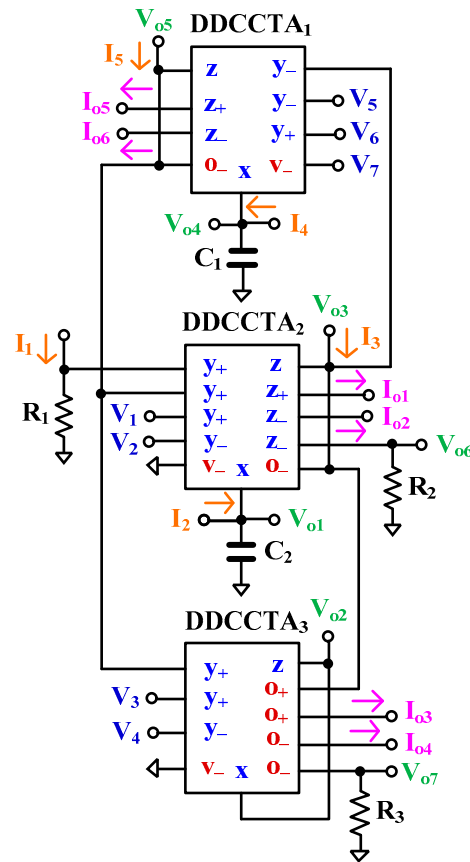


Figure 3. Proposed mixed-mode universal filter using DDCCTAs.

If V_1 to V_7 are the input voltages and V_{o1} to V_{o7} are the output voltages, the circuit can work as a VM filter. Using nodal analysis and (1), the outputs V_{o1} to V_{o7} can be expressed, respectively, by

$$V_{o1} = \frac{\left\{ (sC_1g_{m3} + g_{m1}g_{m2})(V_1 - V_2) + sC_1g_{m3}(V_4 - V_3) \right\} + sC_1g_{m2}(V_6 - V_5) + g_{m1}g_{m2}V_7}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (9)$$

$$V_{o2} = \frac{\left\{ s^2C_1C_2(V_2 - V_1) + (s^2C_1C_2 + g_{m1}g_{m2})(V_3 - V_4) \right\} + sC_1g_{m2}(V_6 - V_5) + g_{m1}g_{m2}V_7}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (10)$$

$$V_{o3} = \frac{\left\{ sC_2g_{m1}(V_1 - V_2) + g_{m1}g_{m2}(V_3 - V_4) \right\} + (s^2C_1C_2 + sC_1g_{m3})(V_6 - V_5) + (sC_2g_{m1} + g_{m1}g_{m3})V_7}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (11)$$

$$V_{o4} = \frac{\left\{ sC_2g_{m1}(V_2 - V_1) + g_{m1}g_{m3}(V_4 - V_3) + g_{m1}g_{m2}(V_6 - V_5) \right\} - (sC_2g_{m1} + g_{m1}g_{m3})V_7}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (12)$$

$$V_{o5} = \frac{\left\{ s^2C_1C_2(V_2 - V_1) + sC_1g_{m3}(V_4 - V_3) + sC_1g_{m2}(V_6 - V_5) \right\} + g_{m1}g_{m2}V_7}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (13)$$

$$V_{o6} = \frac{\left\{ \begin{array}{l} (s^2C_1C_2g_{m3}R_2 + sC_2g_{m1}g_{m2}R_2)(V_2 - V_1) \\ +s^2C_1C_2g_{m3}R_2(V_3 - V_4) + s^2C_1C_2g_{m2}R_2(V_5 - V_6) \\ -sC_2g_{m1}g_{m2}R_2V_7 \end{array} \right\}}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (14)$$

$$V_{o7} = \frac{\left\{ \begin{array}{l} s^2C_1C_2g_{m3}R_3(V_1 - V_2) \\ + (s^2C_1C_2g_{m3}R_3 + g_{m1}g_{m2}g_{m3}R_3)(V_4 - V_3) \\ +sC_1g_{m2}g_{m3}R_3(V_5 - V_6) - g_{m1}g_{m2}g_{m3}R_3V_7 \end{array} \right\}}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (15)$$

If V_1 to V_7 are the input voltages and I_{o1} to I_{o6} are the output currents, the circuit can work as a TAM filter. Using nodal analysis and (1), the outputs I_{o1} to I_{o6} can be expressed, respectively, by

$$I_{o1} = \frac{\left\{ \begin{array}{l} (s^2C_1C_2g_{m3} + sC_2g_{m1}g_{m2})(V_1 - V_2) + s^2C_1C_2g_{m3}(V_4 - V_3) \\ +s^2C_1C_2g_{m2}(V_6 - V_5) + sC_2g_{m1}g_{m2}V_7 \end{array} \right\}}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (16)$$

$$I_{o2} = \frac{\left\{ \begin{array}{l} (s^2C_1C_2g_{m3} + sC_2g_{m1}g_{m2})(V_2 - V_1) + s^2C_1C_2g_{m3}(V_3 - V_4) \\ +s^2C_1C_2g_{m2}(V_5 - V_6) - sC_2g_{m1}g_{m2}V_7 \end{array} \right\}}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (17)$$

$$I_{o3} = \frac{\left\{ \begin{array}{l} s^2C_1C_2g_{m3}(V_2 - V_1) + (s^2C_1C_2g_{m3} + g_{m1}g_{m2}g_{m3})(V_3 - V_4) \\ +sC_1g_{m2}g_{m3}(V_6 - V_5) + g_{m1}g_{m2}g_{m3}V_7 \end{array} \right\}}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (18)$$

$$I_{o4} = \frac{\left\{ \begin{array}{l} s^2C_1C_2g_{m3}(V_1 - V_2) + (s^2C_1C_2g_{m3} + g_{m1}g_{m2}g_{m3})(V_4 - V_3) \\ +sC_1g_{m2}g_{m3}(V_5 - V_6) - g_{m1}g_{m2}g_{m3}V_7 \end{array} \right\}}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (19)$$

$$I_{o5} = \frac{\left\{ \begin{array}{l} s^2C_1C_2g_{m1}(V_2 - V_1) + sC_1g_{m1}g_{m3}(V_4 - V_3) \\ +sC_1g_{m2}g_{m1}(V_6 - V_5) - (s^2C_1C_2g_{m1} + sC_1g_{m1}g_{m3})V_7 \end{array} \right\}}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (20)$$

$$I_{o6} = \frac{\left\{ \begin{array}{l} s^2C_1C_2g_{m1}(V_1 - V_2) + sC_1g_{m1}g_{m3}(V_3 - V_4) \\ +sC_1g_{m2}g_{m1}(V_5 - V_6) + (s^2C_1C_2g_{m1} + sC_1g_{m1}g_{m3})V_7 \end{array} \right\}}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (21)$$

If I_1 to I_5 are the input currents, and I_{o1} to I_{o6} are the output currents, the circuit can work as a CM filter. Using nodal analysis and (1), the outputs I_{o1} to I_{o6} can be expressed, respectively, by

$$I_{o1} = \frac{\left\{ \begin{array}{l} -(s^2C_1C_2g_{m3}R_1 + sC_2g_{m1}g_{m2}R_1)I_1 \\ +(sC_1g_{m3} + g_{m1}g_{m2})I_2 + s^2C_1C_2I_3 + sC_2g_{m2}(I_4 - I_5) \end{array} \right\}}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (22)$$

$$I_{o2} = \frac{\left\{ \begin{array}{l} (s^2C_1C_2g_{m3}R_1 + sC_2g_{m1}g_{m2}R_1)I_1 - (sC_1g_{m3} + g_{m1}g_{m2})I_2 \\ -s^2C_1C_2I_3 + sC_2g_{m2}(I_5 - I_4) \end{array} \right\}}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (23)$$

$$I_{o3} = \frac{s^2C_1C_2g_{m3}R_1I_1 + sC_1g_{m3}(I_3 - I_2) + g_{m2}g_{m3}(I_4 - I_5)}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (24)$$

$$I_{o4} = \frac{-s^2C_1C_2g_{m3}R_1I_1 + sC_1g_{m3}(I_2 - I_3) + g_{m2}g_{m3}(I_5 - I_4)}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (25)$$

$$I_{o5} = \frac{\left\{ \begin{array}{l} s^2C_1C_2g_{m3}R_1I_1 + sC_1g_{m3}(I_3 - I_2) + g_{m1}g_{m2}I_4 \\ +(s^2C_1C_2 + sC_1g_{m3})I_5 \end{array} \right\}}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (26)$$

$$I_{o6} = \frac{\left\{ \begin{array}{l} -s^2C_1C_2g_{m3}R_1I_1 + sC_1g_{m3}(I_2 - I_3) - g_{m1}g_{m2}I_4 \\ -(s^2C_1C_2 + sC_1g_{m3})I_5 \end{array} \right\}}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (27)$$

If I_1 to I_5 are the input currents, and V_{o1} to V_{o7} are the output voltages, the circuit can work as a TIM filter. Using nodal analysis and (1), the outputs V_{o1} to V_{o7} can be expressed, respectively, by

$$V_{o1} = \frac{-(sC_1g_{m3}R_1 + g_{m1}g_{m2}R_1)I_1 + sC_1(I_3 - I_2) + g_{m2}(I_4 - I_5)}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (28)$$

$$V_{o2} = V_{o5} = \frac{s^2C_1g_{m3}R_1I_1 + sC_1(I_3 - I_2) + g_{m3}(I_4 - I_5)}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (29)$$

$$V_{o3} = \frac{-sC_1g_{m3}R_1I_1 + g_{m1}(I_2 - I_3) + (sC_2 + g_{m3})(I_4 - I_5)}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (30)$$

$$V_{o4} = \frac{sC_1g_{m3}R_1I_1 + g_{m2}(I_3 - I_2) + (sC_2 + g_{m3})(I_5 - I_4)}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (31)$$

$$V_{o6} = \frac{\left\{ \begin{array}{l} (s^2C_1C_2g_{m3}R_1R_2 + sC_2g_{m1}g_{m2}R_1R_2)I_1 \\ -(sC_1g_{m3}R_2 + g_{m1}g_{m2}R_2)I_2 \\ -s^2C_1C_2R_2I_3 + sC_2g_{m2}R_2(I_5 - I_4) \end{array} \right\}}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (32)$$

$$V_{o7} = \frac{\left\{ \begin{array}{l} -s^2C_1C_2g_{m3}R_1R_3I_1 + sC_1g_{m3}R_3(I_2 - I_3) \\ +g_{m2}g_{m3}R_3(I_5 - I_4) \end{array} \right\}}{s^2C_1C_2 + sC_1g_{m3} + g_{m1}g_{m2}} \quad (33)$$

It is evident that the proposed mixed-mode universal filter offers many transfer functions of LPF, HPF, BPF, BSP, APF, both non-inverting and inverting transfer functions. Tables 1 and 2, Appendices A and B, VM, CM, TAM, and TIM can provide, respectively, 66, 40, 61, and 27 transfer functions. It should be noted that the voltage gain and transadmittance gain of the transfer functions can be obtained if the V_{o6} and V_{o7} are used for the outputs.

Table 1. Obtaining variant filtering functions of the VM filter.

	Filtering Function	Input	Output	Condition
LPF	Non-inverting	V_7	V_{o1}	-
	Non-inverting	$V_1 = V_3$	V_{o1}	-
	Inverting	$V_2 = V_4$	V_{o1}	-
	Non-inverting	V_7	V_{o2}	-
	Non-inverting	$V_1 = V_3$	V_{o2}	-
	Inverting	$V_2 = V_4$	V_{o2}	-
	Non-inverting	V_3	V_{o3}	-
	Inverting	V_4	V_{o3}	-
	Non-inverting	$V_2 = V_7$	V_{o3}	-
	Non-inverting	V_6	V_{o4}	-
	Inverting	V_5	V_{o4}	-
	Non-inverting	V_4	V_{o4}	$g_{m2} = g_{m3}$
	Inverting	V_3	V_{o4}	$g_{m2} = g_{m3}$

Table 1. Cont.

Filtering Function		Input	Output	Condition
LPF	Inverting	$V_2 = V_7$	V_{o4}	$g_{m2} = g_{m3}$
	Non-inverting	V_7	V_{o5}	-
	Inverting	V_7	V_{o7}	-
	Inverting	$V_1 = V_3$	V_{o7}	-
	Non-inverting	$V_2 = V_4$	V_{o7}	-
HPF	Non-inverting	V_2	V_{o2}	-
	Inverting	V_1	V_{o2}	-
	Non-inverting	V_2	V_{o5}	-
	Inverting	V_1	V_{o5}	-
	Non-inverting	V_3	V_{o6}	-
	Inverting	V_5	V_{o6}	-
	Non-inverting	V_5	V_{o6}	-
	Inverting	V_6	V_{o6}	-
	Non-inverting	$V_2 = V_7$	V_{o6}	-
	Non-inverting	V_1	V_{o7}	-
	Inverting	V_2	V_{o7}	-
	Non-inverting	$V_4 = V_7$	V_{o7}	-
	Non-inverting	V_4	V_{o1}	-
	Inverting	V_3	V_{o1}	-
	Non-inverting	V_6	V_{o1}	$g_{m2} = g_{m3}$
Inverting	V_5	V_{o1}	$g_{m2} = g_{m3}$	
Inverting	$V_2 = V_7$	V_{o1}	-	
Non-inverting	V_6	V_{o2}	$g_{m2} = g_{m3}$	
Inverting	V_5	V_{o2}	$g_{m2} = g_{m3}$	
Non-inverting	V_1	V_{o3}	$g_{m1} = g_{m3}$	
Inverting	V_2	V_{o3}	$g_{m1} = g_{m3}$	
Non-inverting	$V_4 = V_7$	V_{o3}	$g_{m1} = g_{m2} = g_{m3}$	
Non-inverting	V_2	V_{o4}	$g_{m1} = g_{m3}$	
Inverting	V_1	V_{o4}	$g_{m1} = g_{m3}$	
Inverting	$V_4 = V_7$	V_{o4}	$g_{m1} = g_{m3}$	
Non-inverting	V_4	V_{o5}	-	
Inverting	V_3	V_{o5}	-	
Non-inverting	V_6	V_{o5}	$g_{m2} = g_{m3}$	
Inverting	V_5	V_{o5}	$g_{m2} = g_{m3}$	
Inverting	V_7	V_{o6}	$g_{m1} = g_{m3}$	
Non-inverting	$V_2 = V_4$	V_{o6}	$g_{m1} = g_{m3}$	
Inverting	$V_1 = V_3$	V_{o6}	$g_{m1} = g_{m3}$	
Non-inverting	V_5	V_{o7}	-	
Inverting	V_6	V_{o7}	-	

Table 1. *Cont.*

Filtering Function		Input	Output	Condition
BSF	Non-inverting	V_3	V_{o2}	-
	Inverting	V_4	V_{o2}	-
	Non-inverting	$V_2 = V_7$	V_{o2}	-
	Non-inverting	$V_2 = V_7$	V_{o5}	-
	Non-inverting	V_4	V_{o7}	-
	Inverting	V_3	V_{o7}	-
	Non-inverting	$V_2 = V_7$	V_{o2}	-
APF	Non-inverting	$V_3 = V_5$	V_{o2}	$g_{m2} = g_{m3}$
	Inverting	$V_4 = V_6$	V_{o2}	$g_{m2} = g_{m3}$
	Non-inverting	$V_2 = V_3 = V_7$	V_{o5}	-
	Non-inverting	$V_2 = V_5 = V_7$	V_{o5}	-
	Non-inverting	$V_4 = V_6$	V_{o7}	-
	Inverting	$V_3 = V_5$	V_{o7}	-
	Inverting	$V_2 = V_5 = V_7$	V_{o7}	-

Table 2. Obtaining variant filtering functions of the CM filter.

Filtering Function		Input	Output	Condition
LPF	Non-inverting	$I_2 = I_5$	I_{o1}	$g_{m2} = g_{m3}, C_1 = C_2$
	Inverting	$I_2 = I_5$	I_{o2}	$g_{m2} = g_{m3}, C_1 = C_2$
	Non-inverting	I_4	I_{o3}	-
	Inverting	I_5	I_{o3}	-
	Non-inverting	I_5	I_{o4}	-
	Inverting	I_4	I_{o4}	-
	Non-inverting	I_4	I_{o5}	-
	Inverting	I_4	I_{o6}	-
	Non-inverting	I_2	$I_{o1} + I_{o3}$	-
	HPF	Non-inverting	I_3	I_{o1}
Inverting		I_3	I_{o2}	-
Non-inverting		I_1	I_{o3}	Gain ($g_{m3}R_1$)
Inverting		I_1	I_{o4}	Gain ($g_{m3}R_1$)
Non-inverting		I_1	I_{o5}	Gain ($g_{m3}R_1$)
Inverting		I_1	I_{o6}	Gain ($g_{m3}R_1$)
Inverting		I_5	$I_{o1} + I_{o6}$	$g_{m2} = g_{m3}, C_1 = C_2$
Inverting		I_5	$I_{o2} + I_{o5}$	$g_{m2} = g_{m3}, C_1 = C_2$
BPF		Non-inverting	I_4	I_{o1}
	Inverting	I_5	I_{o1}	-
	Non-inverting	I_5	I_{o2}	-
	Inverting	I_4	I_{o2}	-

Table 2. Cont.

	Filtering Function	Input	Output	Condition
BPF	Non-inverting	I_3	I_{o3}	-
	Inverting	I_2	I_{o3}	-
	Non-inverting	I_2	I_{o4}	-
	Inverting	I_3	I_{o4}	-
	Non-inverting	I_3	I_{o5}	-
	Inverting	I_2	I_{o5}	-
	Non-inverting	I_2	I_{o6}	-
	Inverting	I_3	I_{o6}	-
	Inverting	I_1	$I_{o1} + I_{o3}$	-
	Non-inverting	I_1	$I_{o2} + I_{o4}$	-
BSF	Non-inverting	$I_1 = I_4$	I_{o3}	$g_{m3} = 1/R_1$
	Inverting	$I_1 = I_4$	I_{o4}	$g_{m3} = 1/R_1$
	Non-inverting	$I_1 = I_4$	I_{o5}	-
	Inverting	$I_1 = I_4$	I_{o6}	-
APF	Non-inverting	$I_1 = I_2 = I_4$	I_{o3}	$g_{m3} = 1/R_1$
	Inverting	$I_1 = I_2 = I_4$	I_{o4}	$g_{m3} = 1/R_1$
	Non-inverting	$I_1 = I_2 = I_4$	I_{o5}	-
	Inverting	$I_1 = I_2 = I_4$	I_{o6}	-

The natural frequency (ω_o), bandwidth (BW), and quality factor (Q) of the filters can be expressed, respectively, by

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{34}$$

$$BW = \frac{g_{m3}}{C_2} \tag{35}$$

$$Q = \frac{1}{g_{m3}} \sqrt{\frac{g_{m1}g_{m2}C_2}{C_1}} \tag{36}$$

The parameter ω_o can be controlled electronically by g_{m1} and g_{m2} , parameters BW and Q can be controlled electronically by g_{m3} . Thus, parameters ω_o and Q can be orthogonally controlled.

2.3. Non-Ideality Analysis

A non-ideal DDCCTA can be characterized by

$$\left. \begin{aligned} V_x &= \beta_{+j}(V_{y+1} + V_{y+2}) - \beta_{-j}(V_{y-1} + V_{y-2}) \\ I_{z\pm} &= \alpha_{\pm j}I_x \\ I_{o\pm} &= \pm g_{mnj}(V_z - V_1) \end{aligned} \right\} \tag{37}$$

where β_{+j} and β_{-j} are the non-ideal voltage gains between y_{+-} , y_{y--} and x -terminals, $\alpha_{z\pm j}$ is the non-ideal current gain between x - and z -terminals, g_{mnj} is the non-ideal transconductance gain of j th DDCCTA. Ideally, these gains are a unity, and in practice, they are slightly less than one. For the non-ideal voltage and current gains for the circuit operates at

frequencies much less than the corner frequencies of the DDCC, which is the first stage of DDCCCTA, these non-ideal gains can be expressed by [13]

$$\left. \begin{aligned} \beta_{\pm j}(s) &= 1 - \varepsilon_{v\pm j} \\ \alpha_{\pm j}(s) &= 1 - \varepsilon_{i\pm j} \end{aligned} \right\} \quad (38)$$

where $\varepsilon_{v\pm j} (|\varepsilon_{v\pm j}| \ll 1)$ and $\varepsilon_{i\pm j} (|\varepsilon_{i\pm j}| \ll 1)$ are, respectively, the voltage and current tracking errors of j th DDCCCTA.

The frequency-dependent transconductance gain g_{mn} of the OTA, which is the second stage of the DDCCCTA when the circuit works at frequencies much less than the cut-off frequency of the OTA, can be given by [53]

$$g_{mn}(s) \cong g_m(1 - \mu s) \quad (39)$$

where $\mu = 1/\omega_g$ and ω_g is the first pole frequency of the g_m .

Using (38) and (39), the denominator ($D(s)$) of the transfer functions can be expressed by

$$\begin{aligned} D(s) = & \left\{ s^2 C_1 C_2 \beta_{-1} \alpha_{+1} \alpha_{+2} \left(1 - \frac{C_1 g_{m3} \beta_{-1} \beta_{+3} \alpha_{+1} \alpha_{+3} \mu_3 - g_{m1} g_{m2} \mu_1 \mu_2}{C_1 C_2 \beta_{-1} \alpha_{+1} \alpha_{+2}} \right) \right. \\ & + s C_1 g_{m3} \beta_{-1} \beta_{+3} \alpha_{+1} \alpha_{+3} \left(1 - \frac{g_{m1} g_{m2} \mu_1 - g_{m1} g_{m2} \mu_2}{C_1 g_{m3} \beta_{-1} \beta_{+3} \alpha_{+1} \alpha_{+3}} \right) \\ & \left. + g_{m1} g_{m2} \right\} \end{aligned} \quad (40)$$

The non-idealities of transconductance amplifiers can be made negligible by satisfying the following condition

$$\left. \begin{aligned} \frac{C_1 g_{m3} \mu_3 - g_{m1} g_{m2} \mu_1 \mu_2}{C_1 C_2} &\ll 1 \\ \frac{g_{m1} g_{m2} \mu_1 + g_{m1} g_{m2} \mu_2}{C_1 g_{m3}} &\ll 1 \end{aligned} \right\} \quad (41)$$

The non-ideal values of the natural frequency (ω_{on}), the bandwidth (BW_n), and the quality factor (Q_n) can be expressed by

$$\omega_{on} = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2 \beta_{-1} \alpha_{+1} \alpha_{+2}}} \quad (42)$$

$$BW_n = \frac{g_{m3} \beta_{+3} \alpha_{+3}}{C_2 \alpha_{+2}} \quad (43)$$

$$Q_n = \frac{1}{g_{m3} \beta_{+3} \alpha_{+3}} \sqrt{\frac{g_{m1} g_{m2} C_2 \alpha_{+2}}{C_1 \beta_{-1} \alpha_{+1}}} \quad (44)$$

The voltage and current tracking errors will slightly change the values of natural frequency, bandwidth, and quality factor.

3. Simulation Results

The proposed DDCCCTA and mixed-mode universal filter was simulated in SPICE using 0.18 μm CMOS technology to show its performance. The aspect ratios of MOS transistors and capacitance values are shown in Table 3. The power supplies were given as $V_{DD} = -V_{SS} = 0.5 \text{ V}$, $I_B = 5 \mu\text{A}$, $V_B = -0.3 \text{ V}$.

The performance of the proposed DDCCCTA was investigated. Figure 4 shows the DC transfer characteristics when the input voltage V_y was varied and the output voltage V_x is investigated. Figure 4a,b show, respectively, the input voltage swings between V_{y+} and V_x and its voltage error, and between V_{y-} and V_x and its voltage error. Thanks to the BD-MOST technique, the rail-to-rail input voltage swings were achieved for a supply voltage of only $\pm 0.5 \text{ V}$.

Table 3. Transistor aspect ratios and capacitance values of the DDCCTA.

DDCC	W/L ($\mu\text{m}/\mu\text{m}$)	TA	W/L ($\mu\text{m}/\mu\text{m}$)
M_1, M_2	30/0.5	M_1, M_2	60/1
M_3	13/0.3	M_3, M_4	15/1
M_4, M_5, M_b	12/3	M_5-M_{11}	20/1
M_6-M_{11}	50/2	$M_{5c}-M_{11c}$	10/1
M_9-M_{16}	24/3	$M_{12}-M_{19}$	30/1
M_R	4/5	$M_{12c}-M_{19c}$	15/1
Capacitor: $C_{C1} = C_{C2} = 2.6 \text{ pF}$, $C_B = 0.5 \text{ pF}$			

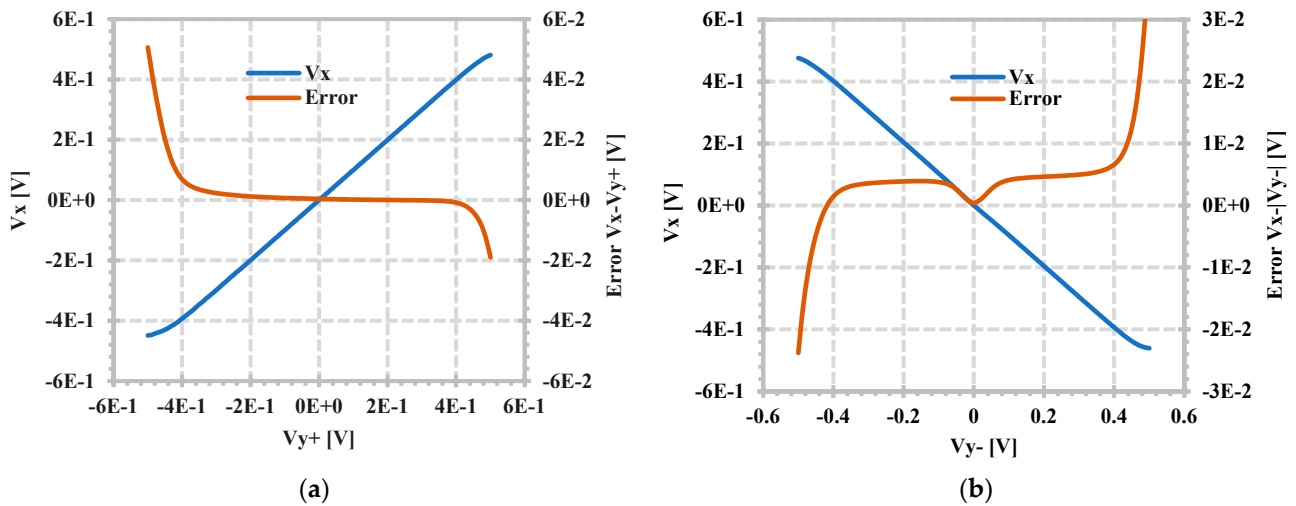


Figure 4. DC transfer characteristics: (a) V_x against V_{y+} and its error, (b) V_x against V_{y-} and its error.

The transconductance characteristic with different setting currents, I_{set} , is shown in Figure 5. Figure 5a,b show, respectively, the DC and AC characteristics, when I_{set} was changed to $[2,4,6,8,10,12,14] \mu\text{A}$. Figure 6 shows the simulated impedances at the x-, z-, and o-terminals of the DDCCTA. From this result, the resistances at the x-, z-, and o-terminals were, respectively, $1.5 \text{ k}\Omega$, $900 \text{ k}\Omega$, and $4.71 \text{ M}\Omega$, whereas the parasitic capacitances at the o- and z-terminals were 0.197 pF and 0.297 pF , respectively.

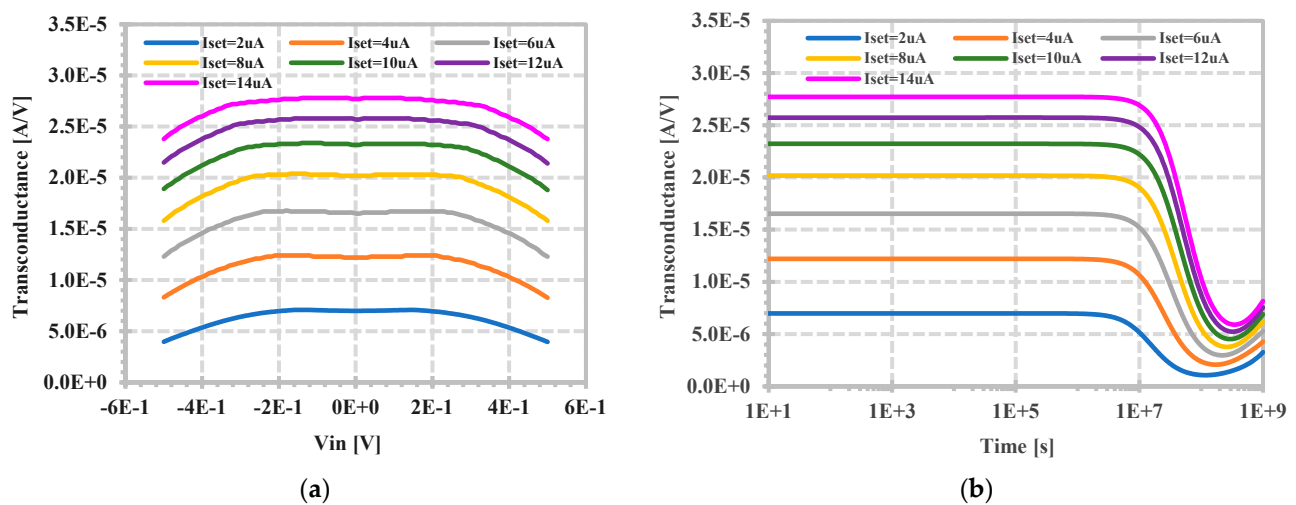


Figure 5. Simulated transconductance characteristic with different setting currents: (a) DC characteristic, (b) AC characteristic.

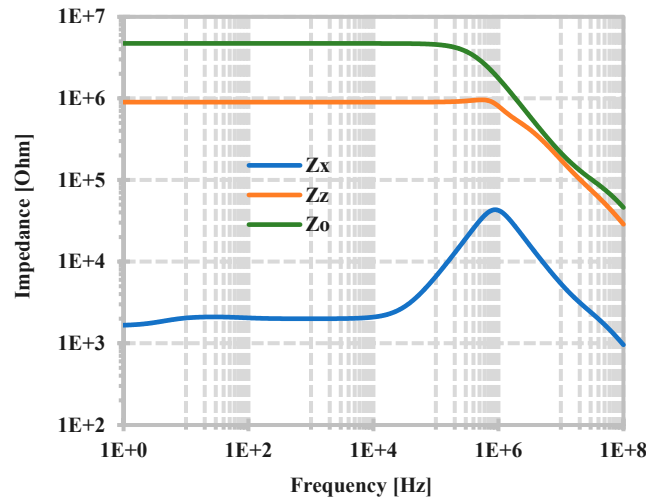


Figure 6. The parasitic impedances at x-, z- and o-terminals of the DDCCTA.

The proposed mixed-mode universal filter was designed and simulated. The capacitance values of C_1 and C_2 were 0.26 nF. In the first case, the setting currents $I_{set1,2,3}$ were set to 5 μ A. Figure 7a shows the simulated frequency magnitude responses of LPF, HPF, BPF, and BSF, and Figure 7b shows the simulated frequency magnitude and phase responses of the APF of the VM filter. The filter consumes 374 μ W of power and provides 10 kHz of the natural frequency.

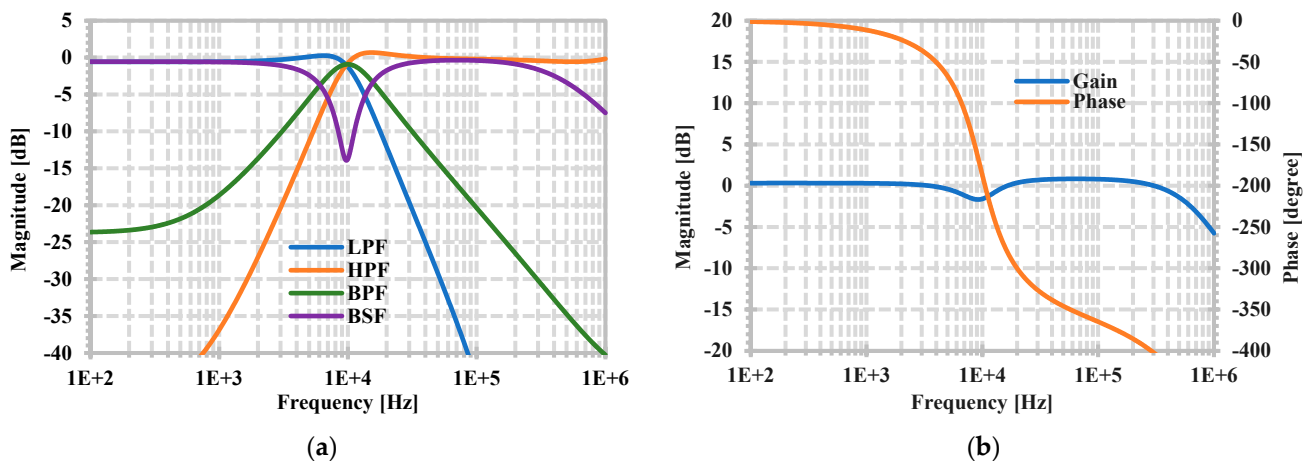


Figure 7. The simulated magnitude and phase frequency responses of VM for: (a) LPF, HPF, BPF, BSP, (b) APF.

Figures 8a, 9a and 10a show, respectively, the simulated frequency magnitude responses (LPF, HPF, BPF, and BSF) of CM, TAM, and TIM, while Figures 8b, 9b and 10b show, respectively, the simulated frequency magnitude and phase responses of CM, TAM, and TIM for APF. Figures 7–10 confirm that the proposed circuit can work as a mixed-mode universal filter.

To confirm that the natural frequency and the quality factor can be electronically controlled, the BPF of VM was selected for a simulation.

Figure 11a shows the frequency magnitude responses of the BPF when the setting currents I_{set} ($I_{set1} = I_{set1} = I_{set2}$) were changed to [1.5, 3.0, 5.0, 10] μ A. The natural frequencies were changed to [4.36, 6.99, 10, 15] kHz when the setting currents I_{set} were changed to [1.5, 3.0, 5.0, 10] μ A, respectively. Figure 11b shows the quality factor that was changed by the setting current I_{set3} of [0.5, 1.0, 2.0, 5] μ A. Thus, the simulated frequency magnitude responses in Figure 11 can be used to confirm that the electronic tuning capability as well as the orthogonally control of parameters ω_o and the Q of the filter can be achieved.

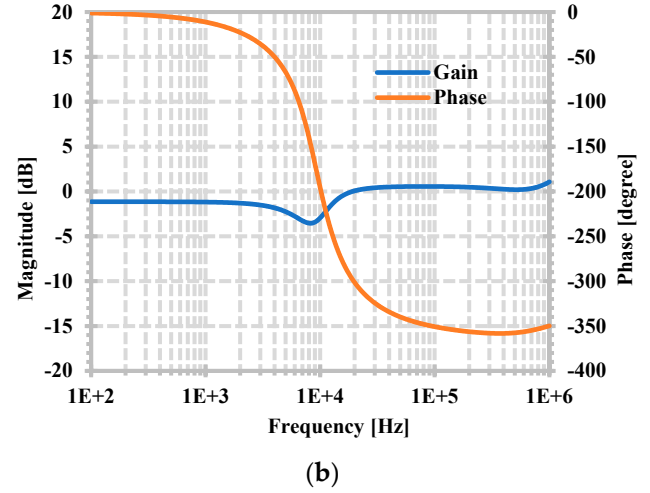
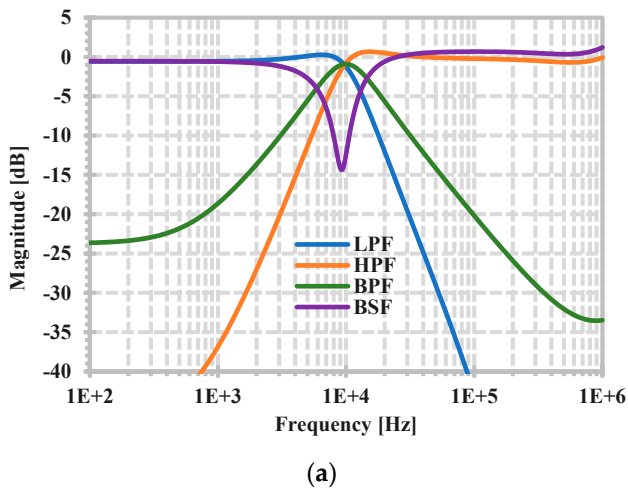


Figure 8. The simulated magnitude and phase frequency responses of CM for: (a) LPF, HPF, BPF, BSP, (b) APF.

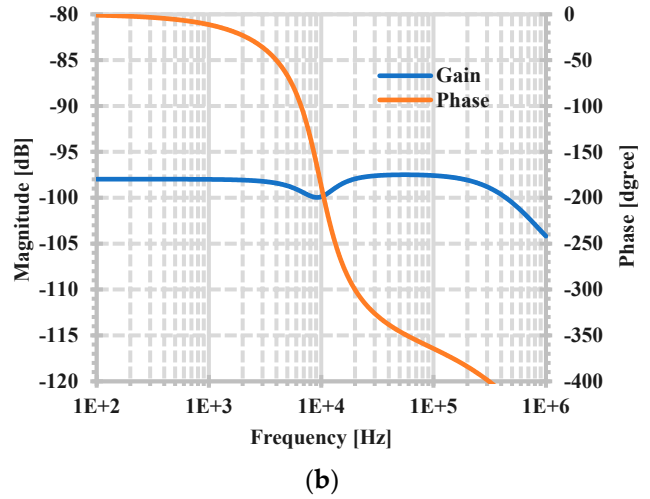
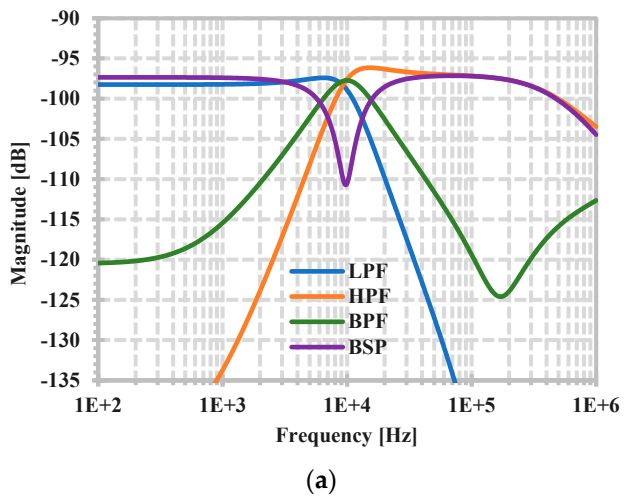


Figure 9. The simulated magnitude and phase frequency responses of TAM for: (a) LPF, HPF, BPF, BSP, (b) APF.

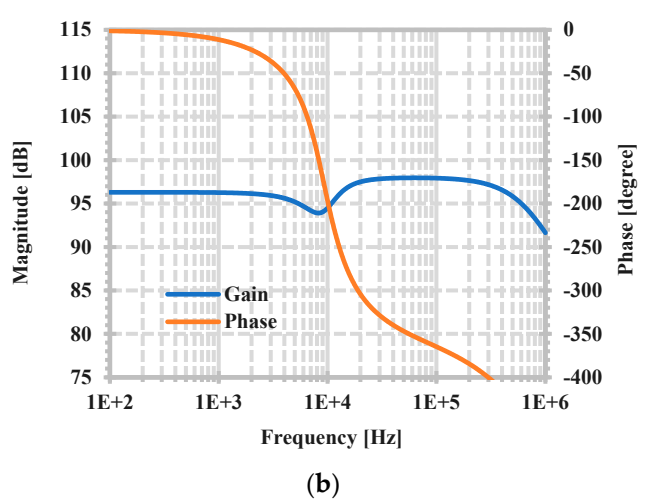
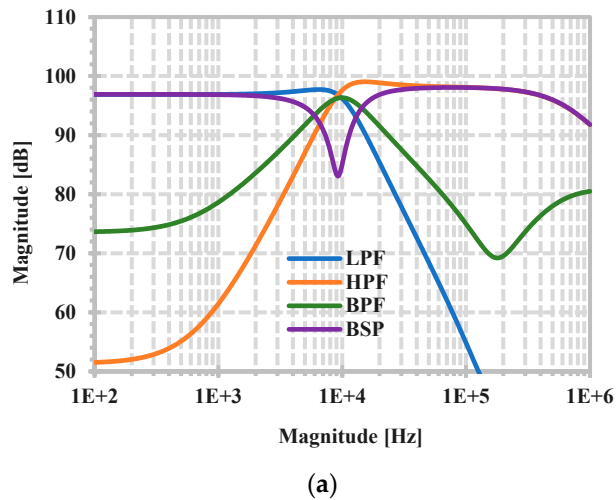


Figure 10. The simulated magnitude and phase frequency responses of TIM for: (a) LPF, HPF, BPF, BSP, (b) APF.

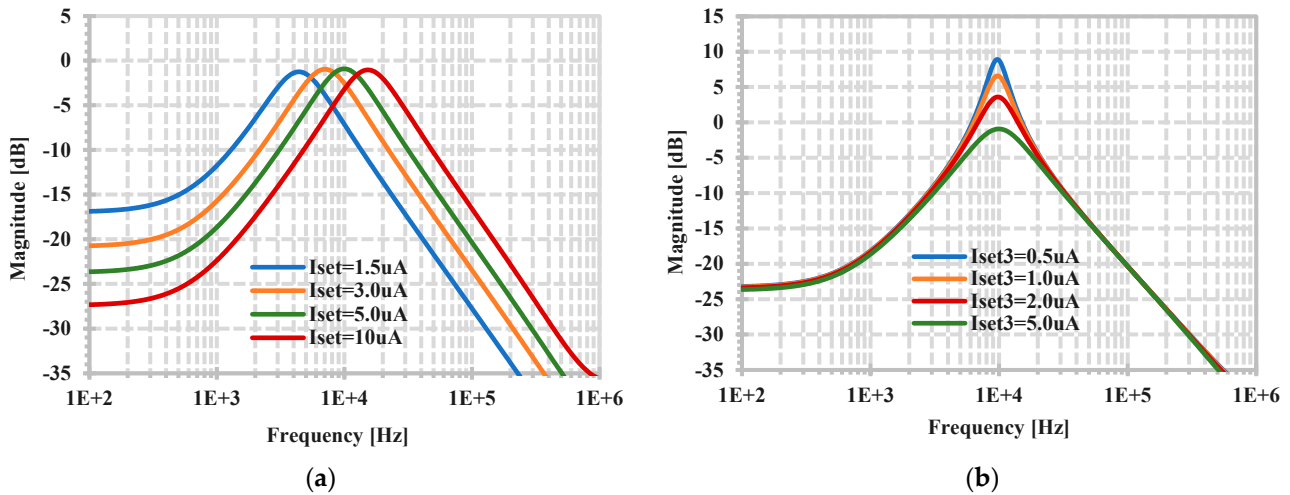


Figure 11. The simulated frequency response of BPF for: (a) the natural frequency was varied by I_{set} ($I_{set} = I_{set1} = I_{set2}$), (b) the quality factor was varied by I_{set3} .

The proposed mixed-mode universal filter performance was tested in the case of the process, supply voltage, and temperature variations. In this case, a BPF of both VM and CM was selected for testing. Figure 12 shows the Monte-Carlo analysis using 200 runs of the frequency magnitude responses with 5% variations of the transistor threshold voltage. The selected frequency magnitude responses of VM, and CM are shown in Figure 12a,b, respectively. Figure 13a,b show, respectively, the BPF’s magnitude frequency responses of the VM and CM when the power supply was changed to 0.9 V, 1 V, and 1.1 V. Figure 14a,b show, respectively, the BPF’s magnitude frequency responses of the VM and CM when the temperatures were changed to $-25\text{ }^\circ\text{C}$, $0\text{ }^\circ\text{C}$, $27\text{ }^\circ\text{C}$, and $75\text{ }^\circ\text{C}$. From this result, at a temperature of $27\text{ }^\circ\text{C}$, the center frequency was 10 kHz, and was changed by 18.8%, 9.6%, and 14.9% when the temperature was changed to $-25\text{ }^\circ\text{C}$, $0\text{ }^\circ\text{C}$, and $75\text{ }^\circ\text{C}$, respectively.

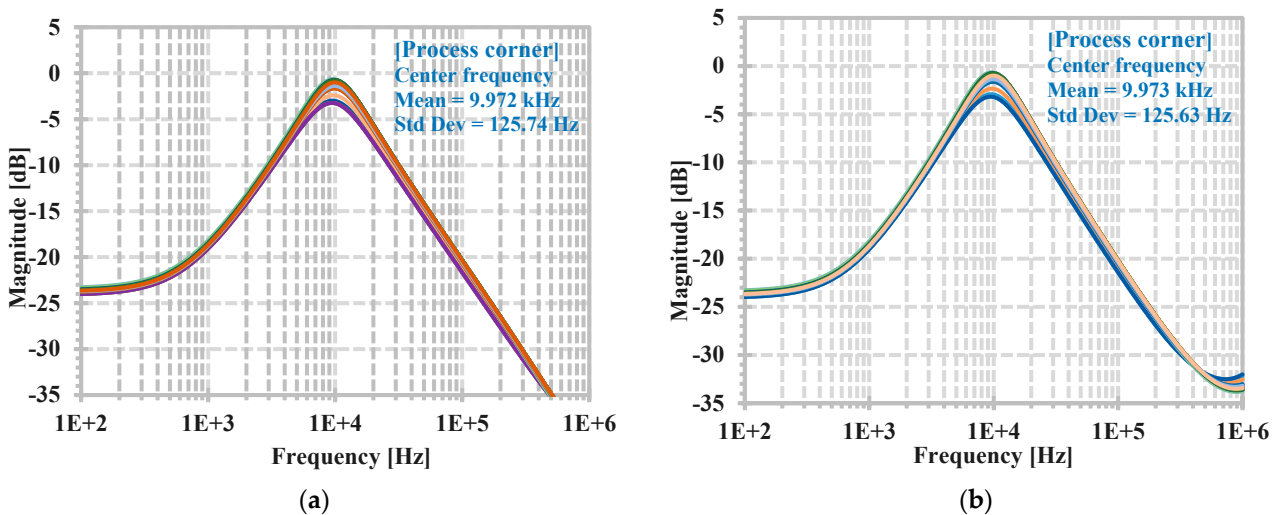


Figure 12. The simulated frequency response of the BPF when the process was varied: (a) VM, (b) CM.

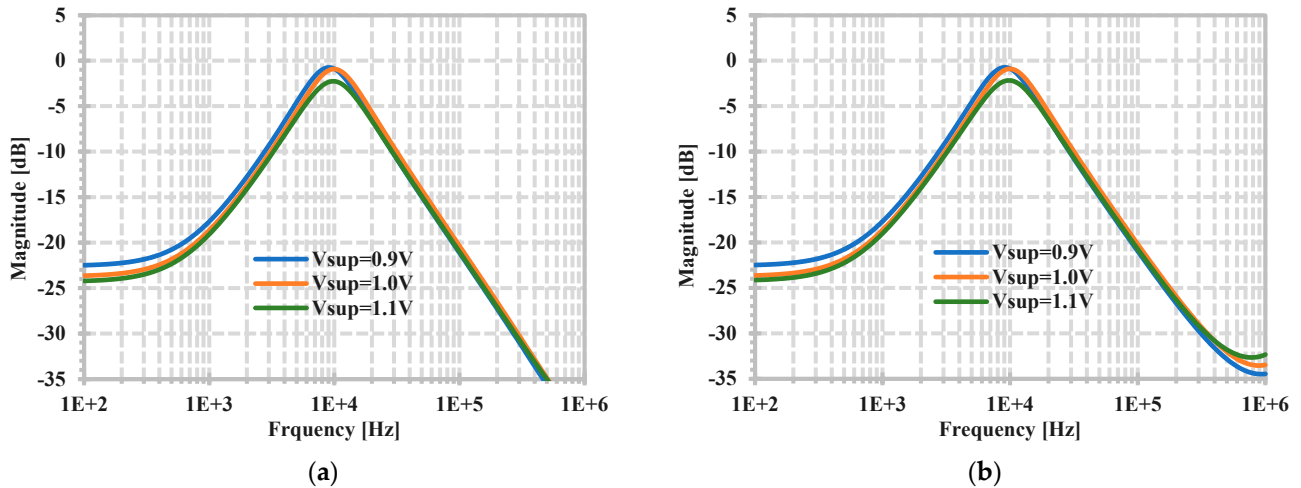


Figure 13. The simulated frequency response of the BPF when the supply voltage was varied: (a) VM, (b) CM.

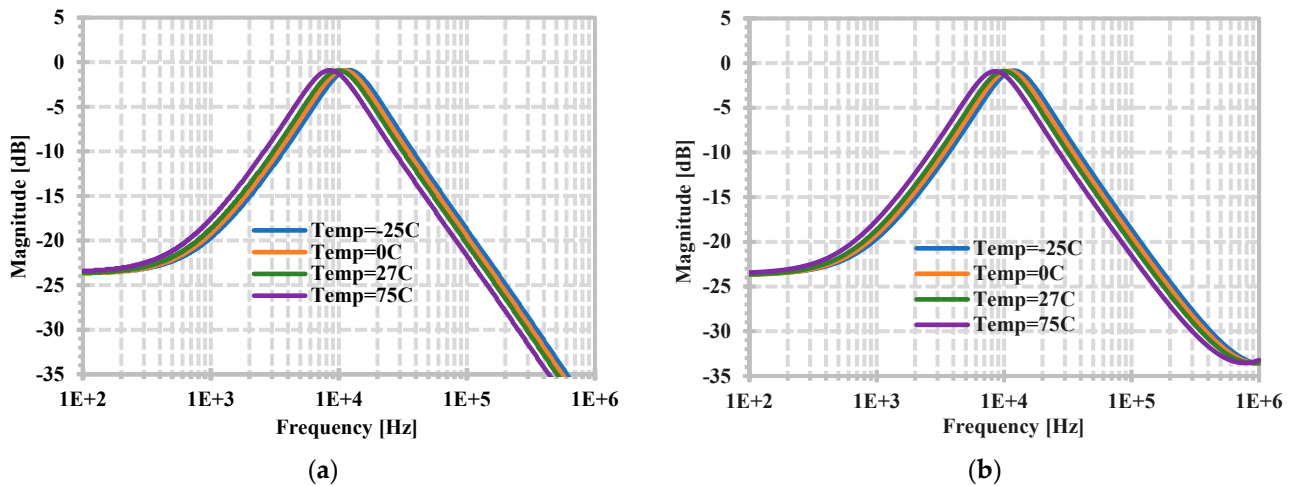


Figure 14. The simulated frequency response of the BPF when the temperature was varied: (a) VM, (b) CM.

The Monte Carlo analysis with 200 runs and 15% tolerance of the capacitors C_1 and C_2 was performed and the BPF of both VM and CM were selected to be shown. Figure 15 shows the histogram of the Monte-Carlo analysis of the center frequencies for the BPF of (a) VM and (b) CM. Figure 15a, shows that the standard deviation (σ) was 825.593 Hz, the mean was 10.045 kHz, and the minimal and maximal center frequencies were 8.031 kHz and 12.382 kHz, respectively, whereas the standard deviation was 825.435 Hz, the mean was 10.047 kHz, and the minimal and maximal center frequencies were 8.032 kHz and 12.386 kHz, respectively, for Figure 15b. To investigate the linearity of the proposed mixed-mode universal filter, the LPF's 10 kHz of the natural frequency was selected for testing, and the in-band frequency of 1 kHz was applied to the inputs, and both the VM and the CM were tested. Figure 16a,b show, respectively, the THDs of VM and CM with different input amplitudes, Figure 16c shows the input and output waveforms of VM of 0.983% THD ($V_{in} = 170$ mV), and Figure 16c shows the input and output waveforms of CM of 1.05% THD ($I_{in} = 5$ μ A).

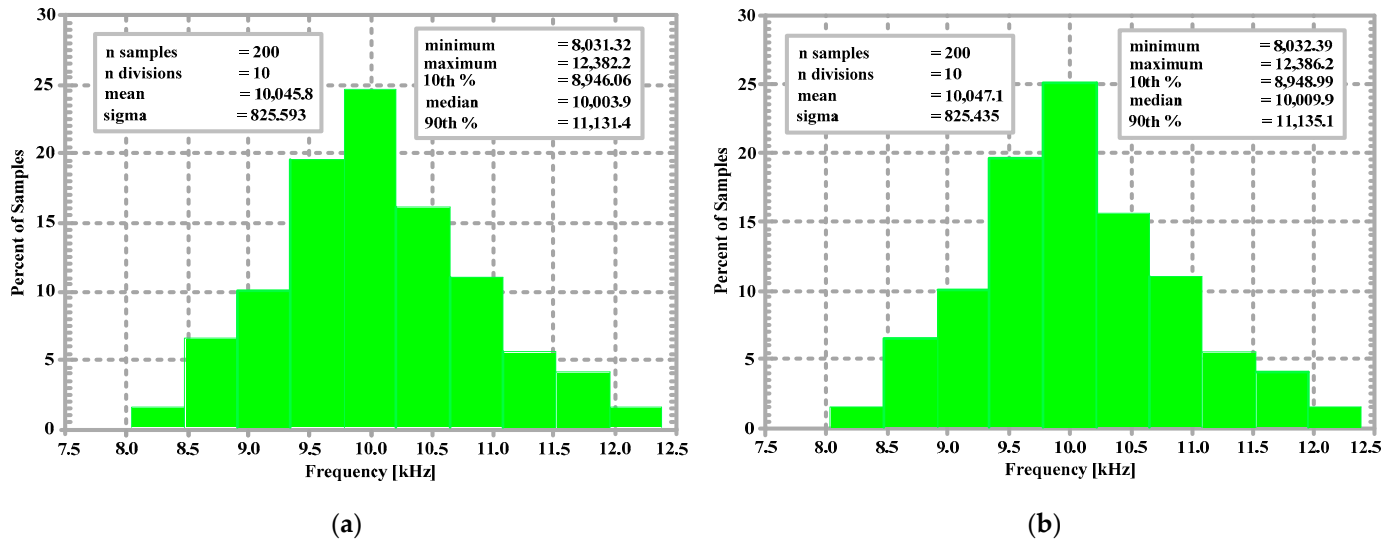


Figure 15. Simulated Monte-Carlo analysis for the BPF with 15% tolerance of the capacitors C_1 and C_2 : (a) histogram for VM, (b) histogram for CM.

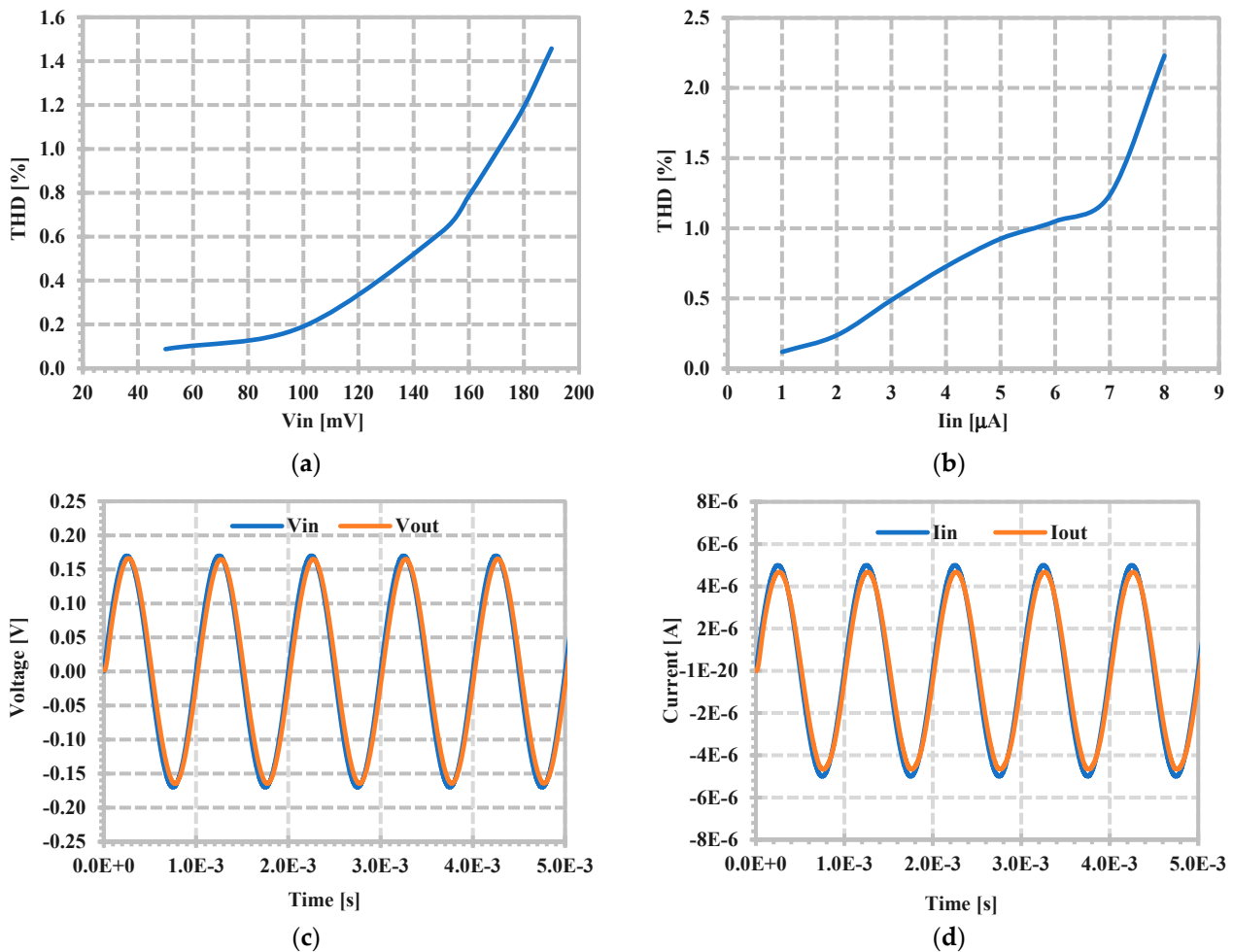


Figure 16. Simulated THD results of LPF: (a) THD with different voltage input amplitude of VM, (b) THD with different current input amplitude of CM, (c) input and output waveforms of 0.983% THD of VM, (d) input and output waveforms of 1.05% THD of CM.

Figure 17a,b show, respectively, the equivalent output noise of the VM and CM of the LPF. The integrated output noises in the bandwidth of 10 kHz were 156.5 μ V for the VM

and 0.729 nA for the CM. The dynamic ranges can be calculated as 57.7 dB for the VM and 73.7 for the CM.

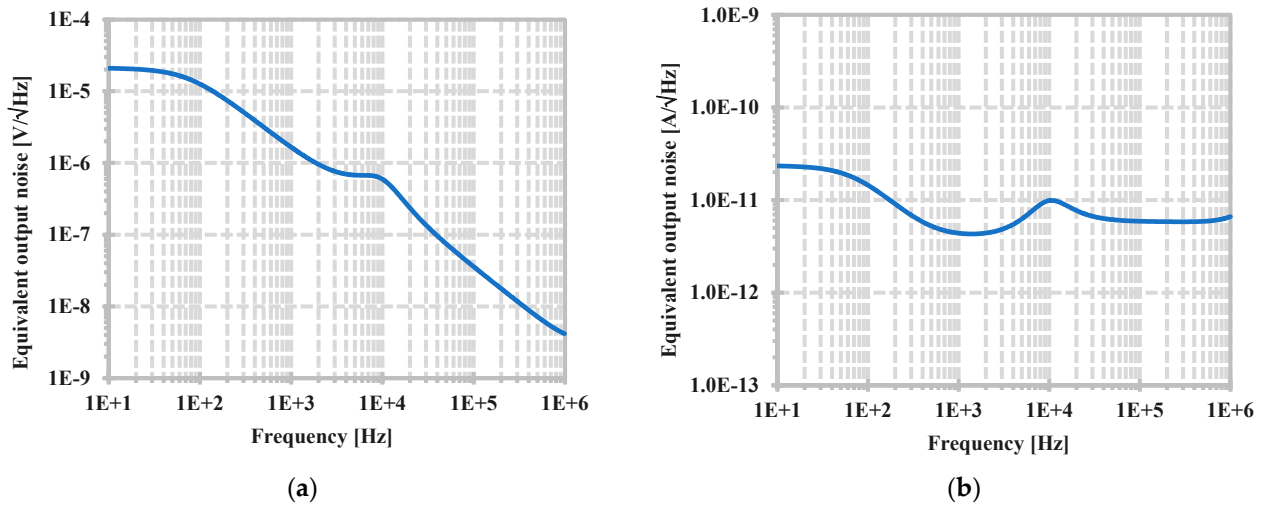


Figure 17. The equivalent output noises of LPF: (a) VM, (b) CM.

A comparison of the performance of the proposed filter with some previous works is shown in Table 4. For a fair comparison, the mixed-mode universal filters in [14,31,32,42,43,46] were selected. In [14], the filter using FDCCII and DDCC can provide many filter responses into the same circuit, the filters using OTAs in [31,32] can operate with low-voltage and low-power, and the recent filters in [42,43,46] use new active building blocks. Compared to [31,32], the proposed filter uses lesser active building blocks. Compared with the proposed structure, the filters in [42,44,47] enjoy using a minimum number of active elements, but to realize some transfer functions, these filters apply the voltage signals via the capacitors or resistors, which is not preferable for voltage-mode circuits, while the filters in [42,47] obtain the output currents via the capacitors or resistors which is not preferable for current-mode circuits. Compared with the filters in [14,31,32,42,43,46], the proposed mixed-mode universal filter can offer a maximum number of transfer functions, thanks to the multiple-input, multiple-output of the DDCCTA, both non-inverting and inverting transfer functions of five standard filter responses of four modes can also be obtained.

Table 4. Comparison of the proposed mixed-mode universal filter’s properties with those of some previous filters.

Factor	Proposed	[14] 2016	[31] 2022	[32] 2024	[42] 2021	[44] 2022	[47] 2022
Number of active devices	3-DDCCTA	1-FDCCII, 1-DDCC	8-OTA	4-OTA	2-VDBA	2-VD-DVCC	1-VGA
Realization	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS
Number of passive devices	2-C, 3-R	2-C, 6-R	2-C	2-C, 1-R	2-C, 2-R	2-C, 3-R	2-C, 1-R
Total number of offered responses	179	80	20	41	15	20	22
Electronic control of ω_0	Yes	No	Yes	Yes	Yes	Yes	Yes
Orthogonal control of ω_0 and Q	Yes	Yes	Yes	Yes	Yes	Yes	Yes
All passive devices grounded	Yes	No	Yes	Yes	No	No	No
High-input impedance (VM)	Yes	Yes	Yes	Yes	No	Yes	No

Table 4. Cont.

Factor	Proposed	[14] 2016	[31] 2022	[32] 2024	[42] 2021	[44] 2022	[47] 2022
High-output impedance (CM)	Yes	Yes	Yes	Yes	No	Yes	No
Power supply (V)	± 0.5	± 0.9	± 0.3	± 0.5	± 0.75	± 1	± 0.9
Power dissipation (μW)	374	-	5.77	156.8	373	4.28×10^3	1.31×10^3
Natural frequency (kHz)	10	1.59×10^3	5	5.95	1.44×10^3	5.305×10^3	3.18×10^3
THD (%)	0.983@170 mV 1.05@ 5 μA	2.2@300 mV _{PP}	1.3@50 mV 0.8@100 nA	1@220 mV	2.2@100 mV	1.82@100 mV	0.47@50 mV
Dynamic range (dB)	57.7 (VM) 73.7 (CM)	-	53.2 (VM)	40.2 (VM)	-	-	-
Verification of result	Sim	Sim	Sim	Sim	Sim/Exp	Sim	Sim/Exp

4. Conclusions

This paper presents a new mixed-mode universal filter using DDCCTAs and passive elements. The proposed filter benefits from using multiple-input, multiple-output, low-voltage and low-power DDCCTAs, which can realize 194 transfer functions of LPF, HPF, BPF, BSF, APF of VM, TAM, CM, and TIM into the same topology. The multiple inputs of DDCCTAs can be achieved using the MIBD-MOST technique to input the differential pairs of the circuit. The circuit's natural frequency and quality factor can be controlled electronically and orthogonally. The proposed DDCCTA and mixed-mode universal filter were designed and verified using a 0.18 μm CMOS process. The DDCCTA can operate with ± 0.5 V of supply voltage and the filter consumes 374 μW of power when operating at 10 kHz natural frequency. Therefore, the proposed circuits are suitable for low-voltage, low-power audio signal processing applications. In conclusion, devices that have multiple-input voltages can provide many VM and TAM filtering functions, while devices that have multiple-output currents will provide many CM, TAM and TIM filtering functions. However, devices with multiple-output currents increase the power consumption of the application.

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Appendix A

Table A1. Obtaining variant filtering functions of the TAM filter.

	Filtering Function	Input	Output	Condition
LPF	Non-inverting	V_7	I_{o3}	-
	Non-inverting	$V_1 = V_3$	I_{o3}	-
	Inverting	$V_2 = V_4$	I_{o3}	-

Table A1. Cont.

Filtering Function		Input	Output	Condition
LPF	Inverting	V_7	I_{o4}	-
	Non-inverting	$V_2 = V_4$	I_{o4}	-
	Inverting	$V_1 = V_3$	I_{o4}	-
HPF	Non-inverting	V_4	I_{o1}	-
	Inverting	V_3	I_{o1}	-
	Non-inverting	V_6	I_{o1}	-
	Inverting	V_5	I_{o1}	-
	Inverting	$V_2 = V_7$	I_{o1}	-
	Non-inverting	V_3	I_{o2}	-
	Inverting	V_4	I_{o2}	-
	Non-inverting	V_5	I_{o2}	-
	Inverting	V_6	I_{o2}	-
	Non-inverting	$V_2 = V_7$	I_{o2}	-
	Non-inverting	V_2	I_{o3}	-
	Inverting	V_1	I_{o3}	-
	Inverting	$V_4 = V_7$	I_{o3}	-
	Non-inverting	V_1	I_{o4}	-
	Inverting	V_2	I_{o4}	-
	Non-inverting	$V_4 = V_7$	I_{o4}	-
	Non-inverting	V_2	I_{o5}	-
	Inverting	V_1	I_{o5}	-
	Inverting	$V_4 = V_7$	I_{o5}	-
	Non-inverting	V_1	I_{o6}	-
	Inverting	V_2	I_{o6}	-
Non-inverting	$V_4 = V_7$	I_{o6}	-	
BPF	Non-inverting	V_7	I_{o1}	-
	Non-inverting	$V_1 = V_3$	I_{o1}	-
	Inverting	$V_2 = V_4$	I_{o1}	-
	Inverting	V_7	I_{o2}	-
	Non-inverting	$V_2 = V_4$	I_{o2}	-
	Inverting	$V_1 = V_3$	I_{o2}	-
	Non-inverting	V_6	I_{o3}	-
	Inverting	V_5	I_{o3}	-
	Non-inverting	V_5	I_{o4}	-
	Inverting	V_6	I_{o4}	-
	Non-inverting	V_4	I_{o5}	-
	Inverting	V_3	I_{o5}	-
	Non-inverting	V_6	I_{o5}	-
	Inverting	V_5	I_{o5}	-

Table A1. *Cont.*

Filtering Function		Input	Output	Condition
BPF	Inverting	$V_2 = V_7$	I_{05}	-
	Non-inverting	V_3	I_{06}	-
	Inverting	V_4	I_{06}	-
	Non-inverting	V_5	I_{06}	-
	Inverting	V_6	I_{06}	-
BSF	Non-inverting	V_3	I_{03}	-
	Inverting	V_4	I_{03}	-
	Non-inverting	$V_2 = V_7$	I_{03}	-
	Non-inverting	V_4	I_{04}	-
	Inverting	V_3	I_{04}	-
APF	Inverting	$V_2 = V_7$	I_{04}	-
	Non-inverting	$V_3 = V_5$	I_{03}	-
	Inverting	$V_4 = V_6$	I_{03}	-
	Non-inverting	$V_2 = V_5 = V_7$	I_{03}	-
	Non-inverting	$V_3 = V_5$	I_{04}	-
	Inverting	$V_4 = V_6$	I_{04}	-
	Inverting	$V_2 = V_5 = V_7$	I_{04}	-
	Non-inverting	V_4	$I_{04} + I_{06}$	-
	Non-inverting	V_3	$I_{03} + I_{05}$	-

Appendix B

Table A2. Obtaining variant filtering functions of the TIM filter.

Filtering Function		Input	Output	Condition
LPF	Non-inverting	I_4	V_{01}	-
	Inverting	I_5	V_{01}	-
	Non-inverting	I_4	V_{02} or V_{05}	-
	Inverting	I_5	V_{02} or V_{05}	-
	Non-inverting	I_2	V_{03}	-
	Inverting	I_3	V_{03}	-
	Non-inverting	I_3	V_{04}	-
	Inverting	I_2	V_{04}	-
	Non-inverting	I_5	V_{07}	-
	Inverting	I_4	V_{07}	-
HPF	Non-inverting	I_1	V_{02} or V_{05}	-
	Inverting	I_3	V_{06}	-
	Inverting	I_1	V_{07}	-

Table A2. Cont.

	Filtering Function	Input	Output	Condition
BPF	Non-inverting	I_3	V_{o1}	-
	Inverting	I_2	V_{o1}	-
	Non-inverting	I_3	V_{o2} or V_{o5}	-
	Inverting	I_2	V_{o2} or V_{o5}	-
	Inverting	I_1	V_{o3}	-
	Non-inverting	I_1	V_{o4}	-
	Non-inverting	I_5	V_{o6}	-
	Inverting	I_4	V_{o6}	-
	Non-inverting	I_2	V_{o7}	-
	Inverting	I_3	V_{o7}	-
BSF	Non-inverting	$I_1 = I_4$	V_{o2} or V_{o5}	-
	Inverting	$I_1 = I_4$	V_{o7}	$g_{m3} = 1/R_1$
APF	Non-inverting	$I_1 = I_2 = I_4$	V_{o2} or V_{o5}	-
	Inverting	$I_1 = I_2 = I_4$	V_{o7}	$g_{m3} = 1/R_1$

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