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2018 15th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)

eISBN: 978-1-5386-5153-7

DOI: https://doi.org/10.1109/SMACD.2018.8434560

Accepted manuscript

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***Abstract*—This paper presents new topology of fully universal multi-parametrically and electronically reconfigurable reconnection-less single-input single-output (SISO) voltage-mode biquad filter. The proposed structure can be reconfigured to offer each of all five second-order transfers functions (high-pass, band-pass, low-pass, band-reject and all-pass) as well as setting of pole frequency and quality factor. Special active device called controlled-gain current-controlled differential difference current conveyor of second generation has been designed in 0.35 μm CMOS technology for purposes of modeling and simulation tests of proposed filter. PSpice simulations confirm intended behavior of the topology.**

Keywords—biquads, current conveyors, electronic control, multi-parametric control, reconfiguration, universal filter

I. INTRODUCTION

An idea of filtering circuits providing different output responses without necessity of change of the input and output terminal has been found as very useful for various applications where galvanic reconnection is problematic (microwave structures and integrated circuits on chip [1], [2]) or even not possible. Reconnection-less reconfigurable biquadratic (2^{nd}-order) filters have been studied in recent years. However, recent studies [3]-[6], have not brought fully universal solution (i.e. offering all five transfer functions). Readjustment between these types of transfers, namely high-pass (HP), band-pass (BP), low-pass (LP), band-reject (BR) and all-pass (AP), is not available in standardly complex solutions of reconfigurable reconnection-less filters of 2^{nd}-order ([3]-[6]), see comparison in Table I. The presented attempts [3]-[6] are not fully-featured (full universality) in comparison to the standard multifunctional single-input multiple-output (SIMO) or multiple-input single-output (MISO) topologies, see for example [7]-[10]. Our newly proposed solution of the filter solves issues of previous topologies, especially lack of full universality and lack of high input impedance (simple cascadability) whereas number of used active elements remains satisfactory in comparison to [4].

This paper is organized in the following way. Section II explains model of new advanced active device (its basic features) typical by multi-parameter controllability and multi-terminal features and designed for purposes of discussed application in universal reconfigurable filter that is introduced in Section III. Section IV shows exemplary results of simulated circuit and Section V provides concluding remarks.

Research described in this paper was financed by Czech Ministry of Education in frame of National Sustainability Program under grant LO1401. For research, infrastructure of the SIX Center was used.

TABLE I. COMPARISON OF RECENTLY DEVELOPED RECONFIGURABLE RECONNECTION-LESS MULTIFUNCTIONAL 2^{ND}-ORDER FILTERS

Reference	Available transfers	No. of act./pas. elements	Mode (voltage-VM/current-CM)	Inp. impedance /independent on frequency?	Out. impedance /independent on frequency?
[3]	BR, AP[a]	2/4	VM	-/No	Low/No
[4]	BR, AP	7/7	VM	-/Yes	Low/Yes
[5]	BR, AP, HP, HPZ[b], LPZ, iBP[c]	4/2[d]	VM	-/No	-/No
[6]	LP, HP, BR, HPZ, LPZ	2/3	CM	Low/Yes	High/Yes
Fig. 4	HP, iBP, LP, BR, AP	4/4	VM	High/Yes	-[e]/Yes

[a] not controllable $Q_p < 0.5$; [b] HPZ, LPZ (HP and LP responses with zero); [c] iBP (inverting BP) not full-featured (low-frequency side-band with finite attenuation); [d] floating C required (complication for IC implementation); [e] depends on setting of controllable resistance of X terminal (active device)

II. CONTROLLED-GAIN CURRENT-CONTROLLED DIFFERENTIAL DIFFERNCE CURRENT CONVEYOR

An overview of advanced active elements has been prepared in [11], [12]. Differential voltage operations as well as current output terminals are highly useful in the design of filtering structures. Therefore, differential difference current conveyor of second generation (DDCC) [13] and its further modification [14] inspired our proposal and presented design. An application of this active element presented in this paper supposes electronic control of parameters (tuning, etc.). Parameters of active element, supposed for adjustment in the intended application, are the current input terminal resistance [15] and current gains (see [16] and references cited therein). Both these parameters can be controlled independently in single active element [17], however, with lack of differential voltage operation [13], [14]. The current-controlled differential difference current conveyor (CCDDCC) [18], [19] solves this issue partially (its current input terminal defines and employs controllable resistance).

The so-called controlled-gain current-controlled differential difference current conveyor of second generation (CG-CCDDCC) was designed in order to overcome these issues and it is shown in Fig. 1. Terminals Y_1 and Y_2 represent high

impedance differential voltage inputs, X is low-impedance controllable current input terminal and $Z_{1,2}$ are high-impedance current outputs. The transfer relations of CG-CCDDCC have the following definition: $V_{Y1} - V_{Y2} = V_X - R_X I_X$ ($V_{Y1} - V_{Y2} = V_X$ for open X), $I_{Z1} = I_X B_a$, $I_{Z2} = -I_X B_b$, where B_a and B_b represent independently electronically adjustable current gains (new feature of the device with respect to previous solutions). Figure 2 introduces the concept of the CG-CCDDCC.

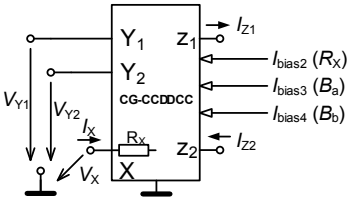


Fig. 1. Symbol of CG-CCDDCC active device.

The structure in Fig. 2 implements operational transconductance amplifiers (OTAs) [20] as the building blocks. The CMOS model (Fig. 3) was prepared in ON Semiconductor 0.35 µm I3T process [21]. The operation between Y_1, Y_2 and X has the following relation (X open):

$$V_X = \frac{I_{OTA1}}{g_{m2}} = \frac{g_{m1}\left(V_{Y1} - V_{Y2}\right)}{g_{m2}}, \qquad (1)$$

where $V_{Y1} - V_{Y2} = V_X$ results from equality $g_{m1} = g_{m2}$. The small-signal input resistance R_X can be found as:

$$R_X \cong \frac{1}{g_{m3}} \cong \left(K_{Pn} \left(\frac{W}{L} \right)_{M29,30} I_{bias2} \cdot 10 \right)^{-1/2}. \qquad (2)$$

The transconductance g_{m3} belongs to the differential pair of the OTA_3 ($M_{29,30}$), and $K_{Pn} = 136 \cdot 10^{-6}$ µA/V^2 [21]. The current gain B_a can be calculated as:

$$B_a = \frac{g_{m6}}{g_{m4}} \cong \sqrt{\frac{2K_{Pn}\left(\frac{W}{L}\right)_{M33,34} I_{bias3}}{4K_{Pn}\left(\frac{W}{L}\right)_{M31,32} I_{bias1}}} \cong \sqrt{\frac{I_{bias3}}{2I_{bias1}}}, \qquad (3)$$

when supposing both transconductance constants and W/L ratios as equal (identical differential pairs). Using the same way of simplification, the gain B_b can be expressed similarly: $B_b = -g_{m5}/g_{m4} \cong (I_{bias4}/(2 \cdot I_{bias1}))^{-1/2}$. The Table II summarizes basic features of proposed CMOS solution.

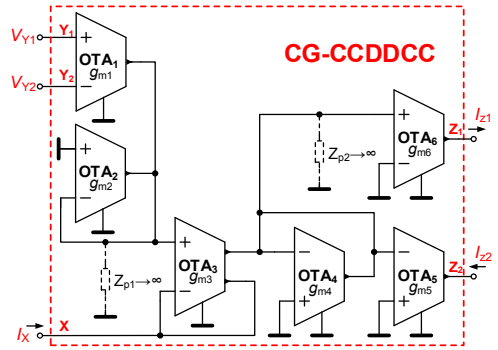


Fig. 2. Internal block concept of designed CG-CCDDCC active element.

TABLE II. TYPICAL PARAMETERS OF CCDDCC CMOS MODEL

	AC analysis		DC analysis
transfer	BW (3 dB) [MHz]	gain [-]	input range
$Y_1 \rightarrow X$	35→61*	0.99	–500→500 mV (X open)
$Y_2 \rightarrow X$	35→60*	–0.99	500→–500 mV (X open)
$X \rightarrow Z_1$	72→105**	0.2→1.4**	–200→200 µA (Z_1 short)**
$X \rightarrow Z_2$	79→104**	–0.1→–1.3**	200→–200 µA (Z_2 short)**

*I_{bias2} = 5→50 µA causing R_X = 2.7→0.71 kΩ ($I_{bias3,4}$ = 100 µA); **$I_{bias3,4}$ = 10→200 µA (I_{bias2} = 25 µA);
For (I_{bias1} = 50 µA, I_{bias2} = 25 µA, $I_{bias3,4}$ = 100 µA, supply ± 1.65 V): R_X = 1 kΩ, 16 µH, 775 fF; R_{Y1} = inf., 13 fF; R_{Y2} = inf., 13 fF; R_{Z1} = 30 kΩ, 713 fF; R_{Z2} = 164 kΩ, 587 fF

III. RECONFIGURABLE FULLY UNIVERSAL FILTER

The transfer function of newly proposed circuitry of electronically reconfigurable reconnection-less SISO biquad (Fig. 4), has the following full form:

$$K(s) = \frac{\frac{R_1 B_{1a}}{R_{X1}} s^2 - \frac{R_1 B_{2b}}{R_{X1} R_{X2} C_2} s + \frac{B_{2a} B_{3a} R_2}{R_{X1} R_{X2} R_{X3} C_1 C_2}}{s^2 + \frac{1}{R_{X1} C_1} s + \frac{B_{2a}}{R_{X1} R_{X2} C_1 C_2}}, \qquad (4)$$

where basic parameters of the filter (pole frequency and quality factor) are given as:

$$f_p = \sqrt{\frac{B_{2a}}{R_{X1} R_{X2} C_1 C_2}}, \quad Q_p = \sqrt{B_{2a} \frac{R_{X1}}{R_{X2}} \frac{C_1}{C_2}}. \qquad (5), (6)$$

The specific setting of the current gains (B_{1a}, B_{2b}, B_{3a}) in (4) produces transfer responses as shown in Table III.

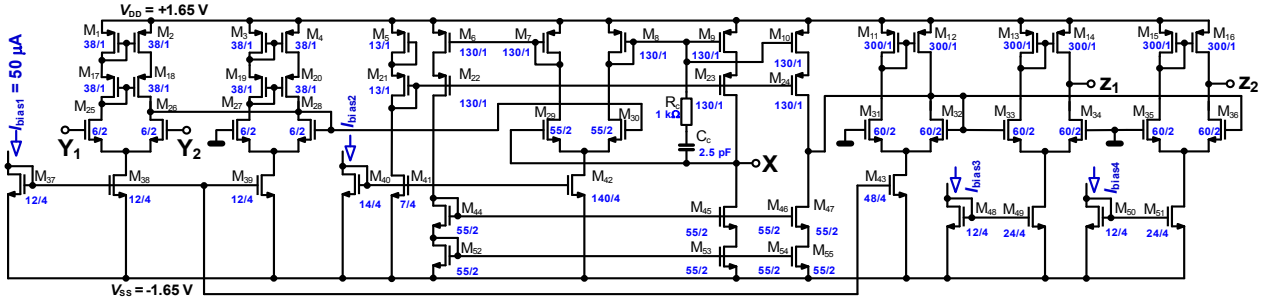


Fig. 3. Full CMOS implementation of CG-CCDDCC based on OTA building blocks as shown in Fig. 2.

TABLE III. CONFIGURABLE PROPERTIES OF THE BIQUDAD (FIG. 4)

transfer	B_{1a} ($I_{bias3(1)}$)[a]	B_{2b} ($I_{bias4(2)}$)	B_{3a} ($I_{bias3(3)}$)
HP	1 (100 μA)	0 (0 μA)	0 (0 μA)
iBP	0 (0 μA)	1 (100 μA)	0 (0 μA)
LP	0 (0 μA)	0 (0 μA)	1 (100 μA)
BR	1 (100 μA)	0 (0 μA)	1 (100 μA)
AP	1 (100 μA)	1 (100 μA)	1 (100 μA)

[a] $I_{bias3(\text{number of CG-CCDDCC in Fig. 4})}$

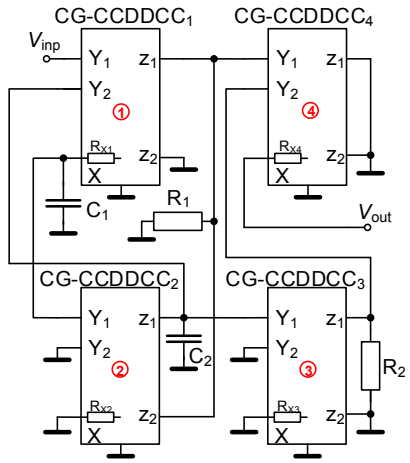


Fig. 4. Universal electronically reconfigurable SISO biquad filter.

IV. DESIGN AND VERIFICATION

Our verification targets on the following parameters of the filter: $f_p = 300$ kHz, $Q_p = 0.707$ (Butterworth approximation), $R_1 = R_2 = 1$ kΩ and $R_{X3} = 1$ kΩ ($I_{bias2(3)} = 25$ μA). Supposing $R_{X1} = R_{X2} = R_{X1,2} = 1$ kΩ ($I_{bias2(1,2)} = 25$ μA) in the initial design, the remaining values of parameters can be achieved from modified equations (5), (6) as: $C_1 = 1/(R_{X1,2}^2 \cdot C_2 \cdot (2 \cdot \pi \cdot f_p)^2)$ and $C_2 = C_1/Q_p^2$. Simple calculation yields values (selected from fabrication series) $C_1 = 360$ pF and $C_2 = 750$ pF. It causes acceptable deviation from initial f_p, Q_p (expected $f_p = 306$ kHz, $Q_p = 0.69$, $Q_p = 6.2$ obtained for $C_1 = 3.3$ nF and $C_2 = 82$ pF).

The PSpice analysis yields $f_p = 305$ kHz and $Q_p = 0.7$. The HP, iBP (also for $Q_p = 6.2$), LP and BR magnitude responses in Fig. 5 document each of possible transfer functions as shown in Tab. III. Transfer of the AP in Fig. 6 includes magnitude and phase response.

The ideal bandwidth (BW) of the iBP reaches $BW = f_p/Q_p = 424$ kHz). The expected $BW = 1/(2 \cdot \pi \cdot R_{X1} C_1) = 442$ kHz and simulation yields 434 kHz. The iBP response offers tunability of f_p (expected $f_p = 201 \rightarrow 358$ kHz, simulated $f_p = 184 \rightarrow 362$ kHz) with various bandwidth (expected $BW = 190 \rightarrow 603$ kHz, simulated $BW = 158 \rightarrow 613$ kHz) by $R_{X1} = 2.7 \rightarrow 0.73$ kΩ ($I_{bias2(1)}$ parameter) or with constant bandwidth in case of B_{2a} ($I_{bias3(2)}$) driving (Fig. 7). For theoretically constant BW operation, the simulated variation of BW achieves $442 \rightarrow 431$ kHz for $B_{2a} = 0.31 \rightarrow 1.4$ while expected $f_p = 173 \rightarrow 364$ kHz and simulated $f_p = 135 \rightarrow 360$ kHz.

The next interesting feature of our filter is tunability (Fig. 8) of the LP filter by simultaneous control of $R_{X1,2} = 2.7 \rightarrow 0.73$ kΩ and B_{2a} ($B_{2a} = 0.31 \rightarrow 1.4$) values when Q_p change is not important. Simple way of LP tuning by $R_{X1,2}$ offers expected $f_p = 130 \rightarrow 410$ kHz (simulated $f_p = 100 \rightarrow 410$ kHz). The combined method ($R_{X1,2}$ and B_{2a} control) extends expected range significantly to $f_p = 34 \rightarrow 567$ kHz (simulated $f_p = 15 \rightarrow 567$ kHz).

Note that continuous and mutually independent adjustability of individual parameters (coefficients) of numerator of transfer function of the filter brings possibility of various shaping of transfer response in dependence on current requirements. The HP and LP transfers with zeros are also available (the zero location and stop-band gain can be set) and also pass-band gain of these functions can be controlled.

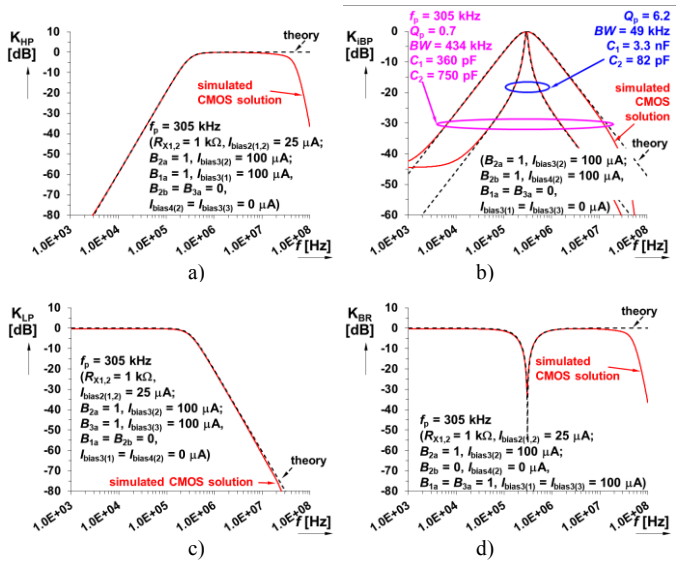


Fig. 5. Magnitude responses of the filter configured as: a) HP, b) iBP, c) LP, d) BR. (Particular setting of current gains is shown in each graph.)

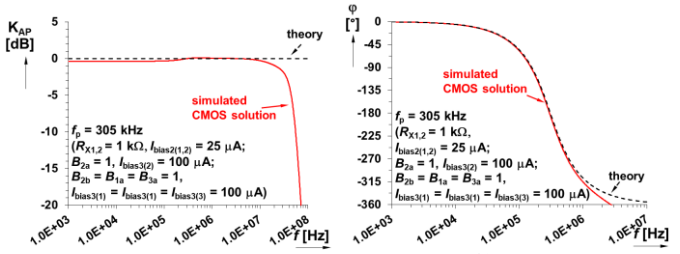


Fig. 6. Configuration as AP filter: a) magnitude response, b) phase response.

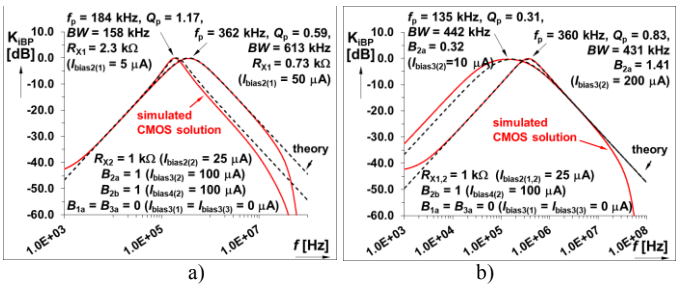
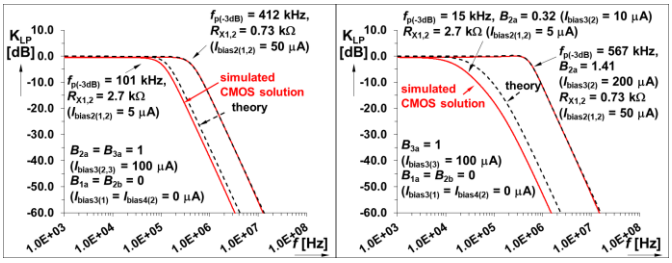
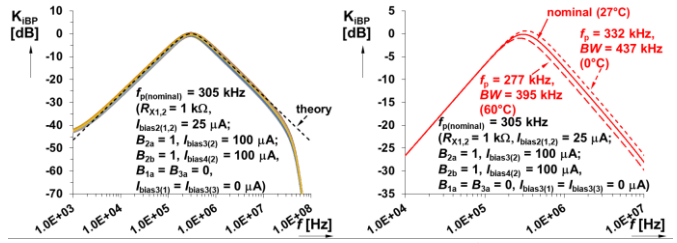


Fig. 7. Tuning of f_p in case of iBP response: a) various BW, b) constant BW.



a) b)

Fig. 8. Tuning of f_p in case of the LP response: a) by $R_{X1,2}$ only, b) by $R_{X1,2}$ and B_{2a}.



a) b)

Fig. 9. Simulation of real influences: a) Monte Carlo analysis observed at iBP response (1000 runs), b) temperature variation (0→60°C).

The fabrication dispersion of active parameters and temperature effects play important role in real influences on performance (Fig. 9). We tested Monte Carlo variation of passive (tolerances 5% for capacitors, and 1% for external resistors) as well as active parameters (tolerance 5% of all $I_{bias2,3,4}$ for setting of R_{X1-3} and current gains) at iBP response for nominal setting: $f_p = 305$ kHz, $Q_p = 0.7$. Simulation (1000 runs) brings max. $f_p = 344$ kHz, min. $f_p = 270$ kHz with 3sigma dispersion 37.6 kHz and max. $Q_p = 0.81$, min. $Q_p = 0.62$ with 3sigma dispersion 0.09. The temperature variation (0→60°C) causes change of $f_p = 332 \rightarrow 277$ kHz, $BW = 437 \rightarrow 395$ kHz.

V. Conclusion

Presented advanced active device brings interesting features for synthesis of complex types of transfers in the frame of newly studied reconnection-less reconfigurable universal filtering application. Presented tunability ranges of f_P are not wide due to conceptual (CMOS) limitations of g_m-s and R_X as well as operational bandwidth values (up to 40 MHz) of designed active device. However, it can be improved in future. The main goal of our work targeted on verification of the CG-CCDDCC CMOS model suited and intended for presented application where reconfigurable features were sufficiently confirmed.

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