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A Tunable Immitance Simulator with a Voltage Differential Current Conveyor

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***Abstract*—In this paper, an electronically tunable immitance circuit is proposed. The presented circuit can be configured as a tunable grounded inductor or capacitor multiplier. The proposed circuit employs a single active element called Voltage Differential Current Conveyor, a single resistor and a single capacitor. The presented circuit does not require element matching constraints. It is linearly tunable over four decades of frequency using bias current control. Simulation results are included to verify theory.**

Keywords—Current conveyor, inductance simulator, immitance, active filter.

I. INTRODUCTION

Immitance simulators have wide application area in analog electronics. They can be used as capacitance multiplier or inductance simulator with suitable choice of passive elements. Immitance simulators may help reducing chip area for example to replace on chip inductors for certain applications. Especially the design of very large capacitors or inductors is impractical in integrated circuit (IC) technology. Some immitance simulator circuits in the literature provide easy electronic tunability if they include current controlled active elements, and this is also exploited in this study.

In the literature many capacitance multiplier circuits have been proposed. Ferri and Pennisi presented a capacitance multiplier circuit by employing a current conveyor, a current operational amplifier, two resistors and a capacitor [1]. Some electronically tunable capacitor multiplier circuits have also been presented in the literature. The circuit in ref. [2] uses two operational transconductance amplifiers (OTA), one operational amplifier, and one capacitor. Abuelma'atti and Tasadduq proposed a circuit using three current conveyors, one resistor and one capacitor [3]. Di Cataldo et. al. presented a circuit using two current conveyors two resistors and one capacitor [4].

Most of the floating or grounded synthetic inductor topologies (Pal [5]-[6], Singh [7], Senani [8], Higashimura and Fukui [9], Paul and Patranabis [10]), suffer from excessive number of active or passive components. The circuits presented in ref. [5-8] use four current conveyors. Another publication presents a circuit suitable for inductor simulation that employs two third generation current conveyors CCIIIs proposed by Liu and Yang [11]. The grounded inductor simulating topology in reference [10] employs only a single current conveyor, four resistors and one capacitor. For each type of inductor at least one condition and/or cancellation constraint is to be satisfied in order to realize the inductor. Moreover for each type of inductor all four passive elements are used. The cancellation constraints require passive component matching which is hardly realizable in practice. Also, Abuelmaatti, Khan, and Al-Zaher [12] proposed floating inductance with only active components.

In this study we proposed an immitance circuit topology providing electronically tunable capacitor multiplier and grounded inductor using a single active element, one resistor and one capacitor. We used a voltage differential current conveyor (VDCC) that is a recently proposed and popular active element [13-18]. The presented topology does not have element matching restriction and employs minimum number of active and passive components. The impedance functions for the nonideal cases are also given. All passive sensitivities are found to be no more than unity. Equations corresponding to these nonidealities are included. Finally a ladder LC highpass filter application example is included.

II. THE VDCC AND PRESENTED CIRCUITS

The VDCC shown in Fig. 1 is described by the following terminal equations:

$$V_n = V_p,\quad I_z = I_n,\quad I_x = g_m(V_v - V_z),\quad I_v = 0,\ I_p = 0. \qquad (1)$$

The proposed immitance simulation topology is shown in Fig. 2. The input impedance of the circuit is given in the following equation:

$$Z_i = \frac{2Y_1}{g_m Y_2}. \qquad (2)$$

Asuming Y_1 and Y_2 selected as either a capacitor or a resistor the passive sensitivities are no more than unity given as $\left|S_C^Z\right| = 1$, $\left|S_G^Z\right| = 1$.

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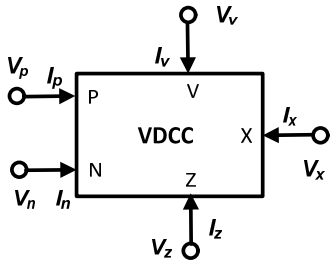


Fig. 1 The VDCC block diagram

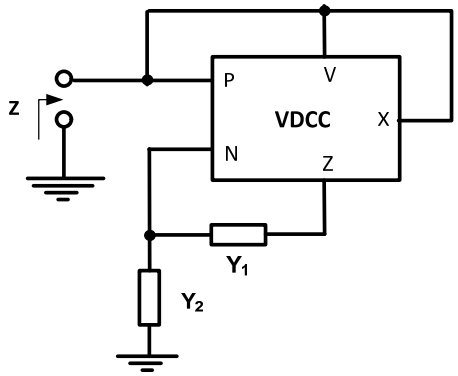


Fig. 2 The presented immitance simulator topology with VDCC

The presented topology in Fig 2 provides a grounded lossless inductor for $Y_1 = sC$ and $Y_2 = 1/R$ as shown in Fig. 3a without matching condition and with minimum number of passive components:

$$L_{eq} = \frac{2CR}{g_m}. \tag{3}$$

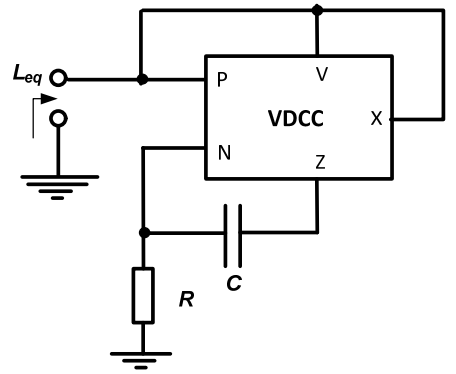
Also a capacitor multiplier can be obtained for $Y_2 = sC$ and $Y_1 = 1/R$ as shown in Fig. 3b similarly without matching condition and with minimum number of components and a grounded capacitor.

$$Z_i = \frac{1}{sC_{eq}}. \tag{4a}$$

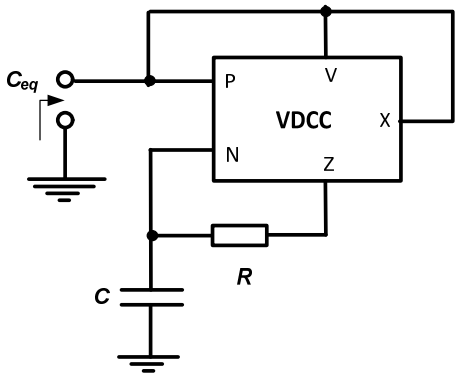
$$C_{eq} = \frac{CRg_m}{2}. \tag{4b}$$

In the modern MOS IC technology, it is easy to obtain high-resistance values without requiring large chip area using pinched n-well and p-well layer [19]. Although accuracy of this type of resistors is around 25-40%, it is not a disadvantage for tunable circuits since deviation from the center frequency can easily be tuned with an external current.

Inductors are difficult to integrate. Therefore inductance simulators are often used instead. Nonideality analysis is necessary to evaluate the behavior. Taking nonidealities as $V_n = \beta V_p$, $I_z = \alpha I_n$, $I_x = \gamma g_m(V_v - V_z)$, the equivalent nonideal inductance becomes:



(a)



(b)

Fig. 3 The presented circuits: (a) inductance simulator configuration, (b) capacitor multiplier configuration

$$L_{eq} = \frac{CR(1+\alpha)}{CRg_m(1+\alpha)(-1+\beta)\gamma + g_m\alpha\beta\gamma}. \tag{5}$$

Comparing Eq. 5 with Eq. 3 one can determine how to minimize nonideal effects.

III. Simulation Results

The functionality is tested on a third-order Butterworth high-pass prototype LC ladder. In our LTSPICE simulations, a CMOS implementation of VDCC in Fig. 4 is used. The transistor parameters used for the simulations are taken from TSMC 0.35µm technology. The aspect ratios of NMOS and PMOS transistors from the internal CMOS implementation of the VDCC are given in TABLE I. I_0 biasing current is 100µA. The proposed circuit in Fig. 3a is simulated with the following passive element values: R = 100 Ω, C = 50 pF. AC response of the input impedance function of the proposed circuit is given in Fig. 5 for I_1 = 10 µA and I_1 = 300 µA. The non-idealities of the VDCC such as current and voltage gain errors, non-ideal output and input impedances of VDCC cause the deviations from theoretical values especially at the low frequencies.

As an application example, a third-order Butterworth high-pass ladder filter is chosen as shown in Fig. 6. The component values are: $R_S = R_L$ = 300 Ω, $C_1 = C_2$ = 1 nF, R = 100 Ω, C = 50 pF, I_1 = 300 µA in Fig. 3(a) for L_1 = 45.5 µH. The simulation result for the AC response is shown in Fig. 7. Also

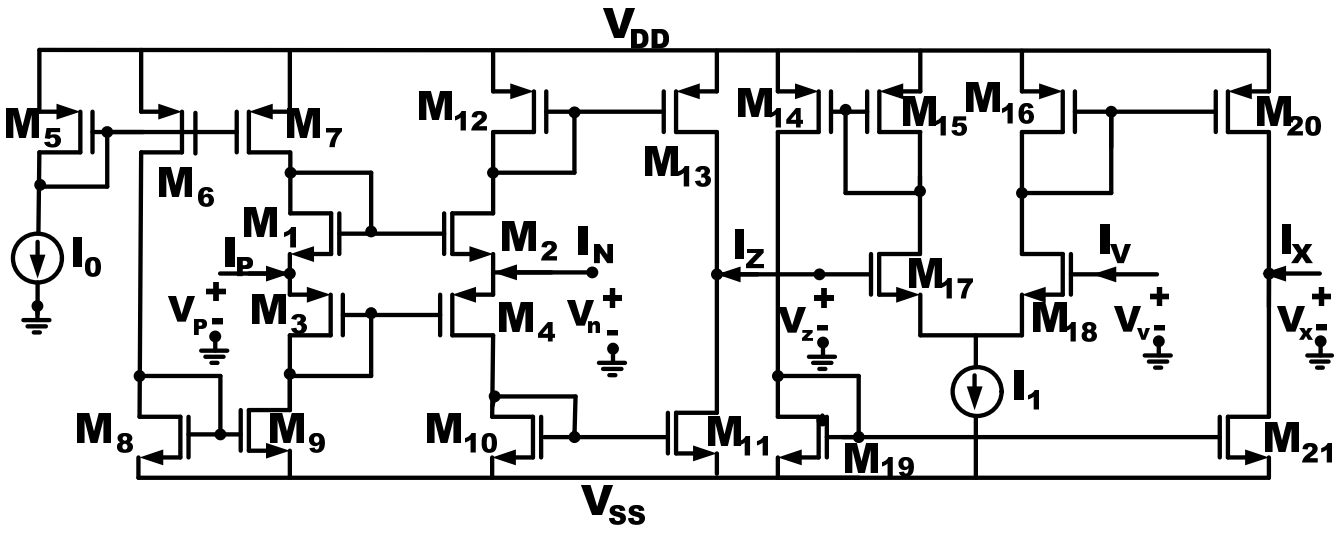


Fig. 4 CMOS implementation of VDCC

TABLE I. TRANSISTOR DIMENSIONS.

MOSFET	W(μm)/ L(μm)	MOSFET	W(μm)/ L(μm)
M1	20/0.35	M12	30/1
M2	20/0.35	M13	30/1
M3	60/0.35	M14	8.4/1.05
M4	60/0.35	M15	10.5/1.05
M5	30/2	M16	10.5/1.05
M6	30/2	M17	4.2/1.05
M7	30/2	M18	4.2/1.05
M8	10/2	M19	4.2/1.05
M9	10/2	M20	8.4/1.05
M10	10/1	M21	4.2/1.05
M11	10/1		

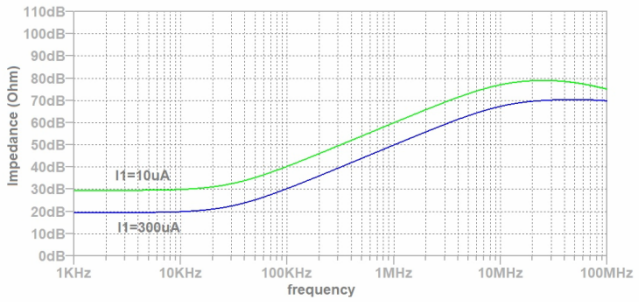


Fig. 5 AC analysis of the inductor simulator configuration (vertical axis represents magnitude of impedance Z with units Ω; 40dB->100Ω)

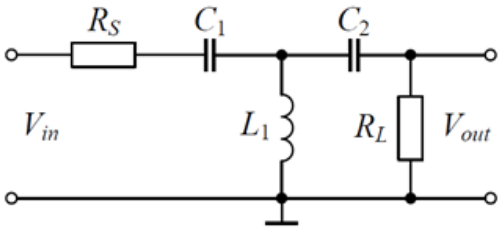


Fig.6 Application example: third-order Butterworth high-pass ladder filter

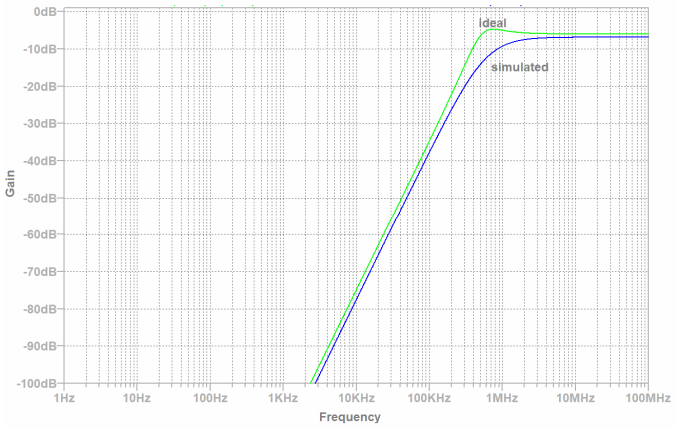


Fig. 7 AC Simulation result of the example filter circuit

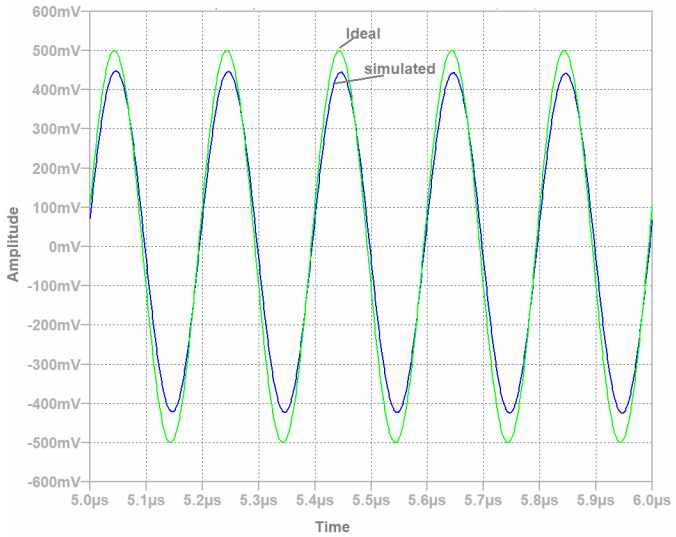


Fig. 8 Transient analysis result of the example filter circuit for 5 MHz output signal (vertical axis represents the output voltage)

5 MHz sinusoidal signal with 1 V peak to peak amplitude is applied to the input of the filter and time domain simulation result is given in Fig. 8. Although some deviations due to the non-ideality of the VDCC, the simulation results confirm well with theory.

IV. Conclusion

In this paper, a grounded immitance simulator topology not requiring passive component matching is proposed. The circuit uses a VDCC, a single capacitor and a single resistor. In the inductance simulator configuration, a high-pass LC ladder filter application example is given to illustrate the practical use of the topology. Simulation results are included to verify theory.

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