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HIGH-VOLTAGE STRUCTURES FOR GALVANIC ISOLATION IN INTEGRATED CIRCUITS

VYSOKONAPĚŤOVÉ STRUKTURY PRO GALVANICKOU IZIOLACI V INTEGROVANÝCH OBVODECH

DOCTORAL THESIS
DIZERTAČNÍ PRÁCE

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ABSTRACT

This Thesis introduces a novel lateral resonant coupling technique and discusses the design of an 800 V galvanically isolated translator which is subsequently utilized in the 800 V half bridge driver for industrial applications. The fabrication cost of this design is lesser in comparison with the currently widespread galvanically isolated translators. For applications that require a higher level of galvanic isolation, a follow-up development of the galvanically isolated translator is presented. This design utilizes a single galvanic isolator for communication in both, low-to-high and high-to-low, directions, which greatly reduces the area consumed by the isolator. As a part of the subsequent design, a galvanic isolator transmitting an analog value is introduced. The analog isolator has been tested in a real AC-DC converter application as a replacement of the standard opto-coupler. This design enables full integration of primary and secondary side controllers in a single package, thereby reducing the complexity and cost of the AC-DC converters.

KEYWORDS

Integrated circuit, high voltage, switch mode power supply, galvanic isolation, very large scale integration, high voltage translator, level shifter.

ABSTRAKT

Tato dizertační práce představuje novou techniku laterární rezonanční vazby, která je využita v návrhu galvanicky izolovaného posouvače úrovně, který je následně implementován v 800 V půlmůstkovém kontroléru pro průmyslové aplikace. Ve srovnání s tradičními galvanickými izolátory jsou výrobní náklady tohoto řešení nižší. Pro aplikace vyžadující vyšší úroveň galvanické izolace je popsán následný vývoj galvanicky izolovaného posouvače úrovně, který využívá pouze jeden galvanicky oddělený posouvač úrovní pro komunikaci v obou směrech, což výrazně snižuje plochu struktury izolátoru. Jako součást následného návrhu je představen galvanický izolátor který je schopen přenášet analogovou hodnotu napětí. Analogový izolátor byl testován v reálné aplikaci síťového spínaného zdroje jako náhrada standardního optočlenu. Tato konstrukce umožňuje integraci primárních a sekundárních obvodů v jednom pouzdře, což umožní snížit složitost a cenu spínaného zdroje.

KLÍČOVÁ SLOVA

Integrovaný obvod, vysoké napětí, spínaný zdroj napájení, galvanické oddělení, vysokonapěťový posunovač úrovně.

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PROHLÁŠENÍ

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V Brně dne ....

(podpis autora)

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V Brně dne: …………………………   …………………………

podpis autora

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1 INTRODUCTION

In the past, the semiconductor industry utilized various methods to form semiconductor devices for controlling HV (high-voltage) systems. A power supply controller that operates from household AC mains having HV values could represent a suitable example. Its input voltage may vary between tens to several hundred volts and the value may change with respect to time. A great demand to provide inexpensive electronic circuits for the power supplies exists. The circuits should be minimized in their physical dimensions and, if possible, integrated on monolithic semiconductor substrates. Many requirements must be fulfilled by the semiconductor process to ensure that the application system can be integrated as a monolithic device.

1.1 The Outline of Typical Contemporary Power Supply Designs

In order to reduce the size of the passive components, the switching frequencies need to increase. For such high frequencies, low to medium voltage applications in which the switching power losses can be dominant, MOSFETs are commonly used. Moreover, some MOSFET devices are designed to be driven with low voltage control, which also helps in reducing application system complexity and enables the employment of low voltage submicron technologies.

In some power supply configurations, two transistors are connected in a stacked configuration in order to drive an inductor and form output voltage. Some examples of such power supply configurations include LLC resonant power converters which can be formed in the half-bridge or full-bridge topology.

Each of the two transistors in the half-bridge circuit is driven by separate transistor drivers. To guarantee substantially constant output voltages of the power supply, control signals from low voltage circuit portions to HV circuit portions, or vice versa, are often used. Between portions with substantially different voltages, control signals need to be transferred or exchanged and the portions ought to be properly isolated.

Numerous cases of gate signal isolation systems in many power electronics circuits using a magnetic [1] or piezoelectric [2] transformer or dielectric coupling [3], [4], [5] to form a low voltage to a high voltage transmission line have been published. For monolithic solution, a level shifter [6] is often used. In order to minimize inductive effects and coupling resulting in increased commutation losses, the amplification of the driving signal is needed in very close proximity to the power transistor gate.

In the event of overvoltage, short circuit current or operation over the temperature limit additional protection circuits may prevent the system application from damage. With the help of VLSI (Very Large Scale Integration), complex functions can be integrated within a small silicon area, with specific isolation characteristics and separate from the power device, allowing operations at HV levels. In addition to level shifting possibility, HV CMOS processes also allow to integrate devices used for sensing the HV potentials or transients.

In power supply systems, the input voltage can be monitored for various reasons, but the most common are feed-forward capability [7] and brown-out detection [8].

Feed-forward is used to make the transfer function independent of the input voltage. This eases the loop compensation. Also, feed-forward is necessary each time the circuit takes action as a result of a power level, as in the case of the circuit needing to skip a cycle when the power drops below 10% of full load or if over-power protection is integrated.

Brown-out detection enables the converter if the line magnitude is sufficient and disables it in any other case. The brown-out circuit usually features a hysteresis for stable operation.

Under any circumstances, monitoring the input or output voltage is realized by HV resistor dividers. The resistivity of the divider is always a compromise between power dissipation and time response. In order to keep the power dissipation in reasonable bounds, the resistivity of the divider is usually high, thereby preventing the sensing of fast transients.

Another approach to sensing HV transitions is applying an HV capacitor. If the HV capacitor is formed as a monolithic structure on the same die as the controller, the capacitor value can be several orders lower in comparison with external capacitors, because of significantly smaller parasitic impedances and high reproducibility. The HV capacitor can also be used as galvanic isolation for signaling purposes.

Eventually, it is also advantageous to have a possibility of supplying the controller directly from the input voltage. Many approaches of forming such HV self-supply exist, see [9], [10] or [11].

Nowadays, it is highly required by semiconductor customers to make all of the above-listed HV devices also resistant to ESD. Many models to classify the susceptibility to damage or degradation of semiconductor devices have been created. The most commonly used ones are Human Body Model (HBM) [12] and Machine Model (MM) [13].

1.2 Organization of the Thesis

The Thesis is divided into seven chapters. Subsequent to this introductory chapter is Chapter 2, which outlines the background of the switching power supplies and the fabrication processes available for HV integrated circuit designs. It also introduces monolithic HV devices dedicated for HV measurements in integrated circuits. Chapter 3 deals with the significance and motivations of this Thesis. Chapter 4 introduces the novel lateral resonant coupling technique and discusses the design of the 800 V galvanically isolated translator which is utilized in Chapter 5, introducing the 800 V half bridge driver for industrial applications. Chapter 6 discusses the follow-up development of the galvanically isolated translator for HV applications, utilizing new ideas as well as those described in Chapters 5 and 6. The attained results of this work along with the outline of possible future work are presented in the final seventh chapter.

2 STATE OF THE ART

Traditional linear AC-DC power supplies have been in most cases replaced by Switch Mode Power Supplies (SMPS) as a way to reduce power consumption, reduce heat dissipation, as well as size and weight. SMPS became the most common power converter in standard consumer electronic devices such as power amplifiers, televisions, personal computers, and so on. For better understanding of the context, generally known SMPS operation principles and associated fundamental power-loss contributors are discussed in the next sections.

2.1 Operation Principle of Switching Power Supply

Various topologies of SMPS have been developed over time, either isolated designs employing a transformer or non-isolated designs utilizing inductors instead. But what all SMPS have in common is that the energy conversion and regulation is provided by power semiconductors that are continuously switching "on" and "off" with high frequency.

The SMPS usually converts voltage and current waveforms on its input to a rectangular shape signal by controlling the semiconductor switching components. The way of driving the switching semiconductor components and the resulting losses on them greatly affect the efficiency of the entire power supply. In the illustration of an ideal switching regulator shown in Fig. 2.1, the efficiency would amount to 100% due to the ideal switch chopping the input voltage. Zero current on the open or closed switch naturally results in zero power loss.

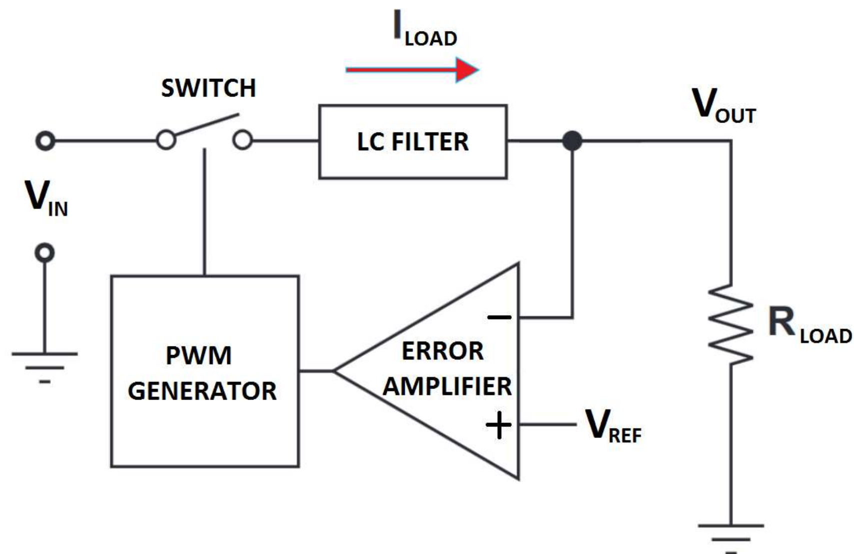

Fig. 2.1. Simplified schematic of the ideal switching regulator. Since the current is zero when the switch is open and the voltage across it is zero when the switch is closed, the power loss is nonexistent in both cases, resulting in 100% efficiency.

Nevertheless, real components are not ideal and during normal operation of the converter, several power loss contributors come into play:

- Switching losses generated on the switching semiconductor components due to dynamic currents and voltages during turn on and off events.
- Switching gate-drive losses generated in the controller gate driver when the switching semiconductor components turn on or off.
- Switching losses in the inductor due to core losses.
- Conduction losses generated on the switching semiconductor components on-resistance and inductor and PCB copper trace parasitic resistance.
- Static losses due to operational current consumption of the controller.

Let us evaluate the basic switching circuit – synchronous buck (step-down) converter shown in Fig. 2.2. This circuit represents a typical situation in power electronics – inductor current is controlled by a series switch. In this switching circuit example, Q1 and Q2 MOSFETS alternate in their switching operation; when the Q1 MOSFET is on, the Q2 MOSFET is off and vice versa.

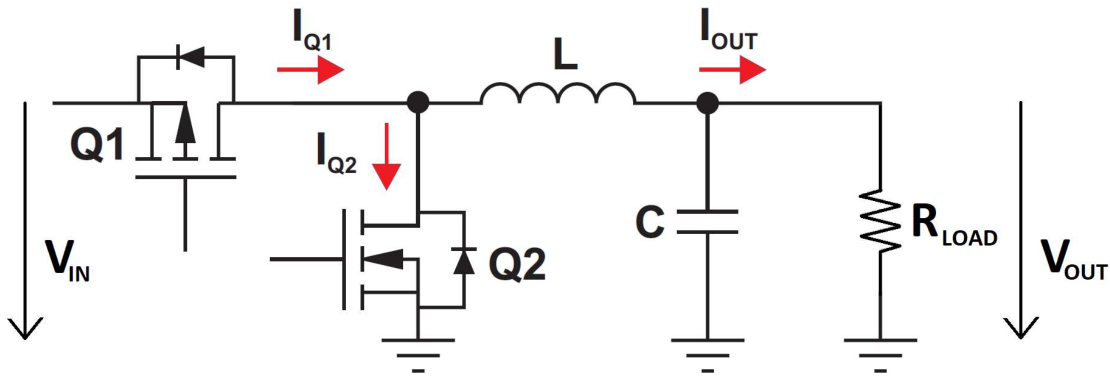

Fig. 2.2. Basic switching circuit – synchronous buck (step-down) converter example. Q1 and Q2 MOSFETS alternate in their switching operation.

Let us assume the Q1 MOSFET is off and the current in the inductor is zero. When the Q1 MOSFET is turned on, the current starts to increase and opposing voltage across inductor terminals is developed in response to the changing current. This voltage drop counteracts the input voltage (V_{IN}), thereby reducing the voltage across the load (V_{OUT}). The energy is stored in the inductor in the form of a magnetic field. When the Q1 MOSFET is turned off, the input voltage (V_{IN}) is removed from the circuit. The stored energy in the inductor magnetic field starts to support the current flow through the load and the inductor becomes a current source. The Q2 MOSFET is turned on and the current starts decreasing, thereby producing a voltage drop across the inductor opposite to the drop at on-state. If the Q2 MOSFET is turned off and Q1 MOSFET is turned on, the inductor current starts to increase again. In the real application of buck converter, a feed-back loop system utilizing an error amplifier and a PWM generator is employed to stabilize the output voltage (VOUT), as shown in Fig. 2.1.

In the complementary switched synchronous buck converter, the current may reverse within the switching period, hence always operating in the continuous conduction mode (CCM). However, the implementation of advanced control techniques enables operation in different modes as well [14].

2.1.1 Conduction Losses in Power MOSFET

Every MOSFET, when it is turned on, has a resistive element described as on-resistance (R_{DSon}), on which power is dissipated as current is conducted through the device. The voltage which is developed on the R_{DSon} is therefore:

$$u_{DS}(i_D) = R_{DSon}(i_D) \cdot i_D \qquad (1)$$

where u_{DS} is drain-source voltage and i_D is the drain current.

The instantaneous value of the power MOSFET conduction loss is therefore:

$$P_C(t) = u_{DS}(t) \cdot i_D(t) = R_{DSon} \cdot i_D^2(t) \qquad (2)$$

An average value of the MOSFET conduction losses is then obtained by integration of the instantaneous power losses:

$$P_C = \frac{1}{T_{SW}} \int_0^{T_{SW}} p_C(t)dt = \frac{1}{T_{SW}} \int_0^{T_{SW}} \left(R_{DSon} \cdot i_D^2(t)\right)dt = R_{DSon} \cdot I_{Drms}^2 \qquad (3)$$

where I_{Drms} is the rms value of the MOSFET drain on-state current.

Although the equations (1), (2) and (3) treat the R_{DSon} as a constant, in addition to junction temperature (T_j) it also represents a function of drain current I_D and gate-source voltage (V_{GS}) as shown in Fig. 2.3 [15].

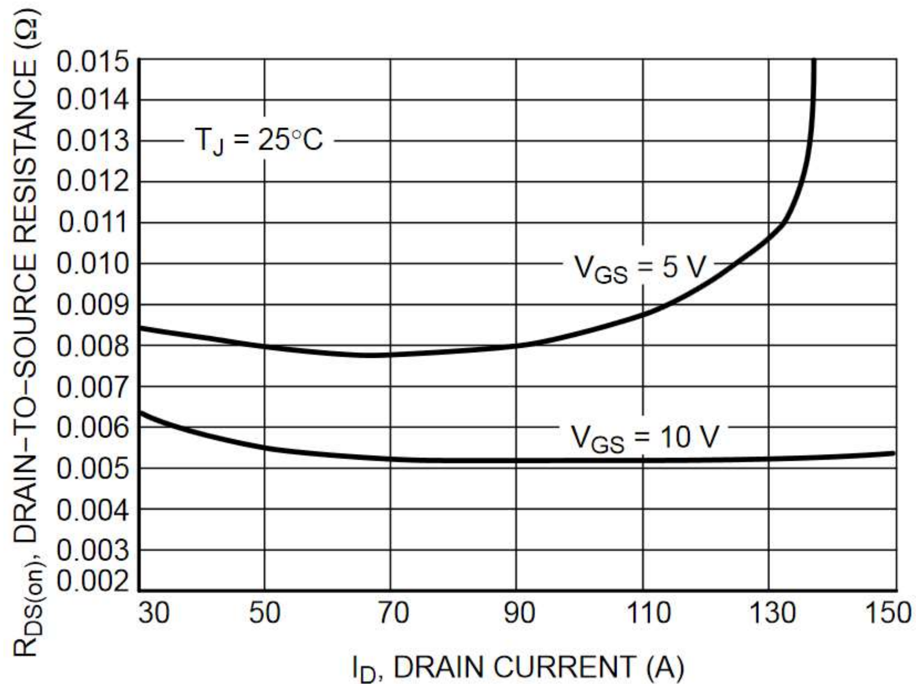

Fig. 2.3. Drain-source resistance as a function of drain current and gate-source voltage at T_J=25°C.

Since the R_{DSon} depends on V_{GS}, I_D and junction temperature (T_j), equation (3) does not determinate the losses entirely. In topologies such as the LLC resonant converter, where a considerable change in I_D is observed during operation, advanced conduction loss assessment needs to be employed. A detailed characterization is essential, comprising a measurement of the R_{DSon} under different V_{GS}, V_{DS} and I_D conditions. Resistance Temperature Detectors (RTDs) are then employed to determine the value of the case temperature, as shown in Fig. 2.4 [16].

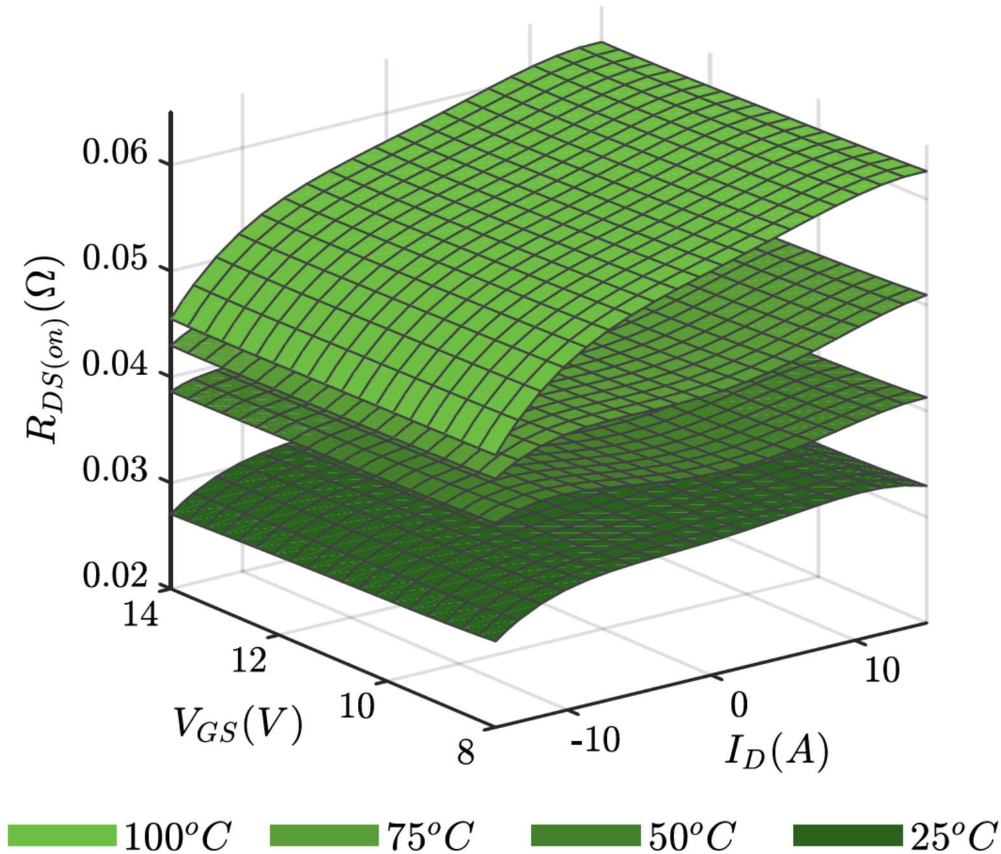

Fig. 2.4. Operating surfaces of R_{DSon} as a function of V_{GS} and I_D for different values of T_j [16].

Such advanced conduction loss assessment is a powerful tool for determining power dissipation in MOSFETs of LLC resonant converters. It provides information about conduction losses in any operating point of the circuit. Switching losses are reduced and I_D varies significantly during operation in this topology. Contrary to this method, the conventional information provided by the datasheet does not represent power losses adequately. Typically, it relies solely either on the dependency of the $R_{DS(on)}$ on Tj or on the dependency of the $R_{DS(on)}$ on I_D.

Since the conduction losses depend particularly on the on-state resistance of a MOSFET device, application designers usually attempt to reduce it by either employing MOSFET devices possessing lower $R_{DS(on)}$ parameter or by connecting several MOSFET devices in parallel. However, the reduction of the $R_{DS(on)}$ leads to the employment of larger devices possessing greater intrinsic parasitic capacitance which stores and then dissipates energy during each switching transition. Owing to this additional source of power-loss in all SMPS, a compromise between gate-drive switching losses and conduction losses needs to be reached in every particular application.

2.1.2 Switching Loses in Power MOSFET

As discussed in the previous section, real MOSFET devices do not have ideal characteristics and require finite times for the turn-on and turn-off transitions. Depending on the application and utilized MOSFET devices, the transition times may vary between tens of nanoseconds to micro-seconds. Despite the short semiconductor switching times, significant instantaneous power loss may occur in the semi-conductor devices during these switching transitions, resulting in extensive average power losses.

MOSFET devices are charge controlled. The conducting state of a MOSFET is determined by the charge on its gate and in its channel. The controlling charge must be inserted or removed in order to switch a MOSFET device on or off respectively; hence, both the switching times and the switching loss are influenced by the amount of the controlling charge. The output capacitances of semiconductor devices, the circuit leakage and stray inductances also store energy which is again lost in most converter circuits during the switching transitions, thereby increasing the overall system power loss.

The MOSFET switching transients and hence the resulting overall application efficiency is affected by several parameters represented in Fig. 2.5 illustrating an interface of a MOSFET driver and a power MOSFET [17]. The capacitive loading effects of the MOSFET are modeled by the C_{GS}, C_{GD} and C_{DS} capacitances. The gate resistance is modeled as R_G and the MOSFET driver output impedance as R_O. Further parameters essential for the power-loss estimation are the $V_{GS(TH)}$ threshold voltage and the V_{GP} "Miller" gate plateau voltage which may be obtained from the MOSFET datasheet. The C_{GS}, C_{GD} and C_{DS} capacitances are normally not listed in the MOSFET datasheet explicitly; instead, the C_{ISS} input capacitance, the C_{OSS} output capacitance and the C_{RSS} reverse capacitance is typically specified. The relationship between the above-listed capacitances is defined by the equations below:

$$C_{ISS} = C_{GD} + C_{GS} \quad (4)$$

$$C_{OSS} = C_{DS} + C_{GD} \quad (5)$$

$$C_{RSS} = C_{GD} \quad (6)$$

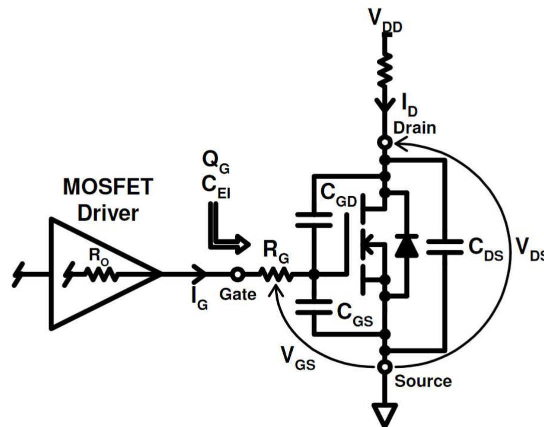

Fig. 2.5. Interface of MOSFET driver and power MOSFET [17].

The reason why MOSFET manufacturers specify C_{ISS} (input capacitance with $V_{DS} = 0$), C_{OSS} (output capacitance with $V_{GS} = 0$) and C_{RSS} (reverse capacitance with $V_{GS} = 0$) instead of C_{GS}, C_{GD} and C_{DS} in the MOSFET datasheets is that these parameters are directly measured. Nevertheless, by applying the equations (4), (5) and (6) the required parameters may be obtained.

Linearized turn on and turn off waveforms are depicted in Fig. 2.6 [17]. The assumption supporting the linearization is that the C_{GS}, C_{GD} and C_{DS} parameters are not voltage dependent, which is not the case precisely; however, such assumption may serve for obtaining approximate expressions adequately.

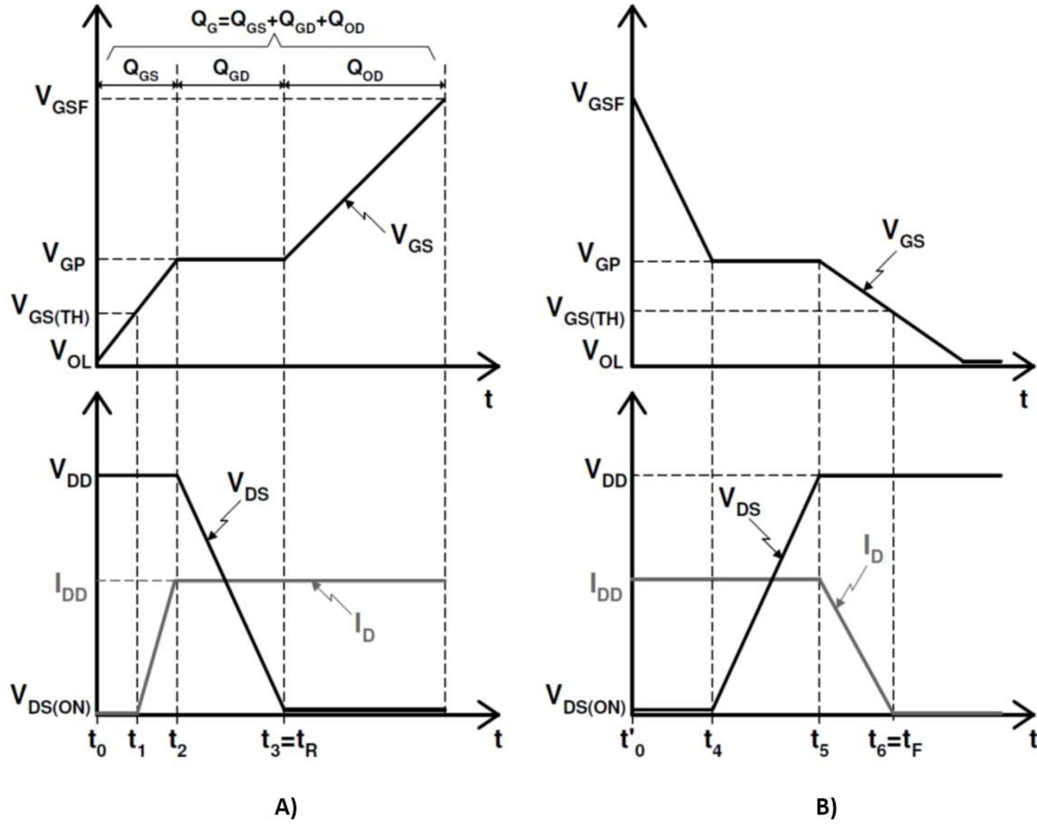

Fig. 2.6. Linearized switching waveforms. A) Turn on switching waveform. B) Turn off switching waveform [17].

Since the switching process takes place in the order of nanoseconds, the time events t_0 through t_R and t_0 through t_F do not represent static states but the crucial dynamic states which occur during the MOSFET turn on and turn off events.

At the t_0 time, the output of the MOSFET driver starts supplying the gate charging current, thereby increasing the gate voltage (V_{GS}). Essentially, no drain current (I_D) is conducted through the device until the V_{GS} attains the $V_{GS(TH)}$ threshold voltage at the t_1 time. At that moment, the channel enhancement begins and the device starts to conduct the drain current (I_D). The t_1 time is determined by the equation:

$$t_1 = (R_O + R_G) \cdot (C_{GS} + C_{GD}) \cdot ln\left(\frac{1}{1-\frac{V_{GS(TH)}}{V_{GSF}}}\right) \qquad (7)$$

Within the t_1 to t_2 time interval the gate capacitance continues charging and the I_D increases due to the increasing channel width. At the t_2 time the channel becomes adequately enhanced and the I_D drain current attains the I_{DD} final drain current. The time t_2 is determined by the equation:

$$t_2 = (R_O + R_G) \cdot (C_{GS} + C_{GD}) \cdot ln\left(\frac{1}{1-\frac{V_{GP}}{V_{GSF}}}\right) \quad (8)$$

In the t_2 to t_3 time interval the MOSFET operates in saturation region ($V_{GS} \geq V_{GS(TH)}$ and $V_{GD} \leq V_{GS(TH)}$). V_{DS} decreases and hence the C_{GD} discharges, resulting in a Miller Effect capacitance which is discharged by the available gate charging current resulting in an approximate constant V_{GP} voltage until the C_{GD} has fully discharged. I_D is approximately equal to I_{DD} and remains in proximity to the constant value in the t_2 to t_3 time interval. The $t_3 - t_2$ time interval is determined by the equation:

$$t_3 - t_2 = \frac{(V_{DD}-V_{DS(ON)}) \cdot (R_O+R_G) \cdot C_{GD}}{V_{GSF}-V_{GP}} \quad (9)$$

At the t_3 time the C_{GD} is totally discharged; therefore, V_{DS} is at its minimum and the MOSFET operates in the triode region ($V_{GS} \geq V_{GS(TH)}$ and $V_{GD} \geq V_{GS(TH)}$). From the t_3 time onwards the V_{GS} starts increasing again due to additional charging of the gate capacitance referred to as overdrive charging. The MOSFET driver gate charging current is essentially zero once the V_{GS} has reached its final value of the V_{GSF}. At this point, the MOSFET channel is entirely enhanced. Assuming that the voltage drop across the MOSFET channel ($V_{DS(ON)}$) is negligible, by utilizing equations (4) through (9) the t_1 to t_3 time interval, also referred as the rise time (t_R), at which the majority of turn on switching losses occur may be expressed as:

$$t_R = \frac{V_{DD} \cdot C_{rss} \cdot (R_O+R_G)}{V_{GSF}-V_{GP}} + (R_O + R_G) \cdot C_{iss} \cdot ln\left(\frac{V_{GSF}-V_{GS(TH)}}{V_{GSF}-V_{GP}}\right) \quad (10)$$

The turn off process of the MOSFET corresponds to the turn on process in reverse as illustrated in Fig. 2.6. Initially, the MOSFET operates in the triode region and the gate capacitance discharges until the V_{GS} attains the V_{GP} Miller Plateau voltage at t_4 time determined by the equation:

$$t_4 = (R_O + R_G) \cdot (C_{GS} + C_{GD}) \cdot ln\left(\frac{V_{GSF}}{V_{GP}}\right) \quad (11)$$

At the t_4 time the MOSFET starts to operate in the saturation region. In the t_4 to t_5 time interval the V_{DS} increases and hence the C_{GD} is charged by the available gate charging current resulting in approximately constant V_{GP} voltage until the C_{GD} has fully charged. Similarly to the turn on process, in this time interval the drain current I_D is approximate constant and equal to the I_{DD}. At the t_5 time the C_{GD} is entirely charged and the V_{DS} drain voltage is equal to the V_{DD}.

The t_4 to t_5 time interval may be expressed by the equation:

$$t_5 - t_4 = \frac{(V_{DD} - V_{DS(ON)}) \cdot (R_O + R_G) \cdot C_{GD}}{V_{GP}} \quad (12)$$

As the V_{GS} decreases, in the t_5 to t_6 time interval the gate capacitance continues discharging and the gate channel reduces. The I_D drain current descends and at the t_6 time equals essentially to zero. The t_5 to t_6 time interval is determined by the equation:

$$t_6 - t_5 = (R_O + R_G) \cdot (C_{GS} + C_{GD}) \cdot ln\left(\frac{V_{GP}}{V_{GS(TH)}}\right) \quad (13)$$

Similarly to the MOSFET turn on process, the majority of the switching losses occur in the t_4 to t_6 time interval, also referred to as the fall time (t_F), expressed by the equation:

$$t_F = (R_O + R_G) \cdot \left[C_{rss} \cdot \left(\frac{V_{DD}}{V_{GP}}\right) + C_{iss} \cdot \left(\frac{V_{GP}}{V_{GS(TH)}}\right)\right] \quad (14)$$

The approximate power MOSFET switching losses may be calculated as the sum of the turn on energy and the turn off energy determined by the equation:

$$P_{SW} = \int_0^{t_R} u_{DS} i_D dt + \int_0^{t_F} u_{DS} i_D dt = \left(\frac{t_R + t_F}{2}\right) \cdot V_{DD} \cdot I_{DD} \cdot f_{SW} \quad (15)$$

Equation (15) estimates the MOSFET switching power losses in converters employing hard switching principle which is typical for applications utilizing self-controlled asymmetric-blocking devices [18]. Besides the switching losses, other typical issues of hard-switched applications include:

- Device stress and hence thermal management,
- electro-magnetic interference (EMI) issues due to high dv/dt and di/dt transients,
- energy loss in stray inductances and capacitances.

Since the switching frequency of present day SMPS increases in order to reduce the weight and size of filter components, switching losses tend to predominate, causing the junction temperatures to rise. Advanced techniques are employed in order to obtain controlled turn-on and turn-off of the devices, such as:

- Employment of snubbers in order to shape switching trajectories,
- turn on and turn off speed control of the gate drive,
- optimization of circuit layout in order to reduce stray inductances, and
- soft switching.

Although the combination of snubbers, gate drive speed control or circuit layout may solve the EMI issues, the switching losses are typically not reduced. An efficient design employs the soft switching method discussed in the next section.

2.1.3 Soft Switching

As discussed in Section 2.1.2, the voltage and current overlap comprise the major source of the switching losses as illustrated in Fig. 2.6. The leading idea in the soft switching is to eliminate or significantly minimize this overlap, thereby substantially reducing the switching losses. Two methods are utilized in order to attain the soft switching:

- Zero voltage switching (ZVS),
- zero current switching (ZCS).

The principle of the soft switching utilizing the zero voltage switching and the zero current switching is illustrated in Fig. 2.7 [19]. In the ZCS, when the MOSFET turns on, the current growth may be delayed by series inductance. When the MOSFET turns off, the current is zero before the voltage is developed. In the ZVS, the MOSFET turns on or off when the voltage across the MOSFET channel is zero. An adequate candidate of the ZCS is the ZCS based DC to DC buck converter [20].

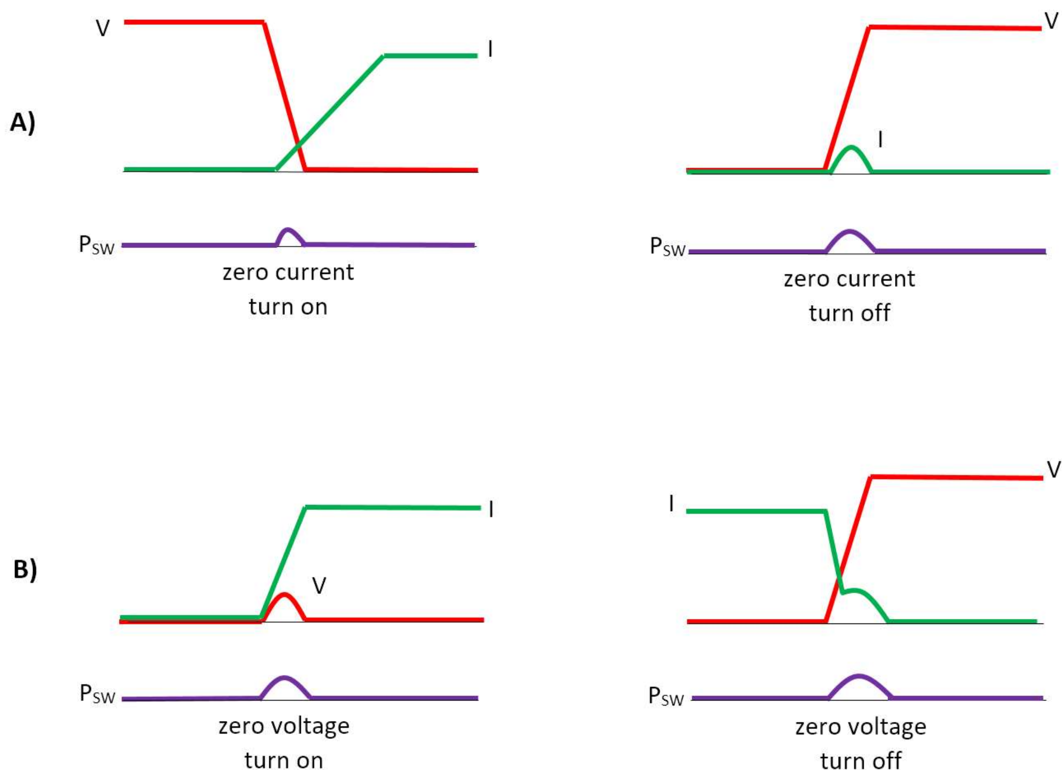

Fig. 2.7. Voltage and current waveforms of soft switching. A) zero current switching (ZCS). B) zero voltage switching (ZVS).

The zero voltage turn on is typically attained when the bypass diode is conducting. The zero voltage turn off may be achieved by employing a capacitive snubber which decelerates the MOSFET voltage development. The soft switching techniques employing resonant techniques to turn on at zero voltage and to turn off at zero current are typically utilized in ZCS buck converters. Both zero voltage turn on and zero voltage turn off are managed by the LLC resonant half bridge converter briefly discussed in the next section.

2.1.4 Soft Switching in LLC Resonant Half Bridge Converter

Switching converters that include a resonant tank circuit which actively participates in determining input-to-output power flow are generally referred to as resonant converters. It is no easy task to provide a comprehensive picture of all types of resonant converters; nevertheless, the property they share is a switch network typically producing a square-wave voltage that is applied to a resonant tank tuned to the fundamental component of the square wave. The tank responds primarily to this component and negligibly to the higher order harmonics, so its voltage and/or current is essentially sinusoidal or piecewise sinusoidal. Depending on the configuration of the resonant tank, the resonant converter may be referred to as series resonant converter (SRC), parallel resonant converter (PRC) or their combination – series-parallel resonant converter [21]. The LLC resonant half bridge controller represents a sensible candidate of such series-parallel resonant (SPRC) converter.

The representative circuit diagram of the LLC resonant half bridge converter is depicted in Fig. 2.8 [22]. The resonant tank consists of three passive components: The L_r series inductance, the C_r series capacitance and the L_m parallel magnetizing inductance. Although the converter diagram may imply that it is similar to the series resonant converter, the operation and characteristic of this converter with participation of L_m differs greatly from SRC.

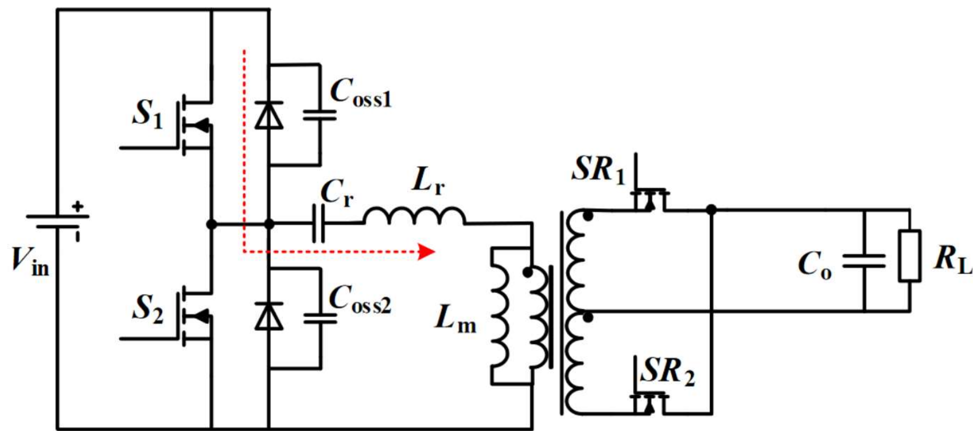

Fig. 2.8. Circuit diagram of LLC resonant half bridge converter [22].

Since the resonant tank is formed by three elements, two resonant frequencies are formed, both playing an important role in the converter operation.

$$f_1 = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{16}$$

$$f_2 = \frac{1}{2\pi\sqrt{(L_r+L_m)C_r}} \tag{17}$$

$$Q_s = \frac{\sqrt{L_r/C_r}}{R_l} \tag{18}$$

The DC characteristics of the LLC resonant converter in Fig. 2.9 [23] illustrates that the peak of the gain moves with the load change. Under the light load conditions, the peak moves towards the f_2 resonant frequency. Under the heavy load conditions, the peak moves towards the f_1 resonant frequency. The gain at the f_1 resonant frequency is always one and independent of the load change.

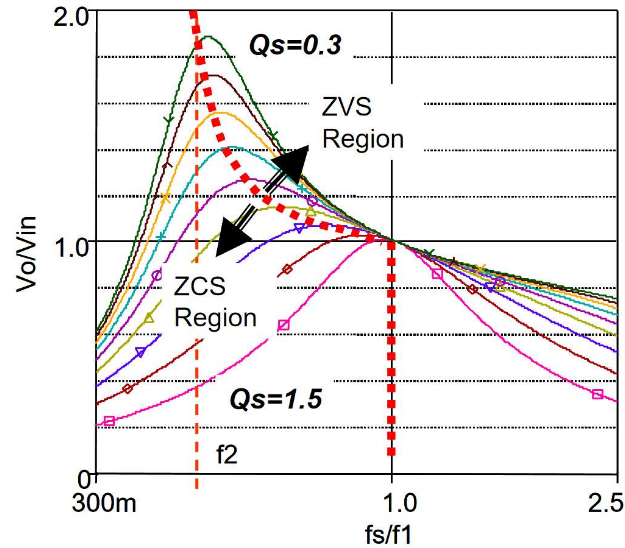

Fig. 2.9. DC characteristic of LLC resonant converter [23].

Fig. 2.9 also illustrates that the operation region is divided into two areas, ZCS and ZVS. When the switching frequency is higher than f_1, the converter always runs in the ZVS. When the switching frequency is lower than f_2, the converter always runs in the ZCS. When the converter operates between the f_1 and f_2 frequencies, the load condition determines whether the converter will run in the ZVS or the ZCS. For the application depicted in Fig. 2.8, the ZVS is preferred, since the MOSFET transistors are used as the primary switches. Therefore, the L_r and C_r values need to be selected in order to ensure that the converter operates in the ZVS under maximum load conditions at all times.

The input impedance of the resonant tank needs to be inductive in order to delay the resonant current behind the voltage of the resonant tank. Referring to Fig. 2.8, when the S_1 switch is turned off, the converter enters the dead time, forcing the both S_1 and S_2 switches off and the resonant current charges the C_{oss1} and discharges the C_{oss2}. The resonant current is conducted through the body diode of the S_2 switch. When the gate drive signal is applied, the voltage across the S_2 is limited to the voltage drop of the body diode thus the S_2 is able to attain the ZVS.

The phase angle between the resonant current and the resonant voltage needs to be adequately large in order to preserve the sign of the resonant current unchanged during the dead time; hence, after the rail-to-rail swing, the voltage on the midpoint of the half bridge structure does not oscillate until the second MOSFET is turned on. Otherwise, the capacitance associated to the midpoint (C_{HB}) would become recharged after its full discharge. The C_{HB} capacitance compounds of the junction C_{oss1} and C_{oss2} capacitances and stray capacitances such as the transformer intra-winding capacitance and the capacitance formed between the MOSFET drain and the heat sink. The value of the magnetic current must be adequately high in order to completely charge or deplete the C_{HB} within the dead time [22].

2.1.5 MOSFET Gate Driver Requirements

The general goal of SMPS systems is to reduce power consumption and heat dissipation, thus attaining high efficiency. Size and weight constrains are also of great importance in the standard consumer electronic field. The efficiency is essentially lessened by two sources of power loss associated with power MOSFET switches:

- Conduction losses,
- switching losses.

While the conduction losses depend particularly on the on-state resistance of a MOSFET device, the switching losses are linked to the switching process, specifically to the voltage and current waveforms developed on the MOSFET switch during turn on and turn off transients.

The conduction losses may be reduced by either employing larger MOSFET devices possessing lower $R_{DS(on)}$ parameter or by connecting several MOSFET devices in parallel. Not only the employment of large devices increases the gate-drive switching losses due to parasitic MOSFET gate capacitance which stores and then dissipates energy during each switching transition, but it may also increase the switching losses if the MOSFET gate driver does not possess ample sink and source current drive capability.

The switching losses may be reduced by altering the phase angle between the drain current and the drain voltage on the MOSFET device, thus achieving soft switching operation. Various techniques of employing resonant circuits in order to achieve soft switching exist and have been published. The LLC resonant converter is a suitable illustration of such designs broadly utilized in the standard consumer electronic devices, such as televisions, personal computers, etc. The gate drive current capability of the MOSFET gate driver for LLC resonant converters is typically of lesser importance because of soft switching operation. Since the LLC resonant converter uses typically the MOSFETs as the primary side switches, the ZVS operation is preferred. Moreover, the LLC resonant converters typically employ N-channel MOSFETs connected in a stacked configuration; hence, the high side gate driver operates against the midpoint, also referred to as the bridge point, thereby floating between the ground and the positive potential of the input high voltage rail. Communication between the high side driver and the low side control circuit must be ensured, utilizing high voltage translators. Precise delay and dead time matching between the low side and the high side gate drivers are the crucial parameters for the half bridge drivers employed in the LLC resonant converters.

It is evident that the MOSFET gate driver requirements are greatly driven by the target application. The pivotal parameters for the half bridge drivers which are the primary aim of this work are:

- Low input to output propagation delay,
- propagation delay matching between the low side and the high side gate drivers, implying
- fast communication between the low side control circuitry and the high side gate driver,
- galvanic isolation between the low side and the high side circuits for high-performance applications, and
- low stand-by current consumption.

2.2 High Voltage VLSI Fabrication Process

In order to manufacture integrated circuits (ICs) on monolithic semiconductor substrate, a semiconductor fabrication process needs to be utilized. Although Complementary Metal–Oxide–Semiconductor (CMOS) technology was patented by Frank Wanlass as far back as in 1963 [24], it is still the most common fabrication process for manufacturing devices that operate at low voltages. In order to integrate low voltage circuits along with the HV circuits mentioned in Section 1.1 which are directly connected to HV levels, additional process steps are needed to enhance the standard CMOS fabrication process. This work deals with two ON Semiconductor proprietary fabrication processes described in the following sections. In the first section, the VHVIC3 technology is presented. As discussed in the second section, the ONC25BCD technology may serve also for forming high voltage structures even without the high voltage process extension.

2.2.1 VHVIC3 Technology

VHVIC3 technology is applied for products employing AC-DC power conversion, thereby process and device design must be optimized for various voltage ranges such as 700V, 500V and 200V high voltage LDMOS and startup N-channel MOSFET, 60V resistors and bipolar transistors, 45V medium voltage LDMOS, 20V P-channel MOSFET and capacitors and 9V CMOS.

Integration of high voltage devices with low voltage devices on the same chip requires the use of a lateral double-diffused MOS (LDMOS) transistor. The VHVIC3 technology implements HV LDMOS (700V and 200V) by applying a technique known as RESURF (REduction of SURface Field) [25], [26]. This technique uses a shallow and precisely controlled N-well region under a carefully grown field oxide to produce a drift region designed to uniformly distribute the applied drain voltage laterally along the silicon/oxide interface in the drift region as shown in Fig. 2.10. The critical parameters affecting breakdown voltage in this technique are junction depth and doping profile of the n-well region, doping concentration of the substrate and the structure of the field shaping poly and metal flaps on the source and drain side. An optimization of these parameters allows for an optimum breakdown voltage versus on-resistance compromise.

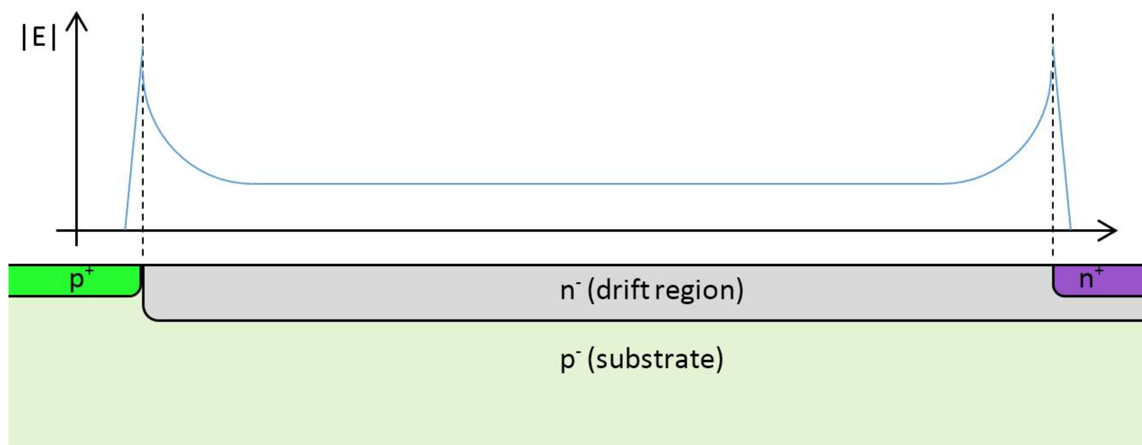

Fig. 2.10. RESURF Principle. The voltage drop is distributed along the drift region, thereby reducing the peak E-field in the blocking state.

The gate structure of the HVLDMOS device is fabricated by the DMOS or Double Diffused MOS transistor method [46]. This technique uses a single polysilicon edge to mask the channel/body region (called PHV) and the source N+ region (called NSD). The process drive-in times and temperatures for the two regions are designed to produce a tightly controlled delta between the lateral diffusion of the two regions under the polysilicon gate. The peak PHV concentration at the lateral junction of the PHV and NSD determines the threshold voltage of the device. A long drift region is required to support large breakdown voltage (60µm for 700V LDMOS and 14µm for 200V LDMOS). This results in a one-sided JFET device with lightly doped grounded substrate as the gate. It also results in large drift region resistance, which is a significant fraction of the total on-resistance.

A typical layout diagram of HV LDMOS is shown in Fig. 2.11. The source and gate structures are designed to fully enclose the high voltage drain island. This helps in isolation of the high voltage drain terminal and efficient use of real estate for current conduction. Bond pads are situated on the drain to provide access to the drain terminal of the LDMOSFET. High voltage interconnects may cause substantial breakdown voltage reduction and potential reliability issues and are not used for that reason. The schematic device layout shown in the figure features two fingers (the actual device possesses multiple fingers designed for a given current conduction capability), which results in one source fingertip and two drain fingertips [27].

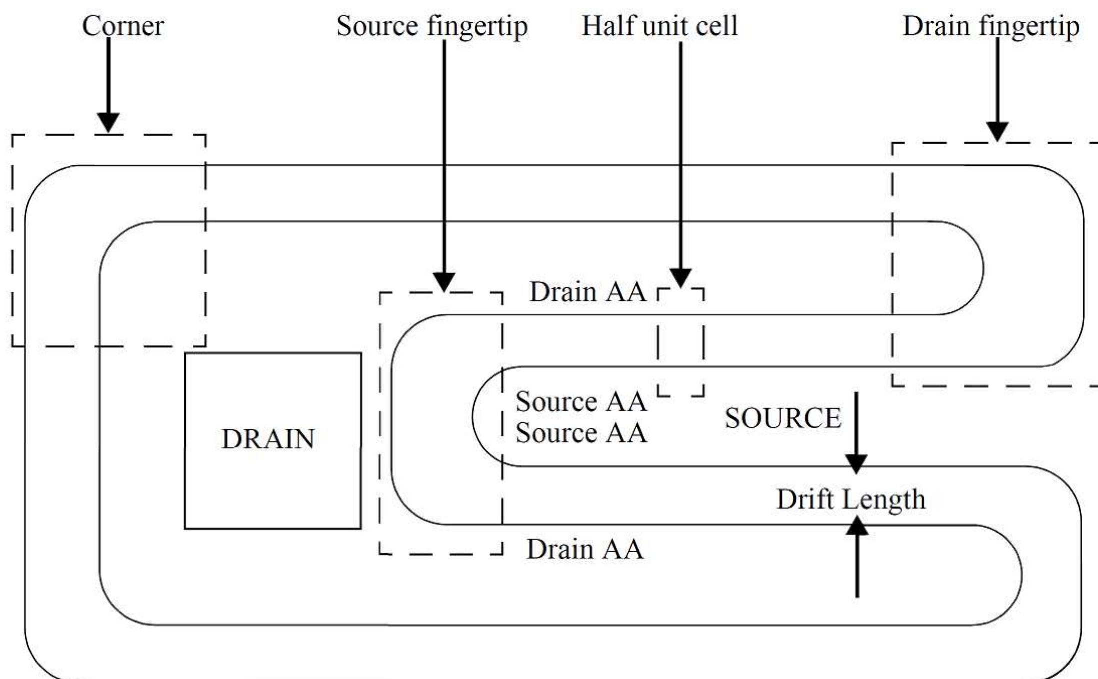

Fig. 2.11. Layout diagram of HV LDMOS. Fingertip design enables efficient use of layout area.

The surface electric field in the drift region of the LDMOSFET peaks near the edge of the drain and the gate metal field plates which is the consequence of the crowding of potential lines at these points. Electric field crowding at the field plate on the source side is further enhanced by the curvature at the source fingertip and similarly on the drain side at the drain fingertip. Owing to that, the breakdown voltage is generally limited by the fingertips. Correct design of the fingertips is therefore imperative in order to maximize

the breakdown voltage. Another fundamental problem in the LDMOSFET design is a large exposed length of the drift region which makes the device breakdown voltage sensitive to charging phenomena on the passivation surface. This may cause breakdown voltage instability which is manifested by considerable alteration of breakdown voltage values. The problem becomes even more serious in higher voltage devices, where the drift region needs to be extended to support the desired breakdown voltage.

The VHVIC3 technology features a twin-well process that provides CMOS, bipolar, and LDMOS devices at a 1μm technology level. The flow is a 15-mask process. The VHVIC3 flow monolithically integrates on the same chip:

- logic and analog functions,
- a start-up LDMOS transistor and
- a high-voltage power LDMOS transistor designed with a BVdss of 700V for a 240 VAC-line operation.

Other devices available from the VHVIC3 process flow include:

- NSD, PSD, PHV, Ptop, N-Well1 and N-Well1 + N-Well2 implanted resistors,
- polysilicon resistors,
- low-voltage CMOS logic,
- medium-voltage CMOS for analog functions,
- vertical and lateral NPN transistors,
- substrate PNP transistors,
- Zener and fusible Zener diodes,
- gate oxide capacitor,
- start-up LDMOS transistor,
- medium-voltage LDMOS transistor,
- high-voltage LDMOS transistor, and
- high-side driver.

Starting material for the VHVIC3 process is a high-resistivity (75-95 Ω-cm) p-type <100> float-zone wafer with 1.2 μm thick polysilicon backseal added in order to provide extrinsic gettering. The low substrate doping, in conjunction with a heavily doped NWell region (N-Well1 + N-Well2) and a Ptop that is diffused inside of this N-Well, provides the required BVdss of the HV double RESURF (REduction of SURface Field) LDMOS transistor. The twin-well process starts with an N-Well (N-Well1 and N-Well2) implant followed by annealing. Depending on the device requirements, the N-Well implants may be used in the above-mentioned combination or just N-Well1 only. The N-Well regions form:

- the body of the PMOS transistors,
- the base of the substrate PNP transistor,
- the collector of the NPN transistors,
- low and high-voltage resistors, and
- the drift region of the LDMOS transistors.

The N-Well implants are followed by the Pwell implant and a subsequent annealing. The P-Well regions form:

- the body of the NMOS transistors and
- provide isolation between devices.

The Ptop is implanted into the N-Well region prior to the creation of the active area.

The Ptop may be employed to form:

- resistors, the base of the NPN transistors,
- Zener diodes,
- capacitors and
- is used in the LDMOS transistors to achieve double RESURF performance.

The active area is defined using a LOCOS (LOCal Oxidation of Silicon) process growing 1.3 µm field oxide. The gate regions are formed by growing a 600 Å (gate) oxide and then depositing poly silicon on top of the oxide. The poly silicon is subsequently a heavily doped N-type.

As the next step, the PHV implant and drive are added to form:

- the body of the LDMOS,
- the drain of the medium-voltage PMOS transistors, and
- the base of the NPN transistors.

Subsequent PSD and NSD implants, followed by annealing, create shallow regions with high concentration of carriers. These implants form:

- the source and drain regions of the MOSFETs,
- the emitter of the bipolar devices,
- resistors, and
- ohmic contact regions.

The interlayer dielectric is formed by a 13 kÅ BPSG (Borophosphosilicate glass) layer. The metallization layers comprise the Al/Cu composite. The metal1 layer is 0.6 µm thick and the metal2 layer's thickness is 1.4 µm. TEOS (tetraethylorthosilicate) is used as the metal interlayer dielectric. The final passivation takes place employing 10 kÅ of PECVD (plasma enhanced chemical vapor deposition) nitride. Consequently, the wafers are background to the final thickness of approximately 14 mils. The backside metallization is optional, depending on the packaging requirements. An example of cross-section of several devices fabricated in VHVIC3 process is depicted in Fig. 2.12.

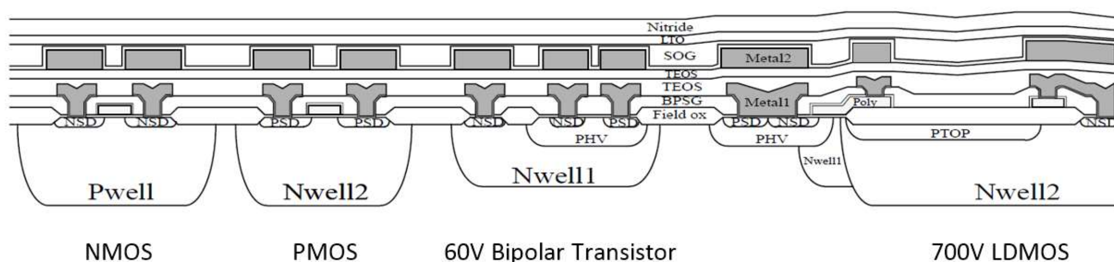

Fig. 2.12. Cross-section of several devices formed in VHVIC3 fabrication process.

As also shown in Fig. 2.12, in the VHVIC3 technology, the double RESURF high voltage LDMOS was carefully designed to sustain required voltage and to provide the lowest on-resistance in considering with the long term reliability performance. The double RESURF structure is formed by utilizing both the Ptop and Nwell2 layers, thereby decreasing the on resistance at the same breakdown voltage level [28], [29].

2.2.2 ONC25BCD Technology

The ONC25BCD technology features a N-buried-layer process that provides CMOS, bipolar, and LDMOS devices at a 250 nm technology level. The flow is typically a 20- to 25-mask process, depending on the selected process flow. The ONC25BCD fundamental flow monolithically integrates on the same chip:

- implanted resistors,
- polysilicon resistors,
- low-voltage CMOS logic,
- vertical NPN transistors,
- substrate PNP transistors,
- vertical PNP transistors,
- Zener diodes,
- gate oxide capacitors,
- inter-metal (MIM) capacitors, and
- medium-voltage LDMOS transistors.

In comparison with the VHVIC3 technology, the ONC25BCD technology does not utilize the LOCOS process for defining the active area. The active area is defined by the Shallow Trench Isolation (STI) process instead [30]. The resulting field oxide width is 4.5 kÅ. The cross-section of the available metal and dielectric layers in the ONC25BCD technology is illustrated in Fig. 2.13.

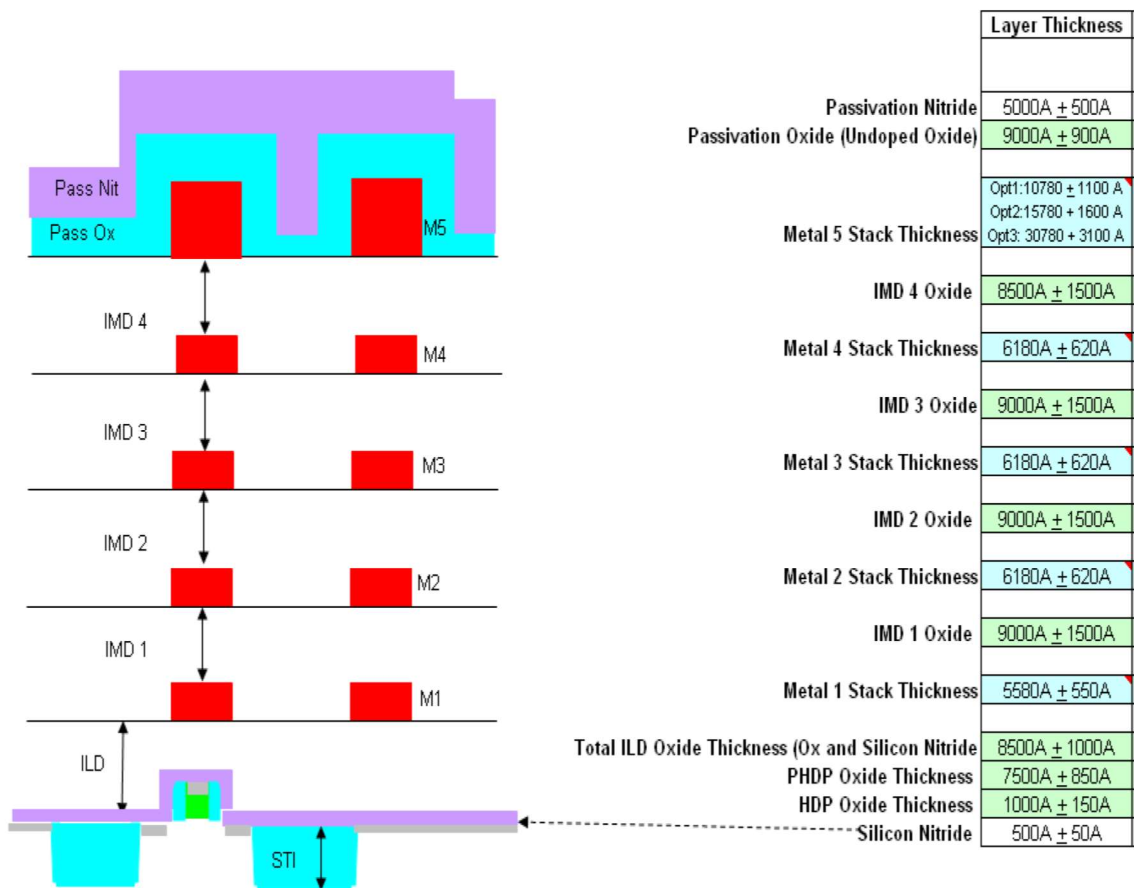

Fig. 2.13. Cross-section and vertical thickness dimensions of metal and dielectric layers in ONC25BCD technology.

The interlayer dielectric is formed by the HTCVD (high temperature chemical vapor deposition) nitride which is subsequently planarized by utilizing chemical mechanical polishing to 9 kÅ thickness. The metallization layers are formed by the Ti/Al/Cu composite. The resulting thickness of the internal metal layer is 0.6 µm. The top metal layer thickness is optional; the minimum thickness is 1 µm and the maximum thickness is 3 µm. Since each of the inter-metal dielectric layer is planarized, the ONC25BCD technology offers to employ a total of 5 metal layers. In the majority of products four metal layers are utilized. The final passivation is formed by 16 kÅ of the undoped silicon oxide and 7 kÅ of PECVD nitride layers. Depending on the packaging requirements, after the final passivation, the wafers are background to the final thickness and optionally the backside metallization is deposited.

The complex stack of the metal and dielectric layers also offers an alternative application to the standard routing purposes. Since the each metal-dielectric layer in the stack is planarized, the metal-to-metal dielectric thickness is given by the sum of the metal and dielectric thicknesses between the respective metal layers:

$$d_{MxMy} = \sum_{i=1}^{y-1} IMDi_{thk} + \sum_{j=x+1}^{y-1} Mj_{thk} \quad (19)$$

where d_{MxMy} is the dielectric thickness between x-th and y-th metal layers, $IMDi_{thk}$ is the i-th inter-level dielectric thickness and Mj_{thk} is the thickness of the j-th inter-level metal layer.

The silicon dioxide dielectric strength of 10^7 V/cm demonstrates the stability under high electric fields, suggesting that the oxide film is very suitable for dielectric isolation. Theoretically the two adjacent metal layers should withstand as high as 900 V differential voltage. But the theoretical value of the dielectric strength is considered as an intrinsic property of the bulk material, independent of the configuration of the material or the electrodes with which the field is applied. Several factors affecting the silicon dioxide dielectric strength exist [31], [32]:

- operation temperature,
- operation frequency,
- SiO_2 purity,
- structural perfection and thickness,
- the presence of a passivating phosphosilicate glass layer,
- the presence and reactivity of the metal electrode and,
- the duration of the post- metallization heat treatment.

Since the dielectric breakdown is dependent on the above-listed factors, various voltage stress profiles are mandated for isolation products which quantify their HV isolation performance. The performance of an isolator is quantified at the component level by parameters such as [33]:

- maximum repetitive peak voltage,
- working voltage,
- maximum transient isolation voltage,
- isolation withstand voltage,
- maximum surge isolation voltage, and
- comparative tracking index.

2.3 Current Development

In this section three monolithic HV structures used in HV switching applications are described. The first section deals with a device which may be used for both static measurement on high potential and supplying of low voltage circuits. The second chapter discusses an HV capacitor which can be used for level shifting or dynamic sensing on high potential. In the third section the high voltage level-shifter designed to shift a control signal from low voltage to high voltage potential is described.

2.3.1 High Voltage NMOSFET with Integrated Resistor Divider

The structure which can be used for both monitoring of HV level and for supplying low voltage circuitry is described in [34]. It is a high voltage NMOSFET device fabricated in VHVIC3 technology. The simplified cross-section useful for brief description is shown in Fig. 2.14.

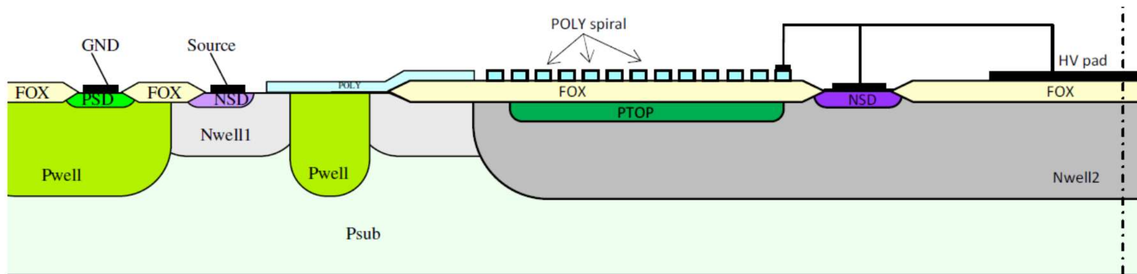

Fig. 2.14. Cross-section of HV NMOSFET designed to monitor HV levels and supply low voltage circuitry.

As discussed in Section 2.2.1, the bulk is a p-substrate with 75-95 ohm-cm resistivity. This resistivity is required for 1000V of intrinsic breakdown capability. The source and drain are formed from low-doped Nwell diffusions and are contacted via high doped NSD implants. To provide the lowest on-resistance with respect to long-term reliability performance of the NMOSFET device, the double RESURF (REduction of SURface Field) architecture was designed. It consists of an Nwell2 diffusion and a floating PTOP implant. The doping concentration of the Nwell2 diffusion is four times higher than that of the Nwell1 diffusion. The doping concentrations of both the NWell2 and the PTOP are designed so that the resulting space charge when depleted is the same as if only the Nwell1 was used. The NMOSFET channel is created from the Pwell diffusion, so it is not isolated from substrate. The structure is rotary symmetrical around the vertical axis drawn as a dot-and-dashed line.

Fig. 2.15 shows the layout of the structure. The drain is formed as a circular shape in the center of the device and the source creates an annulus on the outer edge. Fig. 2.14 and Fig. 2.15 also show the polysilicon spiral divider created over the drift region on the top of the field oxide (FOX). High resistive polysilicon of 5 kohms per square is used to minimize the current consumption. For the sensing purposes, the upper tap of the divider is connected to the drain and the lower tap is usually connected to potential close to substrate potential – see [34], [35]. Fig. 2.15 also shows a projection on the perimeter, which is a connection to the lower end of the drift region formed by the Nwell1 diffusion. In fact, the Nwell1 connection to the drift region forms a pinch resistor with pinch-off voltage of approx. 40 V. In application, this resistor is used for biasing the gate of the HV NMOSFET during operation.

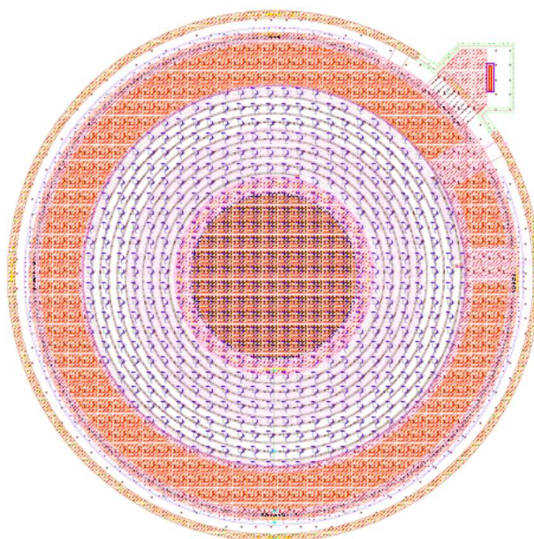

Fig. 2.15. Layout of HV NMOSFET dedicated for both HV level monitoring and supplying of low voltage circuitry.

The main benefit of such design is its area efficiency. By integration of the polysilicon divider into the HV NMOSFET device, the additional area which would be needed for forming of the HV divider is spared. A disadvantage of this design is that the potential which is distributed on the resistor divider must have almost the same behavior as the potential distribution in the drift region underneath to minimize potential difference across the field oxide. This leads to the necessity of holding the lower tap of the divider at potential close to substrate potential resulting in continuous current flow through the resistor divider. This can be an issue for applications where extremely low standby/no load power consumption is required.

Another challenging task is ESD ruggedness of such structure. Because BV (breakdown voltage) of the HV NMOSFET is approximately 700V, the device easily complies with the 200 V Machine Model. To comply with the Human Body Model, additional structure must be formed to protect the device.

The HV NMOSFET device with integrated HV divider as is described hereinbefore can be used for monitoring slow transients of input voltage only. It is well suited for detecting the Brown-Out condition when the power converter is disabled due to low input voltage on the supply line [8]. On the other hand, the device is not very suitable for dynamic or fast transient measurements due to high resistivity of the divider. The combination of high resistivity and all parasitic capacitances coupled to the HV spiral resistor distorts the transient response. One possible approach to overcome the divider ratio drop at high frequencies is to compensate the divider by capacitors. The difference between the compensated and non-compensated HV spiral divider is discussed in [36]. Nevertheless, even the compensated HV divider is not an ideal solution for fast transient measurement, because of non-zero current continuously flowing through the resistor. Therefore using solely the HV capacitor is the best choice for dynamic measurements.

2.3.2 High Voltage Capacitor

The integrated High Voltage Capacitor on monolithic silicon substrate can be used in various applications. Because the capacitance of such capacitor is usually within the range of 10 fF to 10 pF, only signaling purposes are applicable. The first application is monitoring dynamic signals. The second application is capacitive coupling element for galvanic isolation [37], [38].

Fabricating a high voltage capacitor on monolithic silicon substrate is not an easy task. Usually advanced process steps as LOCOS and SOI need to be used [39], otherwise the usage of such capacitor is somehow limited; for example, each capacitor needs to be fabricated on its own die because one of its terminals is the substrate [40].

One possible approach to form a high voltage capacitor is to employ a serial combination of few capacitors arranged laterally in annular configuration. This capacitor was developed and patented by ON Semiconductor [41]. The author of this work is also the co-author of this patent. The cross-section of such capacitor and the layout of the overall structure is shown in Fig. 2.16 and Fig. 2.17 respectively.

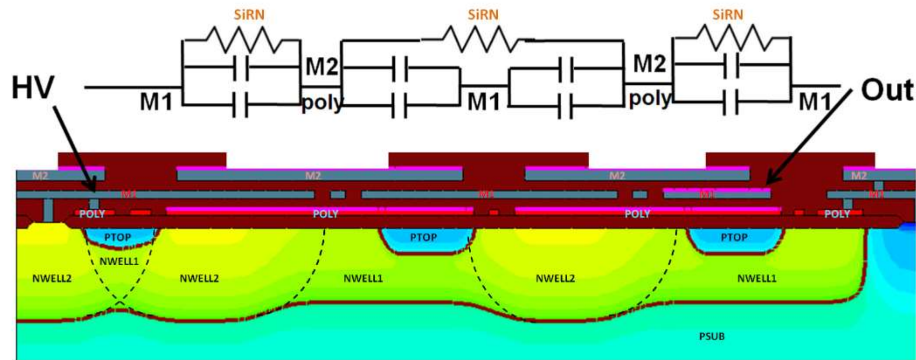

Fig. 2.16. Cross-section of monolithic HV Capacitor used for dynamic sensing.

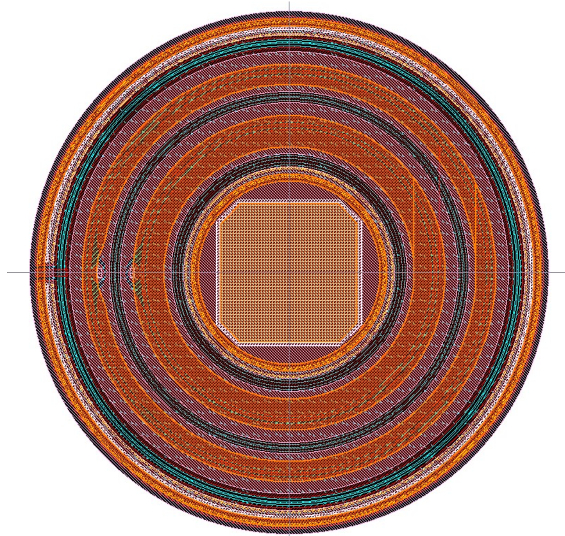

Fig. 2.17. Layout of HV Capacitor. Orange layer shows the passivation openings for interconnection between SiRN and Metal2.

In order to achieve the 700V breakdown, the HV capacitor is formed by four 200V capacitors in series. Each capacitor is formed as a parallel combination of Metal2 – Metal1 and Metal1 – Poly capacitor. The value of capacitance is the same for each of the four serial capacitors. PN junction is added to grade lateral potential under the capacitor. The Nwell is connected to HV potential through the schottky contact to avoid any parasitic injection when HV input is in reverse bias condition. Replacement of the schottky contact by ohmic contact is also possible if there is no risk of reverse bias condition. The charge must be properly balanced, which is managed by Nwell1 with concentric Nwell2 rings. The usage of one Nwell type with properly set doping dose is also possible. PTOP rings are added to the edges of lower Poly plates to optimally adjust the electric field.

It is necessary to have an HV potential equally divided between all four capacitors. Under dynamic conditions, this is ensured by the design, basically by the geometry of each capacitor. Under DC operation, potentials are balanced by using a semi-isolating layer. Silicon Rich Nitride (SiRN) passivation with cuts is used as the semi-isolating layer. Those cuts basically connect SiRN resistors to Metal2 plate of each capacitor, thereby creating high resistivity voltage divider. The voltage across each SiRN resistor is set by its geometry. The layout of the overall structure is shown in Fig. 2.17. The orange annuluses are the passivation openings providing the interconnection between the Metal2 plate and SiRN.

2.3.3 High Voltage Translation Device - Level Shifter

Especially in LLC applications, two switching transistors are connected in stacked configuration [42] also referred to as half-bridge configuration. Both the switching transistors are usually NMOSFETs and are external to the controller. In order to properly control the transistors, the controller is internally divided into two parts – the low voltage part – Low Side, and the high voltage floating part – High Side. The lower transistor in stacked configuration is controlled by the Low Side Driver and upper transistor is controlled by the High Side Driver. The High Side supply return is connected to the middle point of stacked configuration - Bridge Point - so the High Side power supply is floating and during the system operation switches between the ground and the positive supply with a magnitude as high as 600 V. The principle schematic of half-bridge switching power converter is shown in Fig. 2.18.

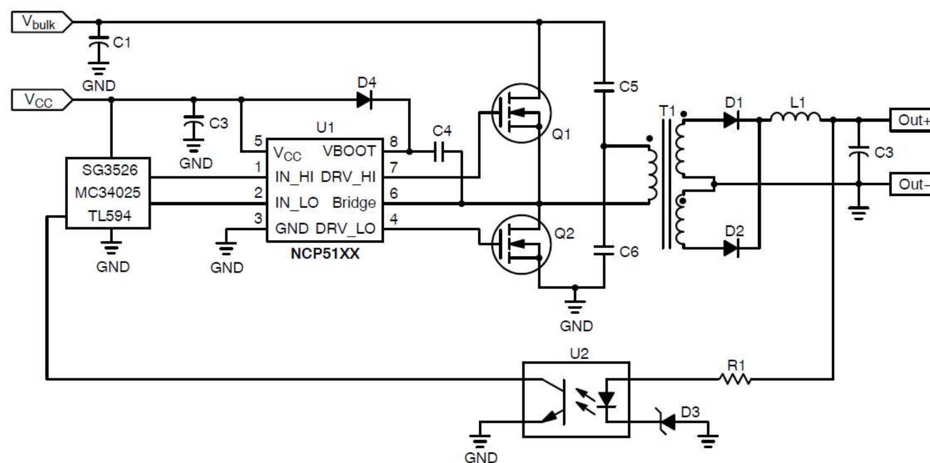

Fig. 2.18. Principle schematic of half-bridge switching power converter.

In order to control the on time and off time of upper transistor by the Low Side controller, high voltage level shifters need to translate the information from low to high potential [43], [44], [45]. Such high voltage signaling can be managed by high voltage LDMOSFET integrated into the HV isolation – see [46], Fig. 2.20. All the possible integrations in the floating high side region are also described in [6] and [47].

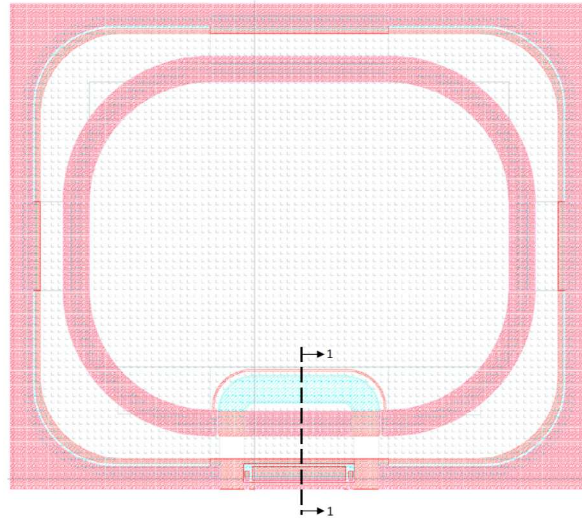

Fig. 2.19. 600V High Side isolation with integrated 600 V level shifter. The floating Nwell region is formed in the center.

High Side isolation with integrated HV LDMOSFET is shown in Fig. 2.19. The central region is filled by the Nwell diffusion to allow positive biasing up to 600 V against the substrate. The cross-sectional view taken along the line 1-1 of the HV LDMOSFET integrated into the High Side region is depicted in Fig. 2.20.

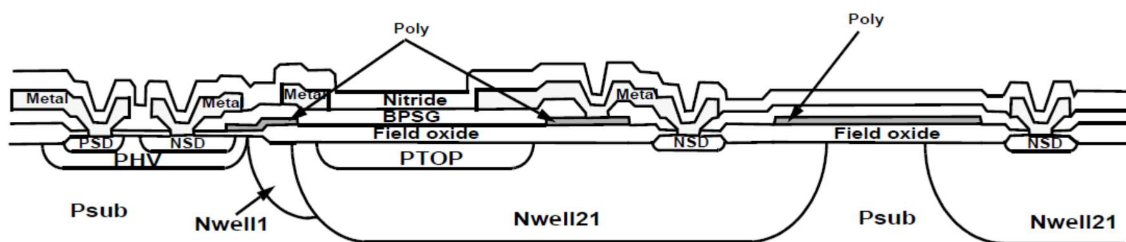

Fig. 2.20. Cross-section of HV LDMOSFET level shifter.

Two separated Nwell regions are shown in the cross section. The Nwell region on the right-hand side represents the central region in which the High Side circuitry is integrated. The Nwell region in the center of Fig. 2.7 is the drain of the HV LDMOSFET. Both Nwell regions are separated in the substrate both in X and Y axis. The width of the gap which isolates the two Nwell regions is wide enough to avoid a punch-through between the two Nwell regions. On the other hand, it must be narrow enough to maintain the depletion region underneath homogenous, thereby not affecting the BV of 600 V [6].

The advantage of such embodiment is that the whole half bridge controller can be minimized in its physical dimensions and integrated on monolithic semiconductor substrate. Lower robustness and a lack of galvanic isolation between high voltage and low voltage parts of application system represent the disadvantages.

It must be noted that such integrated monolithic design is dedicated for low-end applications only. In order to ensure galvanic isolation, one of the following methods of HV isolation needs to be used: Magnetic [1], piezoelectric [2] or dielectric [3], [4], [5].

The monolithic design also suffers from lower ruggedness to ESD. The BV of both the HV isolation and HV LDMOSFET is approximately 700V, so the device easily complies with the 200 V Machine Model. To comply with the Human Body Model, additional structure must be formed to protect the device.

2.3.4 High Voltage Sensing and Signaling Summary

In Section 2.3, three basic structures for both HV signaling and HV sensing which can be integrated on monolithic silicon substrate are discussed. All of them share one advantage – the manufacturing process need not be very complex, as usually several additional low doped diffused layers are added to a standard low voltage process in order to enable high voltage devices.

High Voltage NMOSFET with integrated resistor divider is commonly used for both HV sensing and supplying low voltage circuitry housed on the same monolithic substrate. The limitation of such design is represented by the trade-off between continuous current drawn by the resistor divider and its AC response. Higher resistance lowers the current consumption but at the same time slows down the AC response.

High Voltage Capacitor on a monolithic silicon substrate may be used for signaling purposes such as for monitoring of dynamic signals or as a capacitive coupling element for galvanic isolation [9], [13]. Compared to HV NMOSFET, fabricating a high voltage capacitor on a monolithic silicon substrate is more complex.

High Voltage Level Shifter is typically employed to translate the information from low to high potential regions on the same monolithic substrate [14], [15], [16]. It is commonly used in half-bridge drivers for low to middle power applications in consumer electronic. For industrial applications, galvanic isolation is often required.

2.4 Galvanic Isolation

Galvanic isolation is a design technique that separates electrical circuits in order to prevent current flow; no direct conduction path is allowed. Information or energy can be exchanged between galvanically isolated circuits by other means such as induction, capacitance or electromagnetic wave. Stray currents, such as differences in ground potential or induced currents, are blocked as illustrated in Fig. 2.21.

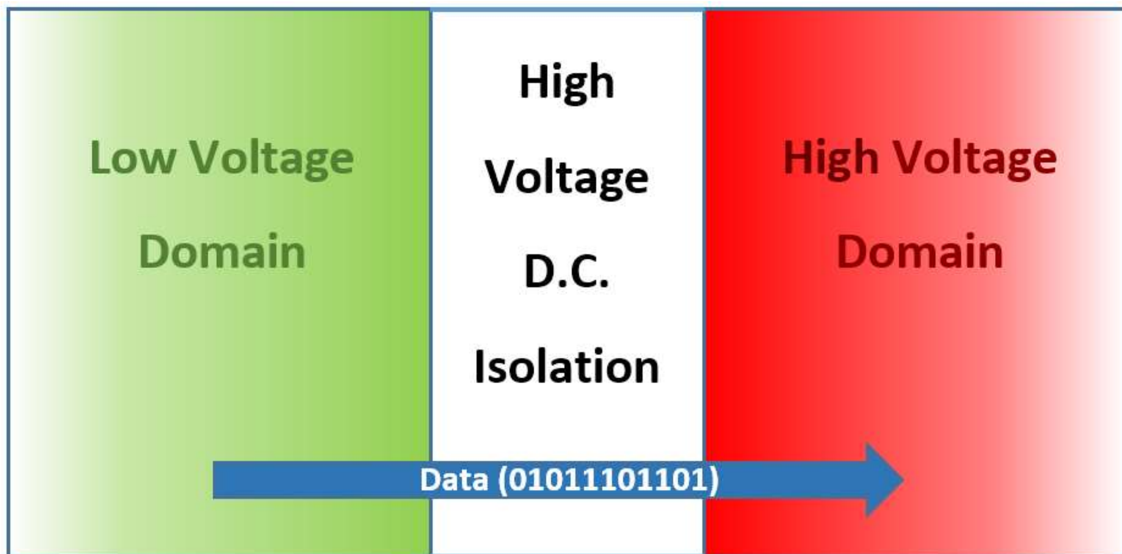

Fig. 2.21. Galvanic isolation. Information or energy is exchanged between galvanically isolated circuits. Stray currents are blocked.

Galvanically isolated communication is an emerging research area in integrated circuits, with various applications such as power management circuits, medical equipment, and network interfaces. The half bridge MOSFET gate driver, discussed in section 2.1, where there is a need for communicating a control signal from a low voltage die to a high voltage die is a sensible application of galvanic isolator. In this application, isolation rating and cost (manufacturing process, assembly steps, and chip area) are the paramount design specifications.

One of the following methods of HV isolation are typically employed in order to provide galvanic isolation:

- Magnetic [1],
- piezoelectric [2] or
- dielectric [3], [4], [5].

For single-package integration, magnetic coupling seems to be the most suitable, which is also apparent from the number of patents in this area. For monolithic design, a coreless planar transformer is optimally used [48], [49] and [50]. On the other hand, it might prove beneficial to invent a new approach which is still not patent-protected.

3 SIGNIFICANCE AND MOTIVATIONS OF THE THESIS

Section 2.3 discusses that the monolithic HV structures used in HV switching applications are not suitable for high-end applications. Such applications require galvanic isolation between power devices and control electronics.

1) Design of 800 V Galvanically Isolated Translator

The first aim of this Thesis is to develop a design of galvanic isolation which can be incorporated in HV applications that require either measuring high voltages or communicating between different voltage domains. In order to simplify the evaluation of the galvanic isolator, the development is divided into two consecutive steps:

- Design of galvanically isolated translator.
- Design of galvanically isolated HB driver for industrial applications.

The design of the galvanically isolated translator must be both cost-effective and easy to apply for follow-up development of fully galvanically isolated half-bridge drivers. The design is divided into three basic blocks:

- Transmission line,
- transmitter,
- receiver.

Transmission Line

The aim of this work is to introduce a novel design of a galvanically isolated translator using adjacently coupled resonators instead of the typical vertical transformer or a high voltage capacitor. In order to achieve low signal attenuation, all transmission line components, such as the adjacently coupled resonators, need to be tuned precisely to the same resonant frequency. In order to evaluate the signal attenuation, extra test structures must be designed:

- Capacitor value skews of the coupled resonators.
- Reduced transmission line with one coupled resonator removed.
- Transmitter generating pulse bursts.
- Transmitter generating continuous signal.
- Receiver outputting digital signal.
- Receiver outputting analog signal corresponding to received signal strength.

As a plus, as soon as the translator is tuned, it can be re-used in various designs with no changes.

Transmitter

The resonant frequency of the transmission line LC components is in the order of Gigaherz. The aim is to connect the transmitter oscillator directly to the first coupled resonator of the transmission line, thereby avoiding the need of using extra on-chip inductors.

Receiver
The low current consumption requirement disqualifies the commonly used low noise amplifier (LNA) from this application. Another design of an RF detector needs to be introduced.

Communication through the Galvanically Isolated Translator
The galvanically isolated domains need to communicate with each other via the means of digital signals. For that purpose, an AC carrier technique relying on modulation and demodulation needs to be used. Therefore, two blocks providing the communication must be designed:

- Modulator: In a modulator, the amplified input voltage modulates the carrier which passes the band-pass galvanic isolator.
- Demodulator: The carrier is demodulated after it passes the isolator. The modulation is filtered out and further amplified.

The important aspect here is current consumption and the resulting power loss of the system.

Physical embodiment of galvanic isolation and the design of both the modulator and the demodulator are the objectives of this work. To send and receive signals at frequencies in the order of GHz while keeping a very low level of transmitted energy, communication on discrete basis must be employed.

Design of Galvanically Isolated Half Bridge Driver for Industrial Applications
A multi-die approach has been chosen as the most suitable solution. Two parts of the half bridge driver must be designed:

- Low voltage die employing the transmitter,
- high voltage die employing the receiver.

For the very first experiment, only a one-way direction – from a low to a high voltage signaling – is intended.

2) Design of GI Translator for HV Applications Complying with the Safety Standards
In order to achieve as high galvanic isolation level as possible, as its second goal, this Thesis aims to introduce the design of a galvanically isolated translator utilizing two vertical transformers connected in series. In order to evaluate this concept, two structures are intended to be designed:

- Bidirectional digital galvanic isolator,
- analog galvanic isolator.

The aim of the bidirectional digital isolator is to investigate the possibility of using only one galvanic isolator for communication in both, low-to-high and high-to-low, directions.

The motivation to the analog isolator design is to enable full integration of primary and secondary side controllers in one single package.

4 DESIGN OF 800 V GALVANICALLY ISOLATED TRANSLATOR

In this chapter, the development of the high voltage level shifter replacement is described. Since the design utilizes the ONC25BCD technology discussed in Section 2.2.2, it is both cost-effective and easily applied in follow-up development of fully galvanically isolated half-bridge drivers. The design of the galvanically isolated translator is divided into three basic blocks:

- Transmission Line,
- Transmitter,
- Receiver.

In the first section of this chapter, the design of the galvanically isolated translator is introduced. In the remaining sections, the development of each of the three above-listed blocks is discussed in detail.

4.1 Galvanically Isolated Translator

The galvanically isolated translator utilizes lateral resonant coupling instead of stacked (vertical) coupling for CMOS galvanic isolators. Fig. 4.1 illustrates two laterally coupled inductors, where the oxide thickness between the two inductors is not limited by the ONC25BCD technology IMD thickness, but is instead determined by the horizontal spacing of the inductors determined by the layout. Although lateral coupling has been used in transmission line power couplers and RF power amplifier combiners, to the best of the author's knowledge, this case of CMOS lateral resonant coupling being utilized and investigated in chip-to-chip communication is yet unprecedented [51], [52].

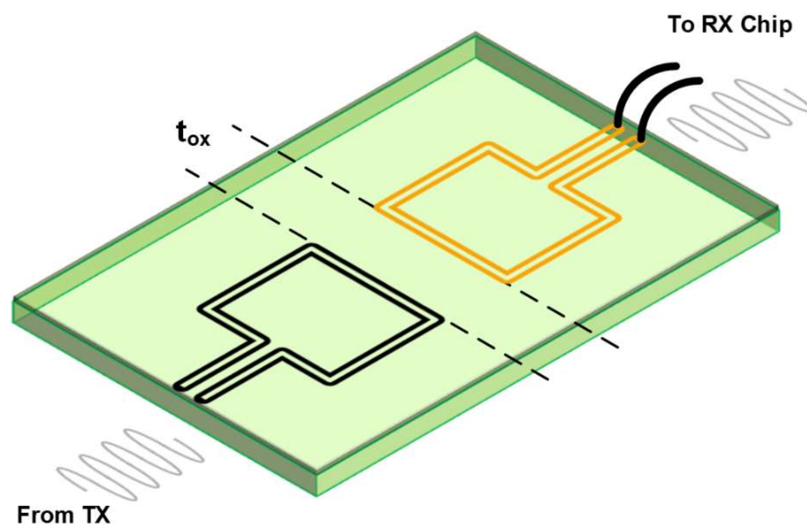

Fig. 4.1. Lateral coupling. Two laterally coupled inductors, the oxide thickness between the two inductors is not limited by IMD thickness.

The block diagram of the galvanically isolated translator is illustrated in Fig. 4.2. The transmitter modulates the input signal by generating RF voltage oscillating at 2.8 GHz. The RF signal is then coupled to the low voltage side of the transmission line and is propagated trough to the high voltage side of the transmission line. The receiver coupled to the high voltage side of the transmission line receives and translates the RF signal back to the logic signal corresponding with the input signal of the Transmitter.

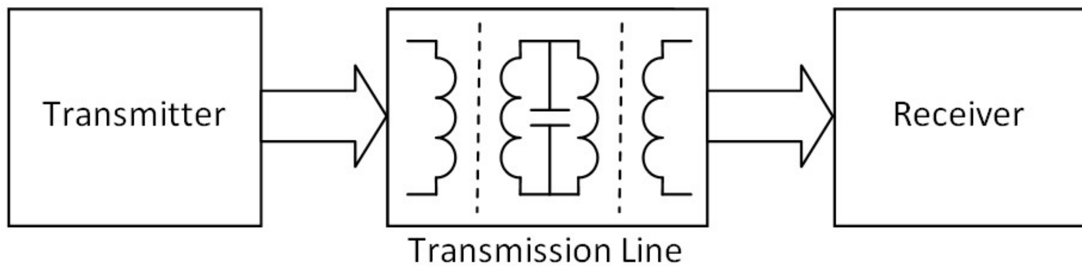

Fig. 4.2. Block diagram of galvanically isolated translator.

The fundamental concept in Fig. 4.2 has been prototyped as an integrated die-to-die system as shown in Fig. 4.3. The system includes two chips interconnected through two bond wires. The transmitter chip (Low Side Chip) is the low voltage die which may be integrated together with a controller. The receiver chip (High Side Chip) can be integrated with high voltage gate drivers and is immune to high voltage transients.

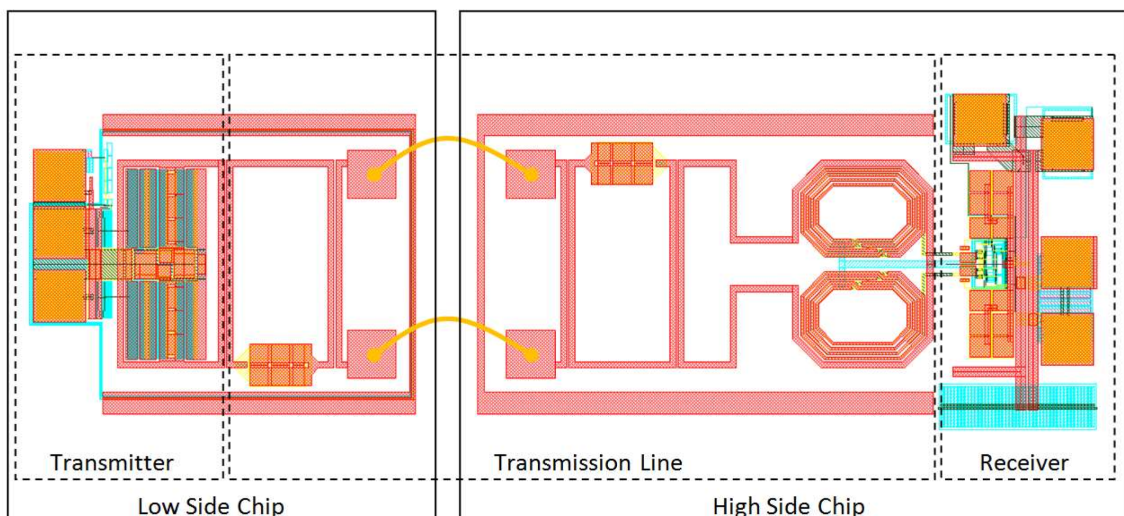

Fig. 4.3. Layout of galvanically isolated die-to-die translator.

Magnetic coupling between the transmitter, the first resonator loop and the inductor connected to the low side bond pads transfers the oscillator signal to the bond pads of the low side chip. Bond wires transfer the signal from the low side chip to the high side chip, where the RF signal is coupled to the primary coil of a center-tapped step-up transformer through the second resonator loop. The output of the transformer resonating with the receiver input capacitance delivers a differential signal to the receiver. The receiver is designed employing a fully differential topology in order to maximize the Common Mode Transient Immunity (CMTI).

Since the coupling of laterally positioned structures is weaker than vertical coupling, resonantly coupled inductors implemented as metal loops are employed in order to maximize the signal strength from the transmitter to the receiver. Generally, a weakly coupled transformer with primary and secondary coils having a coupling factor of k, equivalent inductance of L, series resistance of R, and quality factor of Q can be resonated with a shunt capacitance (C) to increase the transformer coupling to more than k, as derived [51]:

$$\left|\frac{V_o}{V_i}\right| \cong \frac{k}{\left|CL\omega^2(1-k^2)+\frac{R}{L\omega}j-1\right|} = \frac{k}{\left|\frac{1}{Q}j-k^2\right|} \cong kQ \qquad (20)$$

The implemented design is explained and the simulation results illustrating the functionality of the concept are presented in this chapter.

4.2 Transmission Line

The topology of the galvanically isolated translator is depicted in Fig. 4.4. As introduced in Section 4.1, this design utilizes adjacently placed coupled resonators with the gap between them filled with dielectric. By adjusting the spacing between the resonators, the HV isolation may be enhanced and controlled by both the distance between the resonators and the number of gaps/resonators. Employing multiple resonators allows for the distribution of the potential difference between two sides of the isolator over multiple gaps and thus improves the isolation capability and reliability of the isolator. Each of the dielectric gaps between the elements in the communication path enable additional voltage drop to achieve high galvanic isolation. The capacitances of each of the elements to the underlying silicon and to adjacent elements are engineered so that under high voltage transients between the transmitting and receiving sides, the voltage is more evenly split between each of the gaps.

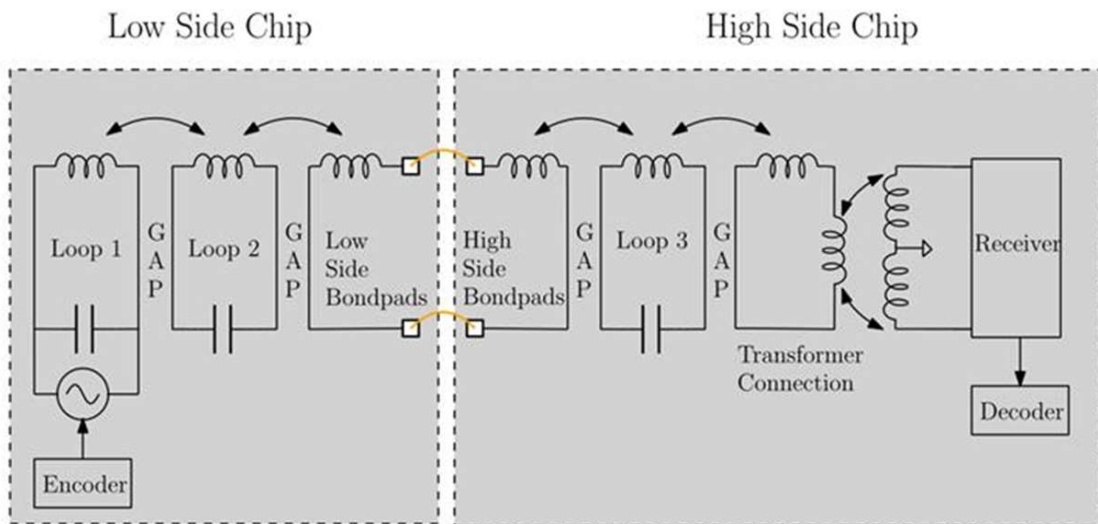

Fig. 4.4. Topology of galvanically isolated translator. HV isolation may be controlled by both the distance between the resonators and the number of gaps/resonators.

Resonance coupling allows for communication over the gaps between adjacent resonators with enhanced coupling resulting in less input to output signal attenuation. In addition the resonators' narrow bandwidth transfer function improves the noise immunity of the system. The resonant element offers two additional benefits: The out-of-band noise sources are filtered out and a minimum number of cycles is required to develop a detectable signal based on the Q of the resonator. The higher the Q is, the larger the number of cycles is necessary. Therefore, a single glitch is filtered out even though it is within the bandwidth of the resonator. It is improbable for a noise signal the likes of a glitch to meet both the frequency and the minimum time criteria simultaneously, which forms a very robust communication channel rejecting external noise.

The high Q system limitation lies in its increased delay time through the communication channel. Higher Q results in prolonging the propagation delay. The resonant frequency of each resonant element must be tuned precisely in order to attain minimum signal attenuation.

The differential transformer, also illustrated in Fig. 4.4, used on the receiving side and resonated with the transmitting frequency enables rejection of common mode noise. A step up transformer is utilized to enable increasing the voltage amplitude in order to reduce the gain requirements of the receiver.

The design of the transmission line system is partitioned into the three fundamental blocks which are examined in detail in the sections below:

- Fundamental resonator,
- bond-wire connection,
- center-taped solenoid differential transformer.

4.2.1 Fundamental Resonator

The fundamental resonator is formed by a metal loop and a Metal-Insulator-Metal (MIM) capacitor in series. The layout arrangement and its equivalent circuit schematic are depicted in Fig. 4.5.

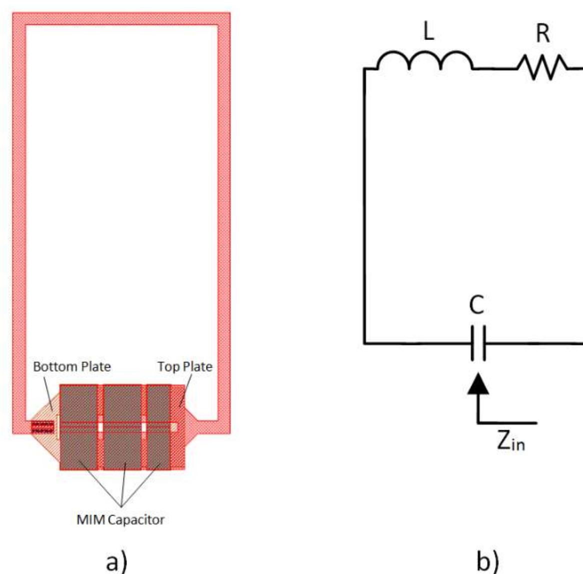

Fig. 4.5. Fundamental Resonator: a) layout arrangement, b) equivalent schematic.

The resonant frequency of the circuit in Fig. 4.5 b) can be found as [53]:

$$\omega_0 = \sqrt{\frac{1}{LC} - \frac{R^2}{L^2}} \qquad (21)$$

At resonance, the input impedance looking into the capacitor in parallel with the inductance loop is given:

$$Z_{in}(j\omega_0) = R_t = \frac{L}{RC} \qquad (22)$$

If the Q of the resonating circuit is defined as:

$$Q = \frac{\omega_0 L}{R} \qquad (23)$$

Then the relation

$$R_t = \frac{L}{RC} = R \cdot (Q^2 + 1) \qquad (24)$$

illustrates the impedance-transforming property of the circuit. The small resistance R is transformed to a larger value R_t when the circuit resonates.

The fundamental resonator structure shown in Fig. 4.5 has been optimized by employing an electromagnetic (EM) simulator designed for passive circuit modeling and analysis. The attained values of R, L and C are displayed in Tab. 4.1.

Tab. 4.1: Fundamental Resonator properties.

Parameter	Value	Unit
R	1.345	Ohm
L	588.8	pH
C	5.602	pF
R_t	75.62	Ohm
Q	7.371	-
$f_{resonance}$	2.748	GHz

The R, L and C values listed in Tab. 4.1 obtained by the EM simulator have been fine-tuned in the complete transmission line lump element model employing the Spectre circuit simulation software. The R, L and C lump elements have been tuned in order to attain sensible congruence between the simulated and the physically measured data, as discussed in Section 4.5.

4.2.2 Bond-wire Connection

The low side chip is connected to the high side chip via bond-wires as shown in Fig. 4.3. In order to simulate the transmission line performance during the design phase, a model of the bond-wire connection has been also obtained via the EM simulator. The schematic of the bond-wire is shown in Fig. 4.6.

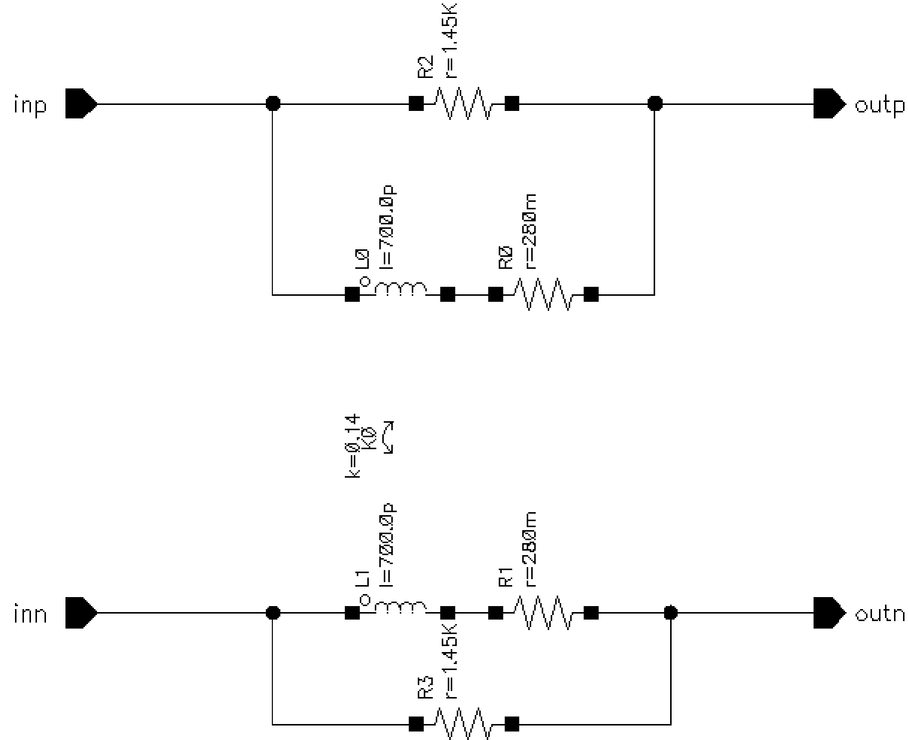

Fig. 4.6. Schematic of bond-wire connection between low side chip and high side chip.

4.2.3 Center-taped Solenoid Differential Transformer

The receiver input is connected to the final structure in the transmission line chain, which is the center-taped solenoid differential step-up transformer illustrated in Fig. 4.3 and Fig. 4.4. The center-taped solenoid differential transformer has been placed at the output of the transmission line for two purposes:

- In order to reduce the gain requirement of the receiver, and
- to provide a fully differential signal for the receiver.

Monolithic inductors generally occupy the largest portion of the die size area. Engineering of a step-up transformer is therefore challenging. In order to reduce the die size to a minimum, a solenoid structure similar to [54] has been utilized to attain maximum voltage gain of the transformer. The advantage of the solenoid structure is that the transformer windings are arranged vertically, employing all the metal layers available in the given process.

Since the receiver input is designed as differential in order to reject common mode signals, thereby enhancing the noise immunity of the system, the center tap of the transformer is connected to the high side chip ground and the windings drive the sources of the receiver input transistors.

As illustrated in Fig. 4.7 a), the transformer is formed by a one-turn inductor as the primary side winding and two inductor coils comprising eight turns connected to each other as the secondary side windings.

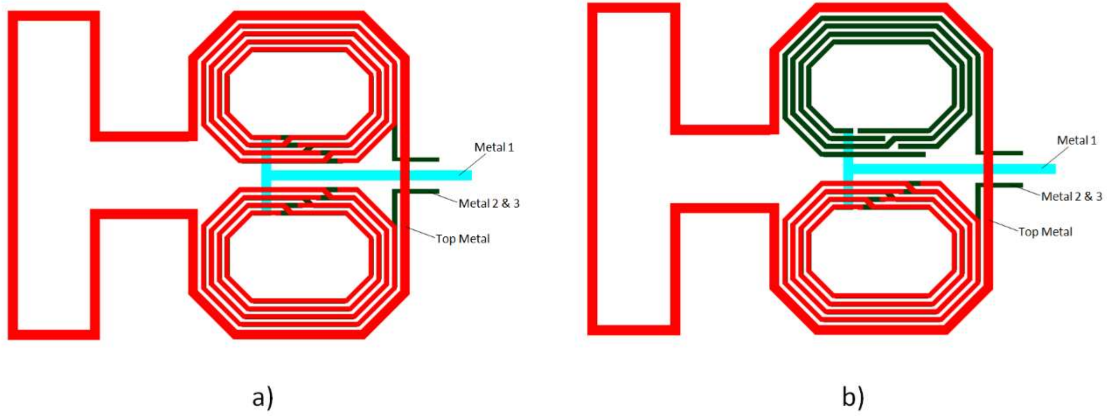

Fig. 4.7. Schematic of center-taped solenoid differential transformer: a) solenoid transformer layout, b) solenoid transformer layout with top metal removed from the upper inductor.

Fig. 4.7 b) depicts the transformer layout with the top metal removed from the winding of the upper inductor, revealing that the lower metal winding is connected in series with the upper metal winding. For the upper winding, the 3 µm top metal layer is employed; for the lower winding, both metal 2 and metal 3 layers are used in parallel in order to reduce parasitic resistance, because the inner metal layers are thinner than the top metal layer, as discussed in Section 2.2.2. The center tap of the transformer is connected via metal 1 layer, whose resistance is reduced by widening the wire. Metal interconnection layers (vias) are inserted in between the individual metal layers.

In order to increase the output to input voltage ratio, the transformer needs to operate at resonance. It has been extracted from the simulation that load capacitance of 195 fF ensures the maximum voltage gain of the system, which is 13.3 V/V. This is more than the transformer's turn ratio of 8 [51].

4.3 Transmitter

A complementary negative G_M oscillator has been utilized as the transmitter. The main benefit of such concept is that the primary inductance of the transmission line is also employed as the inductive element of the LC tank. A PMOS-NMOS cross-coupled pair generates negative conductance in order to compensate the input conductance seen from the output LC tank. Since the PMOS or NMOS cross-coupled pair generates conductance equal to $-\frac{1}{2}g_{mp}$ or $-\frac{1}{2}g_{mn}$ respectively, a complementary PMOS-NMOS stage has the advantage of generating conductance equal to [55]:

$$G_{OUT} = -\frac{1}{2}g_{mp} - \frac{1}{2}g_{mn} \quad (25)$$

Hence, the resulting conductance is the sum of the conductance of the NMOS and PMOS cross-coupled pairs connected in parallel.

Fig. 4.8 depicts the schematic of the transmitter. In order to turn the oscillator on and off based on the input signal (IN), two switches (M1, M4) are connected to the sources of the NMOS cross-coupled pair. An imbalanced drive of these switches employing the 300 ps delay accelerates the turn-on of the oscillator.

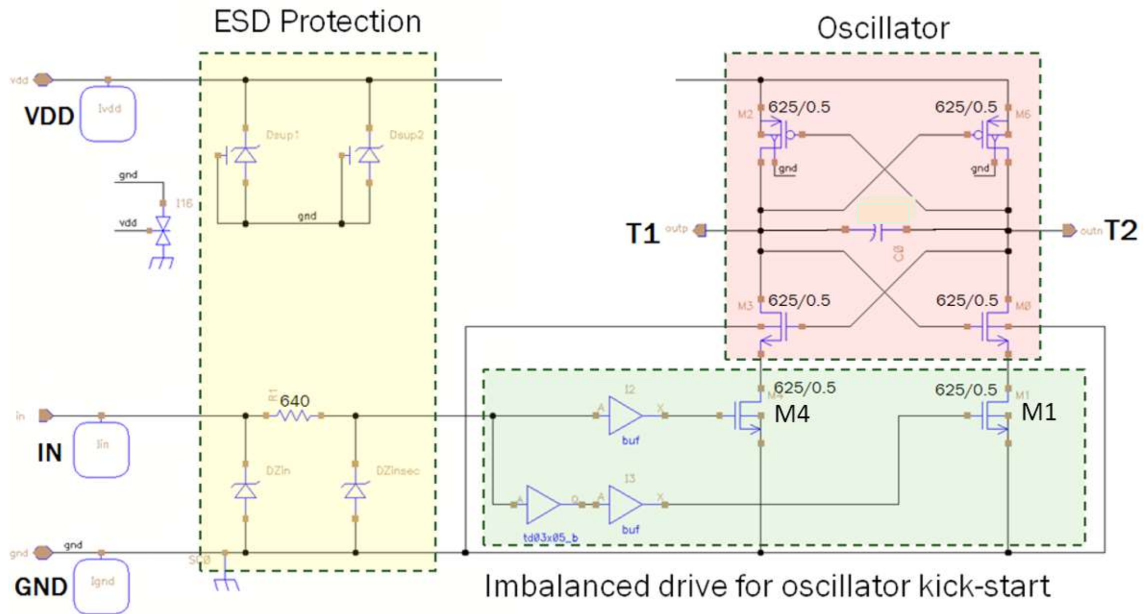

Fig. 4.8. Schematic of transmitter.

In order to minimize the die area, the oscillator transistors are arranged beneath the first loop of the transmission line, which also forms the passive LC tank of the oscillator. The low side chip layout with the highlighted location of the oscillator transistors together with the passive LC tank on the top of it is depicted in Fig. 4.9 a). The first loop of the transmission line with the MIM capacitors arrangement is illustrated in Fig. 4.9 b).

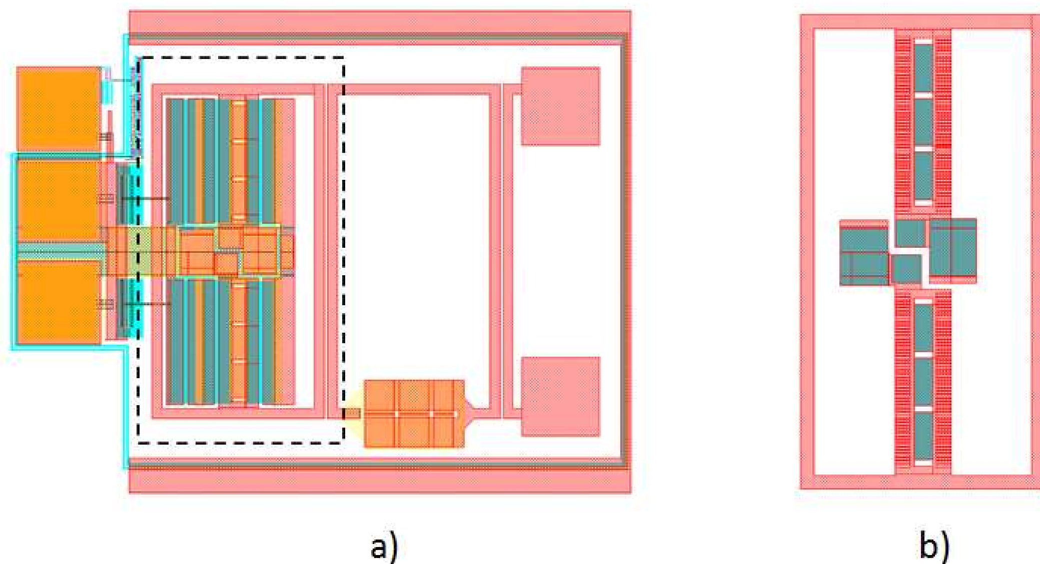

Fig. 4.9. Layout of the low side chip: a) oscillator location in dashed box, b) oscillator passive LC loop – blue rectangles represent MIM capacitors.

In order to operate at the optimum frequency (2.8 GHz), a total capacitance of 15.94 pF must be connected in parallel with the primary inductance of the transmission line. Two sources of capacitance are involved:

- The first source of capacitance is the active core of the oscillator – the four cross-coupled transistors. The SPICE simulation has produced the capacitance value of 10 pF.
- The remaining 5.94 pF is implemented as MIM capacitors connected between the positive and negative branches of the oscillator. These MIM capacitors are arranged beneath the metal connections highlighted by the blue rectangles in Fig. 4.9 b).

4.4 Receiver

In order to explain the circuit operation, the receiver is divided into two stages. The transmission line is connected to the first stage, which is the RF input stage of the receiver. In the second stage, the received signal is amplified and translated into a logic signal. Since precise reconstruction of the RF signal is not imperative in this application, a mere RF detector may be implemented, thereby attaining extremely low current consumption. Various common source RF input stages have been published [56], [57]. The main limitation of these designs lies in the employment of a Low Noise Amplifier (LNA) exhibiting high power consumption, which is undesirable for the presented application. Another detriment of typically utilized designs is the necessity of extra inductors, which brings additional model characterization effort and also substantially enlarges the receiver area.

The receiver, illustrated in Fig. 4.10, utilizes a cross-coupled differential pair as an RF detector in the first stage and a current amplifier in the second stage. Contrary to the typically utilized common source stage, the common gate stage may be employed in this design due to the fact that the output impedance of the transmission line is significantly lower than the input impedance of the receiver.

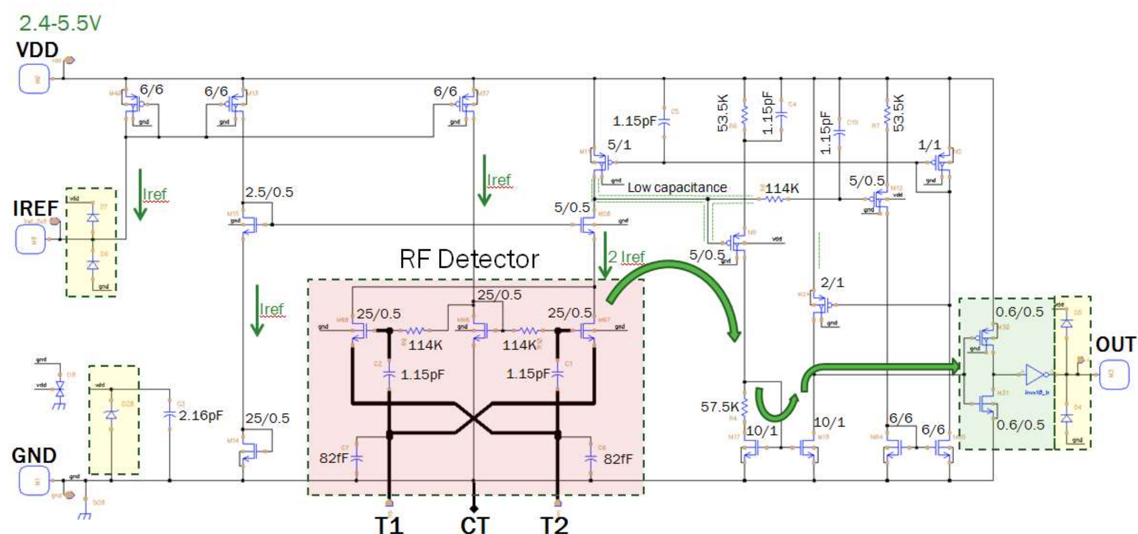

Fig. 4.10. Schematic of receiver. RF detector is utilized as the common gate stage.

The input impedance/capacitance is adjusted by the capacitors connected between T1/T2 and CT terminals in order to match the resonant frequency of the receiver input stage with the resonant frequency of the resonators forming the transmission line. The center-tapped transformer on the output of the transmission line is coupled to the RF detector of the receiver as shown in Fig. 4.3 andFig. 4.4. The center tap is connected to the CT terminal.

The RF detector as the first stage of the receiver is illustrated in Fig. 4.11. Nominal bias currents for the RF detector stage are set by the current mirror (M1, M2 and M3) according to the reference current conducted through the I_{REF} terminal. The M3 PMOS transistor supplies the bias current to the M4 NMOS transistor, thereby forming bias voltage for the M5 & M6 cross-coupled pair. The balanced configuration of the RF detector stage ensures that under quiescent conditions, the bias current is evenly divided between M5 and M6. The RF detector input terminals are connected to the sources of M5 and M6 which are capacitively cross-coupled via capacitors (C3, C4) to their gates, hence forming a rectifying full-wave differential input pair, with M5 and M6 conducting the negative and positive half-cycles of the received RF signal. This results in a full-wave rectified current that has a frequency of 5.6 GHz, which is twice as much as the carrier frequency. The RC parasitics and the limited frequency response of the M9 and M10 transistors provide a low-pass frequency response at the M9 drain node (N1). This low-pass response filters the rectified current to provide an envelope current, I_{ENV}. Since the input pair of the RF detector is cascoded by M9, the presence of an RF signal increases the current of M9 from its quiescent value (I_Q) to a total of $I_Q + I_{ENV}$. The total current value of M9 is compared with the quiescent value I_Q, and the difference is amplified in the second stage.

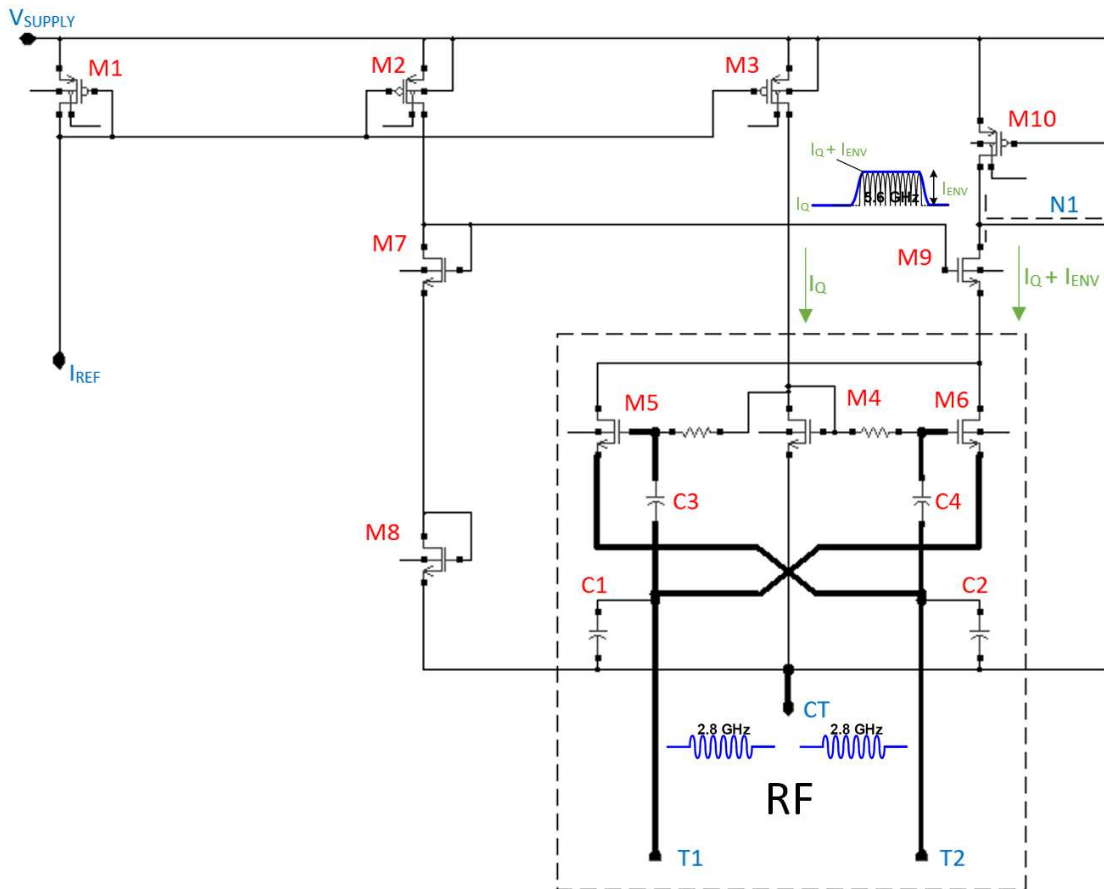

Fig. 4.11. Detail of the first stage of the receiver – RF detector.

In comparison to traditional LNA designs, the bias current of the RF detector is significantly lower, since the current which is subsequently amplified in the second stage is conducted from the transmission line.

Since the M5 & M6 cross-coupled pair forms a differential amplifier, any common mode component of the signals on T1 and T2 preserves the balance in the division of the bias current and also preserves the V_{GS} of the M5 and M6 NMOS devices; and hence, only a differential signal is amplified, thereby attaining a highly desirable CMTI of the receiver.

The second stage of the receiver is depicted in Fig. 4.12. The reference current (possessing the quiescent value I_Q) conducted by M10 is generated by the feedback system formed by M10, M11, M12, M13 and M14 transistors. The feed-back system regulates the M10 current in order to achieve a value equal to the current conducted by M9 under quiescent conditions. The V_{DS} voltage of M10 is regulated to a value given by $I_Q \times R3$ plus V_{GS} of M11 through the M11, M12, M13 and M14 feedback network transistors. By employing the feed-back system, the value of the current conducted through M10 is exactly equal to the I_Q quiescent current conducted through the M9 cascode transistor, thereby minimizing the required I_{ENV} envelope current to be detected. The value of the V_{DS} voltage of M10 is adjusted to maintain M9 and M10 in saturation regime during idle mode, which minimizes parasitic capacitance coupled to the N1 node, thus reducing the propagation delay of the receiver.

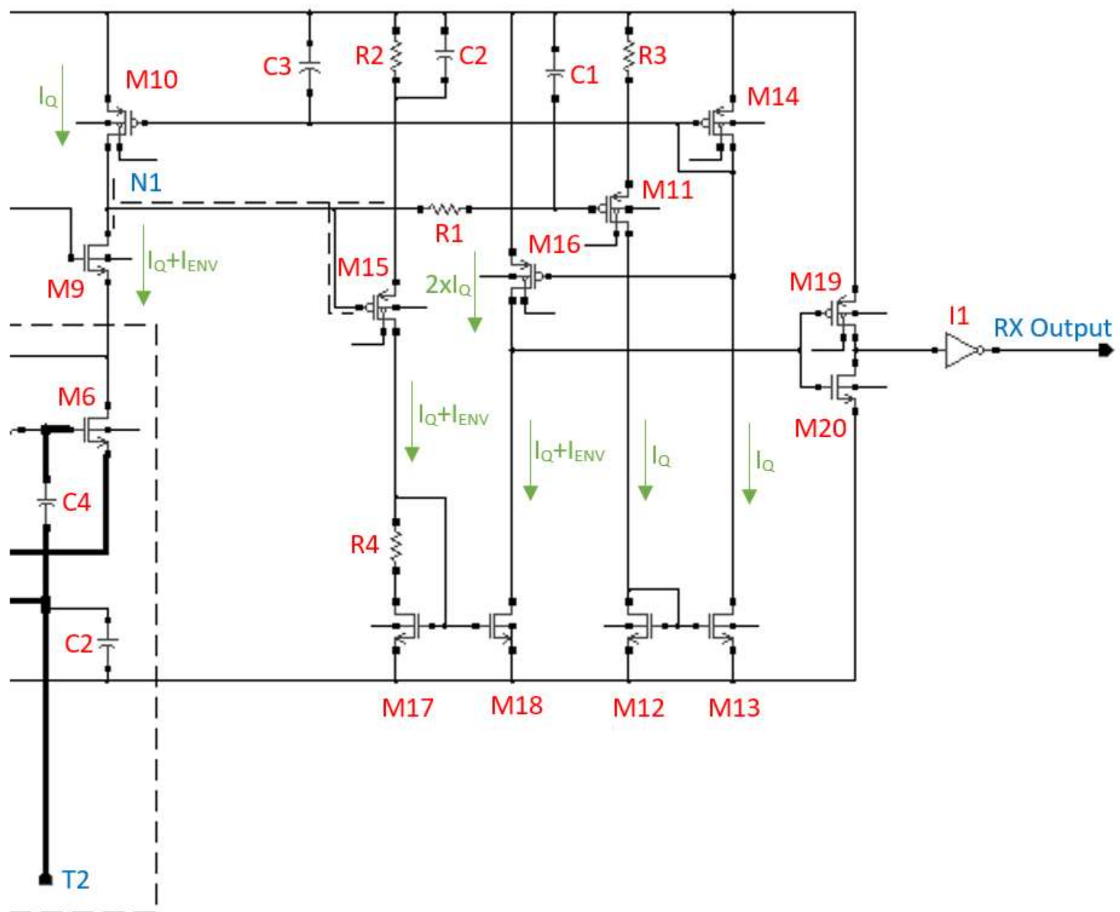

Fig. 4.12. Detail of the second stage of the receiver – amplifier of the received RF signal.

In order to further increase the RX sensitivity and minimize the power consumption in the idle mode, the feedback network also regulates the input transistors (M15, M16) of the current comparator to their threshold voltage. Higher RX sensitivity also reduces the propagation delay, since fewer number of RF input cycles are needed to develop voltage above the RX detection level.

The DC nature of the reference current is provided by the R-C filter (R1, C1) connected to the gate of M11. When receiving, M9 conducts current equal to I_Q+I_{ENV} and the difference between the M9 current and the reference current is amplified in the second stage by the current comparator. The current comparator inputs are formed by the gates of M15 and M16. While M15 is regulated in order to conduct the current of I_Q, the M16 transistor conducts current given by $2\times I_Q$, since M16 is designed twice larger than M15. Such configuration forces the output of the current comparator into the high state (no RF detection) under quiescent conditions.

Upon RF reception, the M15 current is allowed to increase due to the high-pass filter response formed by R2-C2, while the M16 current is maintained at $2\times I_Q$. Hence, the feedback network ensures that the current comparator always compares the change in the current due to the RF signal (I_{ENV}) with the quiescent current value (I_Q). Current amplification of the envelope signal is performed through the M17 & M18 transistors and the R4 resistor. The insertion of the R4 resistor forces a non-linearity into the M17-M18 current mirror, thereby amplifying the differential signal. Under quiescent conditions, the voltage drop on the R4 resistor is given by $I_Q\times$R4. The value of the R4 resistor is adjusted in order to form such a voltage drop that M17 remains operating in saturation regime and hence the value of the current conducted through M17 is mirrored as the identical current conducted through M18. When an RF signal is applied, the I_{ENV} current increases the current conducted through M17 and R4. The voltage drop developed on the R4 resistor increases the VGS voltage of M17 and M18, thereby forcing the M17 and M18 transistors into the triode region.

The current to voltage conversion is performed on the output stage of the current comparator formed by the M16 and M18 transistors. The voltage output of the current comparator is provided to the inverter (I1) in order to form a digital output. The inverter is subsequently followed by buffering inverters (not depicted in Fig. 4.12) in order to provide the driving capability for driving either the input capacitance of the oscilloscope or off-chip decoder circuit.

The presented design of the receiver has been patented by the author of this work [58].

The simulation results illustrating the receiver response to the input RF signal are depicted in Fig. 4.13. The amplitude of the differential RF signal between the T1 and T2 terminals is set to approximately 30 mV in the simulation test. The RF signal bursts are 50 ns long and the detection latency time of the receiver is approximately 15 ns.

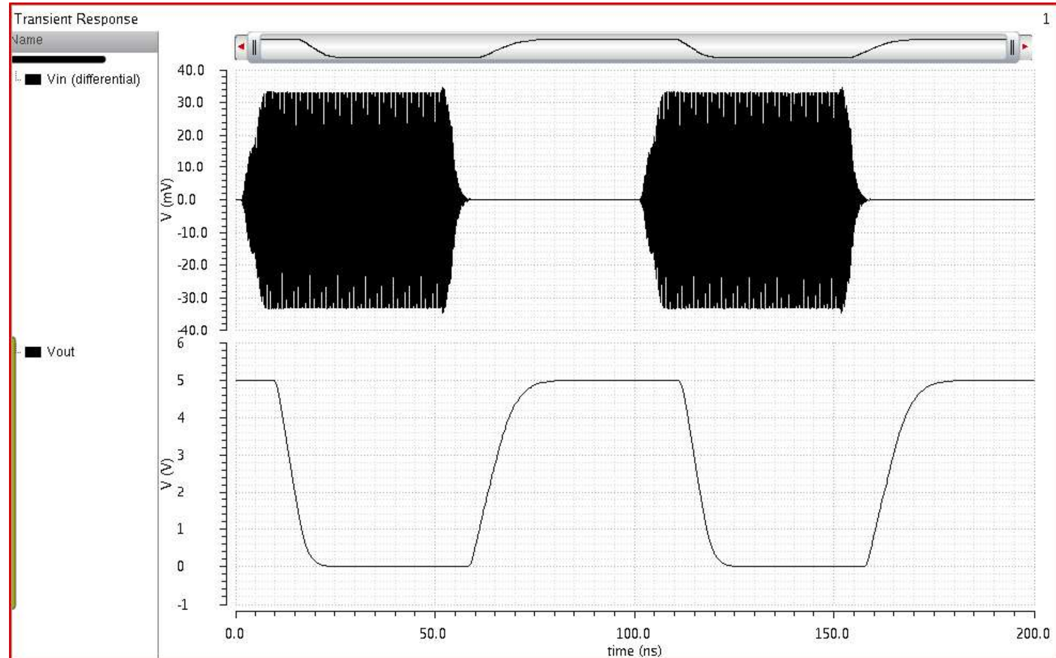

Fig. 4.13. Simulation results of the receiver. In response to 30 mV input differential signal, detection latency of the receiver is 15 ns.

4.5 Physical test structures

The previous sections imply that in order to attain low signal attenuation, all transmission line components, such as the adjacently coupled resonators, need to be tuned precisely to the identical resonant frequency. Also a digital-to-RF scheme must be considered, since it represents the major contributor to current consumption of the galvanically isolated translator system. In order to evaluate the signal attenuation, as well as the viable communication scheme, extra test structures have been designed:

- Capacitor value skews of the coupled resonators,
- reduced transmission line with one coupled resonator removed,
- a transmitter generating pulse bursts,
- a transmitter generating a continuous signal,
- a receiver outputting a digital signal, and
- a receiver outputting an analog signal corresponding to received signal strength.

In the following sections, each of the above-listed structures is discussed; simulation results and the physical measurement values are compared. In Section 4.5.1, the simulation model of the transmission line is introduced, since it poses the essential part during the design of the 800 V galvanically isolated translator.

4.5.1 Transmission Line Model

As discussed in Section 4.1, the galvanically isolated translator is divided into the low side chip and the high-side chip, both interconnected by bonding wires. Therefore, the model of the transmission line is divided into three model's subsets:

- Low-side part of the transmission line model,
- high-side part of the transmission line model, and
- bond-wire connection model.

An s-parameter-based model of each of the above-listed parts has been extracted by employing an EM simulator in the first phase of the model development. The s-parameter-based models have been then utilized in order to synthetize lump-element models which have been tuned according to the measurement results on the physical structures. The lump-element models of the low-side part and the high-side part of the transmission line are illustrated in Fig. 4.14. Each of the magnetically coupled blocks of the transmission line is represented by a separate lump-element model in order to simplify the model tuning and to provide greater insight into the system relations.

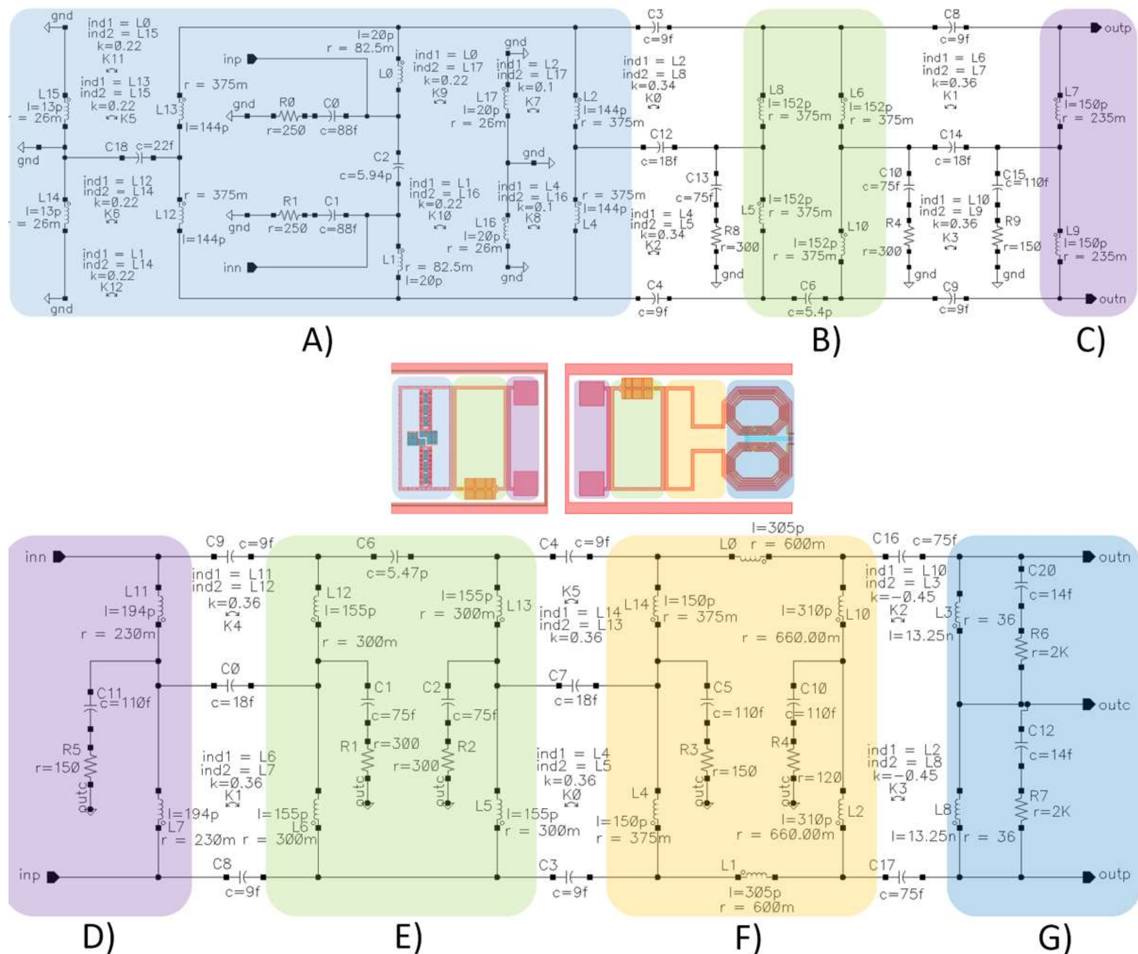

Fig. 4.14. Lump-element models of low-side and high-side part of transmission line. Individual parts of transmission line are highlighted: A) Oscillator loop. B) Fundamental resonator. C) Low-side half of bond-wire connection loop. D) High-side half of bond-wire connection loop. E) Fundamental resonator. F) Primary side of center-taped transformer. G) Secondary side of center-taped transformer.

4.5.2 Receiver Outputting Analog Signal

Since on-chip direct measurement of RF signal attenuation is not possible, a dedicated receiver outputting analog signal representing the RF signal strength has been designed. Its schematic diagram is illustrated in Fig. 4.15.

The receiver outputting digital signal is in greater detail described in Section 4.4. Minimizing the parasitic capacitance coupled to the N1 node is not imperative, since the minimal propagation delay is not the aim in this receiver application. Therefore, the active load formed by the M10 transistor in Fig. 4.11 is replaced by a resistor (R_{SENSE}), which enables measuring the RF signal strength as a voltage drop developed on the R_{SENSE}. The N1 voltage is provided to the output by an operational amplifier (OA) in order to provide the driving capability for driving the input capacitance of the oscilloscope probe.

Supposing V_X is the differential voltage on the RX output between the quiescent and reception mode, then the amplitude of the RF signal on the receiver differential input (T1, T2) is given by:

$$V_{AMP} = \sqrt{\frac{V_X L}{2\mu C_{OX} W R_{SENSE}}} \qquad (26)$$

where μ is the charge-carrier effective mobility, W is the gate width, L is the gate length and C_{OX} is the gate oxide capacitance per unit area. Thus, the signal attenuation of each transmission line test structure may be evaluated by connecting it to this receiver.

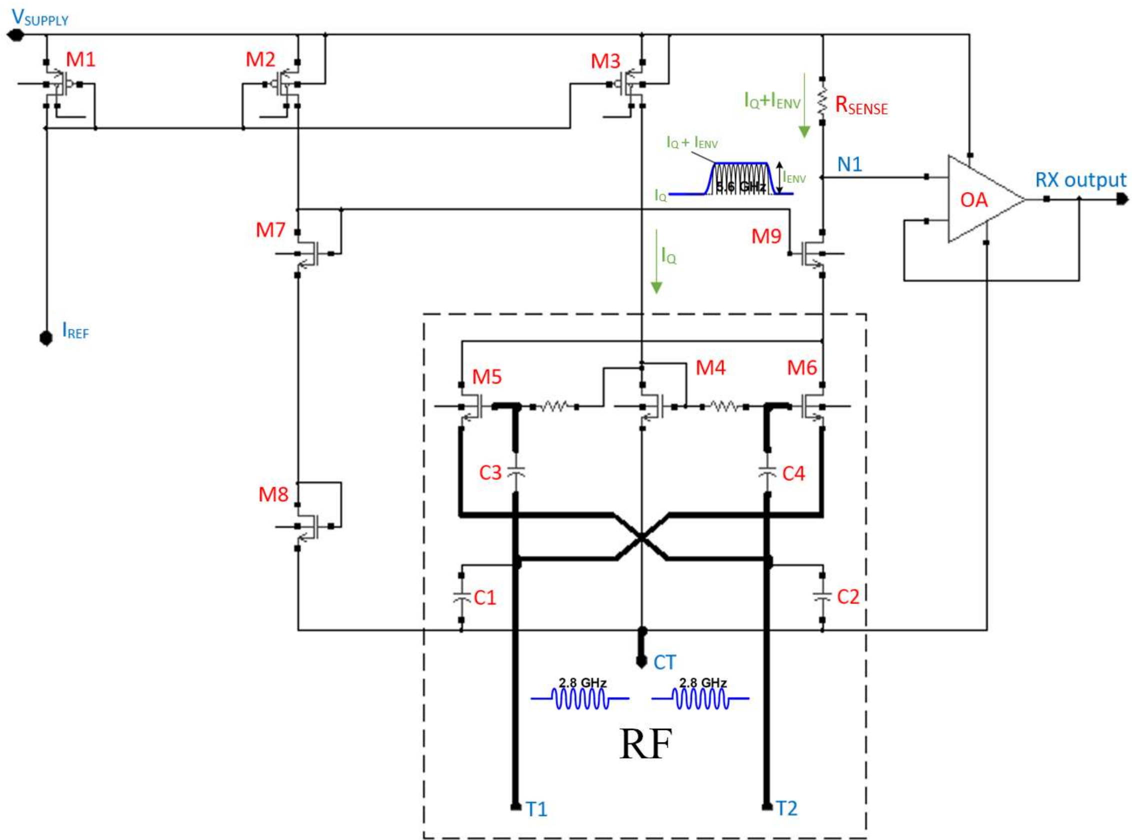

Fig. 4.15. Schematic diagram of receiver outputting analog signal. Voltage drop developed on R_{SENSE} is provided to the output by operational amplifier.

4.5.3 Transmitter Generating Pulse Bursts

Various applications require transmitting of pulses or pulse bursts in response to the input digital signal. In order to generate pulse bursts possessing a defined width, the transmitter generating a continuous signal discussed in Section 4.3 is enhanced by an edge detector which detects the rising and falling edges of the digital control signal and activates the oscillator only during these events. The schematic diagram and the simulation results are depicted in Fig. 4.16. The rising or falling edge of the input digital signal is represented by a different pulse burst width. Similarly to the transmitter introduced in Section 4.3, the imbalanced drive of the oscillator turn-on switches is also inserted in order to accelerate the oscillator activation.

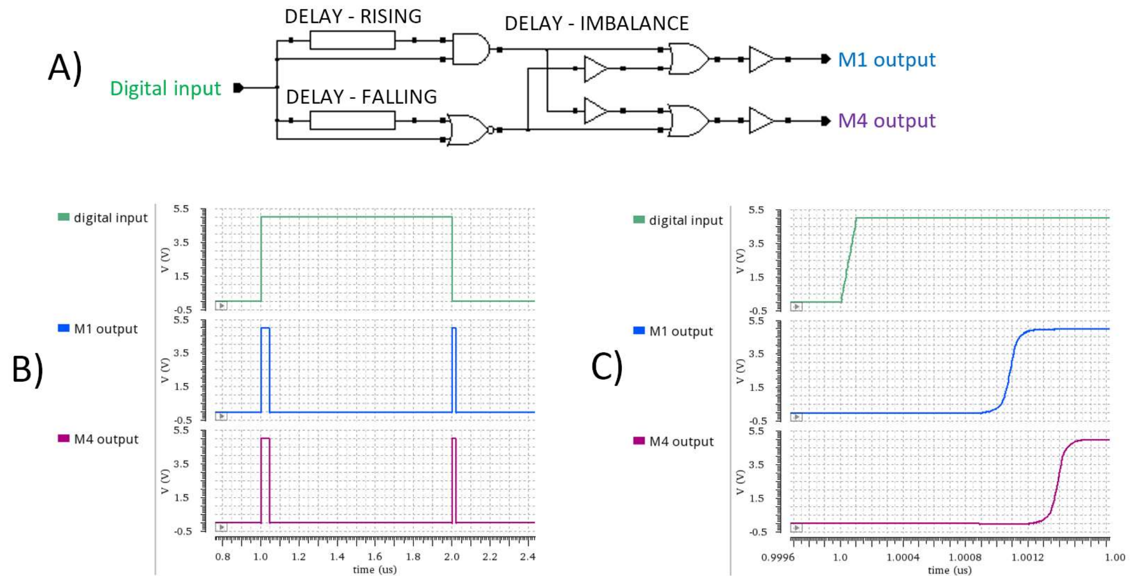

Fig. 4.16. Schematic diagram of edge detector with imbalanced outputs. A) Schematic diagram. B) Simulation results illustrating different rising and falling pulse widths. C) Detail of simulation results illustrating imbalanced drive of oscillator turn-on switches.

4.5.4 Capacitor Value Skews of the Coupled Resonators

As discussed in previous sections, the resonant frequency of the coupled resonators must be tuned precisely to the oscillator frequency in order to attain minimal signal attenuation of the received signal. Although both the fundamental resonator structure depicted in Fig. 4.5 and the transmitter layout illustrated in Fig. 4.9 have been optimized by utilizing an EM simulator, various parasitic elements are typically not considered, and hence the final resonant frequency of either the oscillator or the fundamental resonator may differ.

It has been discovered in former designs of RF test structures that the typical parametric mismatch between the EM simulation and the physical structure does not exceed 5%. That implies that if the oscillator frequency was shifted by 5% and the fundamental resonator frequency was shifted by -5%, the total shift would come to 10%. The probability of such scenario is negligible; nevertheless, four structures with altered resonant frequency of the fundamental resonator have been designed. Since the resonant frequency of the fundamental resonator is given by the loop inductance and the parallel capacitance, the value of the MIM capacitors (Fig. 4.5) is altered to -10%, -5%, +5% and +10%.

4.5.5 Reduced Transmission Line

In order to thoroughly investigate the concept of resonantly coupled lateral structures, a test structure with the high-side fundamental resonator eliminated has been designed. The aim of this experiment is to demonstrate that the fundamental resonator does not attenuate the transmitted signal, but conversely, the resonating element improves the coupling factor, thus reducing the signal attenuation. Since the lump-element model of the complete transmission line has been obtained in Section 4.5.1, only the high side fundamental resonator is removed from the schematic diagram, as illustrated in Fig. 4.17.

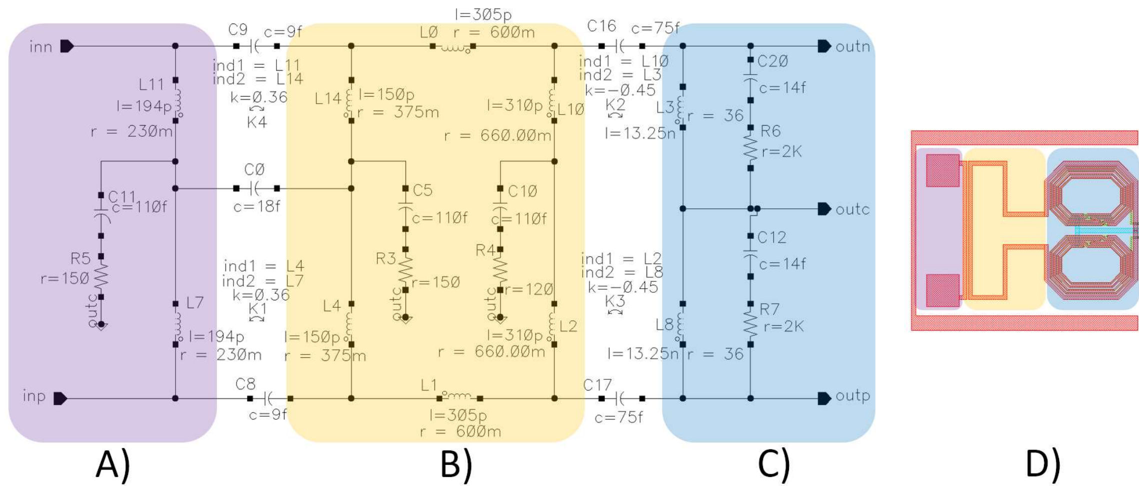

Fig. 4.17. Lump-element model of high side part of reduced transmission line. A) High-side half of bond-wire connection loop. B) Primary side of center-taped transformer. C) Secondary side of center-taped transformer. D) Layout of reduced transmission line.

The simulation outcome comparing the complete and reduced transmission line connected to the receiver outputting the analog signal are depicted in Fig. 4.18. The results illustrate that the presence of the resonating element on the high side part of the transmission line leads to 31% less signal attenuation.

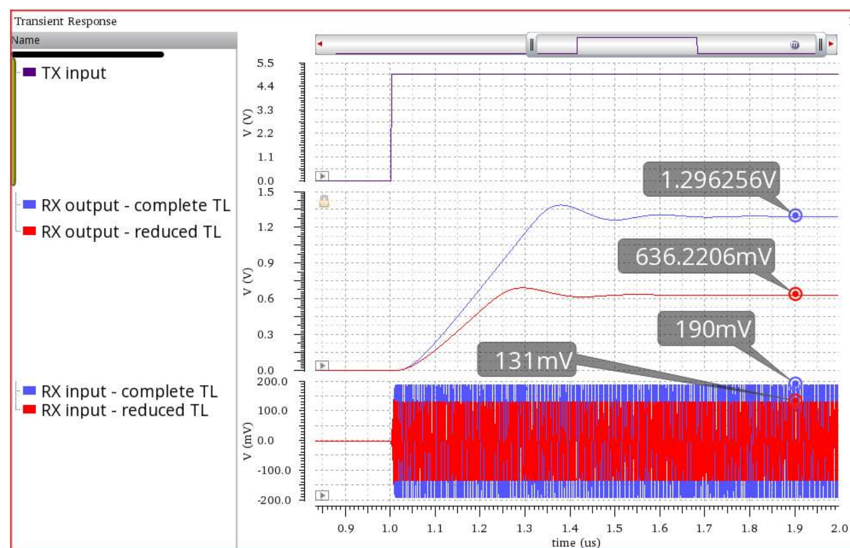

Fig. 4.18. Simulation results comparing complete and reduced transmission line. RX output voltage is measured as differential value between quiescent and active mode.

4.5.6 Evaluation of the Test Structures

The design is realized in the ONC25BCD process introduced in Section 2.2.2. The low side and high side chips are assembled as a multi-chip module in a SOIC-16 Dual Flag package utilizing the standard bond-wire assembly design as demonstrated in Fig. 4.19. Both the low side and high side chips are housed on separated flags of the lead frame as illustrated in Fig. 4.19 A), thereby allowing for HV bias between their reference potentials.

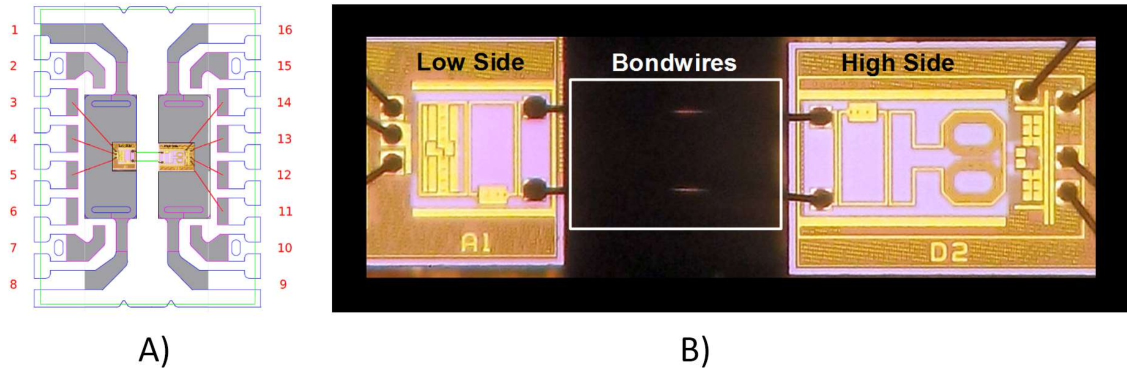

Fig. 4.19. Galvanically isolated translator system module. A) High side and low side chips assembly in SOIC-16 Dual Flag package. B) System micrograph.

The EM simulations and the lump-element model for the entire system was employed to design and predict the transmitter-to-receiver channel's voltage gain and resonance frequency. The combination of the above-listed test structures was further utilized in order to:

- Tune the lump-element model of the transmission line, and
- identify the specific parameter values for achieving the optimal system performance.

The measured average parameters of the physical test structures utilizing the receiver outputting the analog signal are listed in Table 4.2. The signal strength of the complete transmission line, the reduced transmission line and four capacitor skews of the fundamental resonator is expressed as the V_X differential voltage on the output of the receiver. The simulated results of the tuned transmission line lump-element model are also included for comparison. As can be seen from Table 4.2, the simulation and measured results reveal the identical trend.

Table 4.2. Measured parameters of the transmission line test structures at V_{TX} = 5 V.

		Measured			Simulated		
T-Line	V_{TX} [V]	I_{TX} [mA]	f_{OSC} [GHz]	V_X [mV]	I_{TX} [mA]	f_{OSC} [GHz]	V_X [mV]
Complete	5.0	346	2.86	1133	366	2.76	1296
Reduced	5.0	364	2.84	749	366	2.76	636
Complete_C-10 %	5.0	339	2.81	643	338	2.78	666
Complete _C-5 %	5.0	356	2.81	1193	350	2.76	1021
Complete _C+5 %	5.0	361	2.88	633	369	2.95	544
Complete _C+10 %	5.0	337	2.90	310	357	2.98	297

The high variation of the I_{TX} transmitter current consumption among the test structures is influenced by the structure-to-structure process variation and the self-heating mechanism. In order to significantly suppress the self-heating, the duty cycle of the transmitter activating signal was reduced to 1% during the measurement. The I_{TX} values in Table 4.2 have been recalculated to a 100% duty cycle, thus indicating the steady-state current consumption of the transmitter in the active mode.

Since the transmitter oscillator is not current limited, the I_{TX} current consumption depends on the supply voltage to a large extent. The measurement results with the V_{TX} supply voltage reduced to 4 V are listed in Table 4.3.

Table 4.3. Measured parameters of the transmission line test structures at V_{TX} = 4 V.

		Measured			Simulated		
T-Line	V_{TX} [V]	I_{TX} [mA]	f_{OSC} [GHz]	V_X [mV]	I_{TX} [mA]	f_{OSC} [GHz]	V_X [mV]
Complete	4.0	234	2.91	368	250	2.84	736
Reduced	4.0	244	2.90	288	250	2.84	417
Complete_C-10 %	4.0	232	2.85	417	232	2.80	492
Complete _C-5 %	4.0	240	2.86	640	240	2.79	731
Complete _C+5 %	4.0	242	2.93	191	243	3.01	216
Complete _C+10 %	4.0	228	2.94	95	239	3.02	130

Table 4.3 indicates that the current consumption of the transmitter is reduced by approximately 30 % at 4 V supply. The simulation has shown that the oscillator amplitude is also reduced, leading to the signal amplitude on the receiver input decreased by approximately 30 % as well, confirming that the intensity of the received signal remains well within the range detectable by the receiver. The comparison of the measured and simulated differential voltage on the receiver output is depicted in Fig. 4.20, which plots the V_X differential voltage waveforms over the variation of the fundamental resonator capacitor. The fundamental resonator is designed so that the resonant frequency reaches 2.75 GHz. As illustrated in Table 4.2 and Table 4.3, at 5 V supply, the oscillator frequency is shifted by approximately 3.5 %, which conveniently corresponds with the V_{TX} peak position in Fig. 4.20 A). At 4 V supply, the oscillator frequency is shifted by 6 %, which also corresponds with the V_{TX} peak position in Fig. 4.20 B).

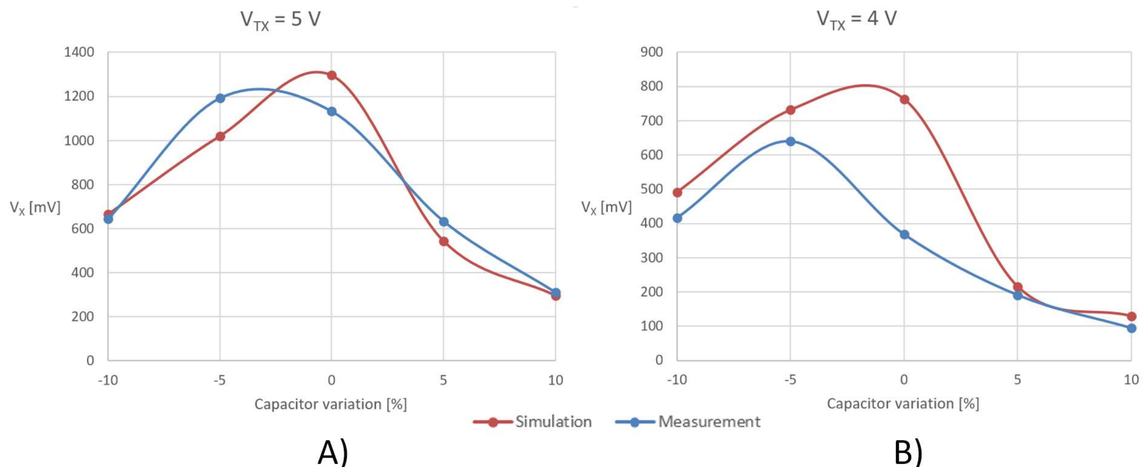

Fig. 4.20. Measured and simulated differential voltage on receiver output. A) Transmitter supply voltage 5 V. B) Transmitter supply voltage 4 V.

4.6 Communication through the Isolator

The communication through the transmission line introduced in Chapter 4 may be established by utilizing an RF signal detector only. Therefore two possible modulation schemes are considered for employment:

- ON-OFF Keying (OOK) digital modulation, or
- Pulse Width Modulation (PWM).

Both modulation schemes have been evaluated on physical test structures. The results achieved are discussed in the following sections.

4.6.1 ON-OFF Keying Digital Modulation

The principle underlying the OOK digital modulation is that the digital data is represented as either the presence or absence of a carrier signal. It does not matter whether the presence of the transmitted signal is assigned to the logic high state and the absence of the signal is assigned to the logic low state or vice versa. Depending on a concrete application, one of the assignment is usually more beneficial, particularly in the aspect of the system current consumption.

The merits of the OOK coding comprise high data rate as well as high robustness against an error. The major handicap is represented by the high current consumption due to continuous transmission of the carrier signal. The current consumption is therefore given by the duty cycle of the input digital signal only; it is not dependent on the input signal frequency.

The physical structures introduced in Section 4.5 have been characterized and the measured waveforms are depicted in Fig. 4.21. The output signal is inverted.

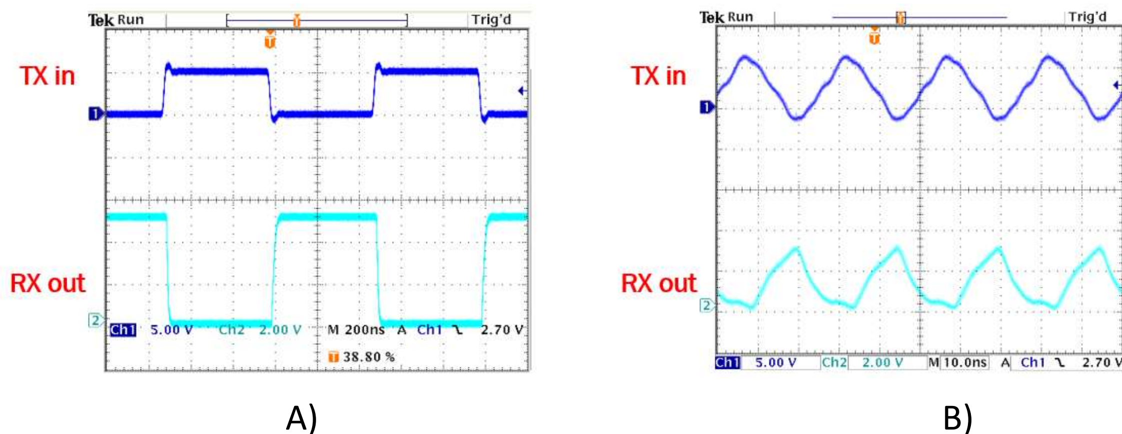

Fig. 4.21. Measured results of communication through the isolator using OOK modulation: A) 2 Mbps (1 MHz). B) 80 Mbps (40 MHz).

4.6.2 Pulse Width Modulation

In order to significantly reduce the current consumption of the translator, the PWM has also been evaluated. The principle of the PWM lies in the digital data being represented as a distinct width of a pulse, or pulse bursts, of a carrier signal. Similarly to the OOK modulation, it is of no substantiality whether the logic high is assigned to the wider pulse while the logic low is assigned to the narrower pulse, or vice versa.

In the half bridge driver application, it must be ensured that in the event of an erroneous reception, no serious damage of the application arises. Owing to that, it is beneficial to assign the narrow pulse to the logic low state (representing the deactivation of the driver) and the wider pulse to the logic high state (activation of the driver).

The current consumption of the transmitter is reduced, since the transmitter is activated only when the digital input signal alters its logic state. But the penalty of the lesser current consumption is that the transmitted data rate is limited, since two pulses are generated, one for each input signal transition. The width of the transmitted pulse must be decoded exactly, and hence the robustness against an error is also impacted. The test structures employing the transmitter discussed in 4.5.3 have been characterized and the measured waveforms are depicted in Fig. 4.22.

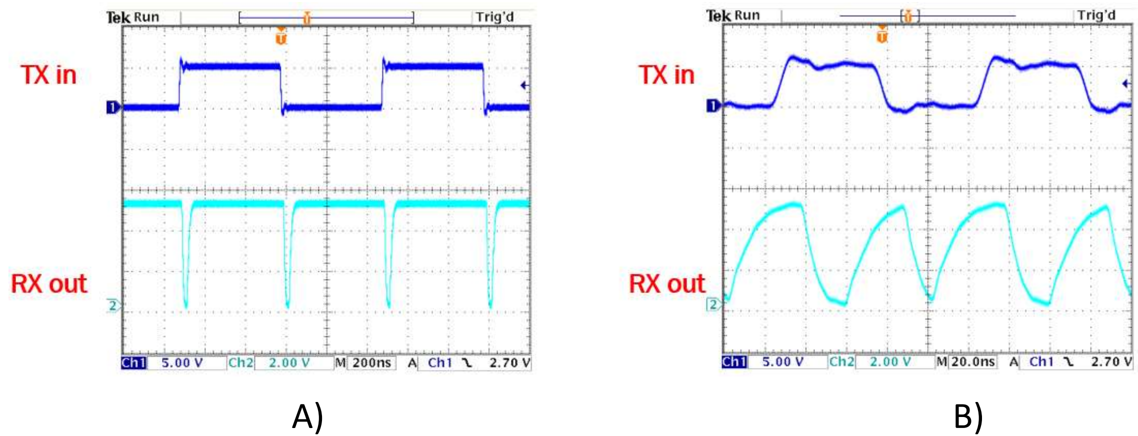

Fig. 4.22. Measured results of communication through the isolator using PWM coding: A) 2 Mbps (1 MHz). B) 20 Mbps (10 MHz).

The measured waveforms are distorted by the input capacitance of the oscilloscope probe. The waveform depicted in Fig. 4.23 shows that the physical measurement is in great conformity with the simulation if the identical load capacitance on the receiver output is incorporated.

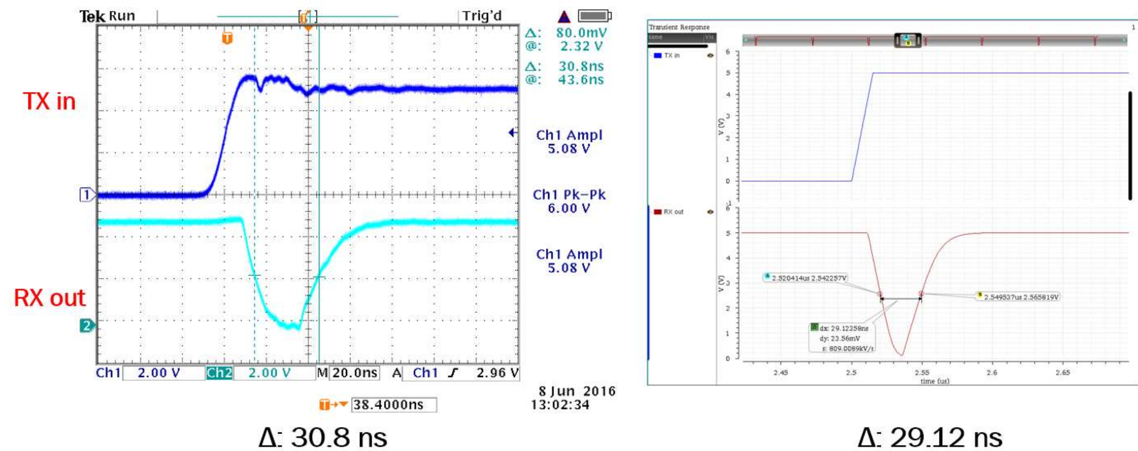

Fig. 4.23. Measured and simulated waveforms on receiver output. Test structure of the galvanically isolated translator utilizes transmitter generating pulse bursts.

The results of the signal pulse width and the propagation delay from the transmitter digital control input to the receiver output are listed in Table 4.4. The comparison of the measures between OOK and PWM schemes are shown in Table 4.5.

Table 4.4. Signal pulse width and propagation delay.

	Propagation delay [ns]		Pulse width [ns]	
	Low to High	High to Low	Low to High	High to Low
Measured	13.6	17.6	30.8	27.6
Simulated	12.7	17.6	29.1	24.6

Table 4.5. Comparison between OOK and PWM measures at 1 MHz input signal frequency.

Parameter	**OOK**	**PWM**
Power consumption I_{TX}	117 mA @ V_{TX} = 4 V	4.7 mA @ V_{TX} = 4 V
Power consumption I_{RX}	160 µA @ V_{RX} = 5 V	160 µA @ V_{RX} = 5 V
Data rates	High	Intermediate
Error robustness	High	Intermediate

4.7 Results and Discussion

The concept of the lateral resonant coupling introduced in this chapter has been prototyped and investigated using the test structures. This technique has been proved as a viable solution to increase the maximum achievable isolation rating in fully-integrated CMOS galvanic isolation designs. The proposed method utilizes the lateral on-chip spacing between resonant structures to provide galvanic isolation. The high sensitivity and low power receiver has been designed in order to guarantee reliable communication over process variation. The key parameters of the galvanically isolated translator are listed below:

- ONC25BCD, 4 metal process option.
- No high voltage process extension.
- Silicon area of the translator: 0.94 mm^2.
- Attained RMS isolation: 3.3 kV.

The lump-element model of the transmission line has been obtained in order to enable the simulation of complex systems integrated in this concept of the galvanically isolated translator.

5 DESIGN OF 800 V GALVANICALLY ISOLATED HALF BRIDGE DRIVER FOR INDUSTRIAL APPLICATIONS

Among industrial applications, safety requirements are not the driving reasons for which the galvanic isolation is required. The galvanically isolated translator introduced in Chapter 4 which has been developed in the first phase of the development replaces the standard junction-isolated high voltage level shifter in order to provide:

- Advanced noise immunity, specifically against high dV/dt transitions,
- negative transient immunity, and
- higher operating voltage.

Because the monolithic half bridge driver is junction-isolated, the high voltage floating region along with the high voltage level shifters are coupled to the substrate through parasitic capacitance. High dV/dt transients generate capacitive currents which may interfere with other signals in the application system and cause a system failure. In the case of galvanic isolation, these stray currents are at least one order of magnitude lower, thereby minimizing such potential problems.

The negative transient immunity (NTI) of monolithic half bridge drivers is naturally limited by the fact that the high voltage floating region is isolated by reversely polarized P-N junction only. Essentially, attainable negative voltage is therefore limited by the supply voltage of the high voltage floating region. Because the galvanic translator provides the same level of isolation in both polarities, the NTI is enhanced up to the intrinsic breakdown voltage of the galvanic translator.

The breakdown voltage of the high voltage P-N junction represents yet another limiting factor. Although high voltage technologies capable of 1200 V exist, typically utilized monolithic half bridge drivers do not exceed 800 V. As discussed in Chapter 4, the breakdown voltage of the galvanically isolated translator is determined by the number of coupled resonators.

Fig. 5.1 depicts the segmentation of the half bridge driver for industrial applications in the package. All the low voltage signals are processed by the low voltage die. The high voltage die is responsible for driving the high side external MOSFET only.

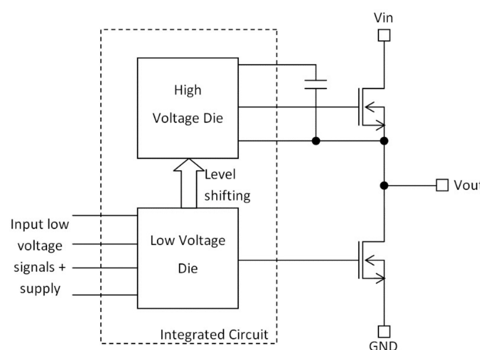

Fig. 5.1. Proposed multi-die concept of half bridge driver for industrial applications.

Both high and low voltage dice have been fabricated in ONC25BCD technology. The design introduced in Chapter 4 has been employed as the galvanically isolated translator. Although the basic flow of the ONC25BCD process technology offers five metal layers, only four metal layers have been utilized in this design. It has been proven on the test structures that employing four metal layers guaranties 3.3 kV RMS isolation. Such value is sufficiently high for 800 V reliable operation. The device also complies with the HBM ESD JEDEC standard [12], since the 3.3 kV RMS offers higher breakdown value than required by the HBM ESD standards.

5.1 Communication through the Isolator

Since the proposed half bridge gate driver utilizes the galvanically isolated translator introduced in Chapter 4, an employment of the OOK or PWM may be taken into consideration. Due to the current consumption constrains, the PWM has been chosen as the sensible candidate for this design. The input control signal is modulated by the edge detector, discussed in Section 4.5.3, in order to provide 40 ns and 20 ns pulses representing the leading and the falling edge of the input signal respectively. The pulse bursts are transmitted to the high voltage die, where they are demodulated to obtain the high side driver control signal.

5.2 Low Voltage Die

The low voltage die houses several circuits responsible for the low side driver operation and the transmission of the high side driver control signal. The layout overview of the low voltage die is illustrated in Fig. 5.2. The die size amounts to 1.3 × 1.2 mm.

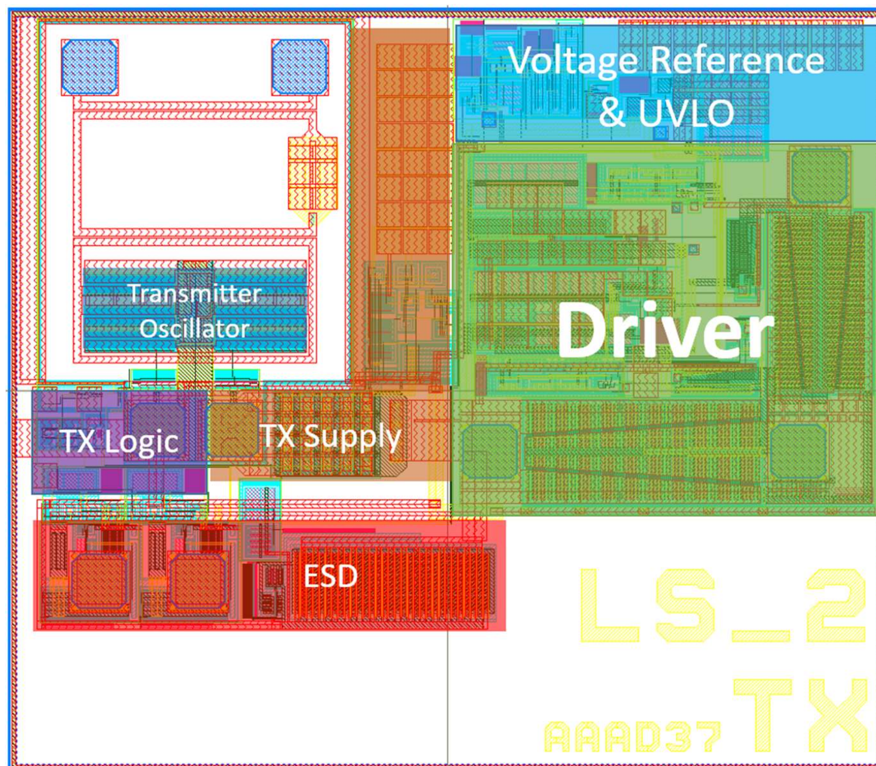

Fig. 5.2. Layout of low voltage die of half bridge driver for industrial applications.

5.2.1 Transmitter with Oscillator

The transmitter discussed in Section 4.3 has been utilized in order to drive the transmission line. As discussed in Section 4.5.6, its reliable operation is provided if the supply voltage is higher than 4 V. Nevertheless, at 5 V supply, the current consumption of the transmitter increases significantly. Therefore, the 4.5 V value has been chosen as the compromise ensuring sensible voltage margin for stable operation.

5.2.2 Transmitter Power Supply

During pulse transmission, the transmitter current consumption increases from substantially zero current to its maximum value. The transmitter power supply must be capable to deliver approximately 300 mA current in an extremely short time. Such requirement practically disqualifies any design of a voltage regulator employing a feed-back loop system. The simplified schematic diagram of the transmitter power supply and the simulated voltage and current waveforms are depicted in Fig. 5.3 A), B).

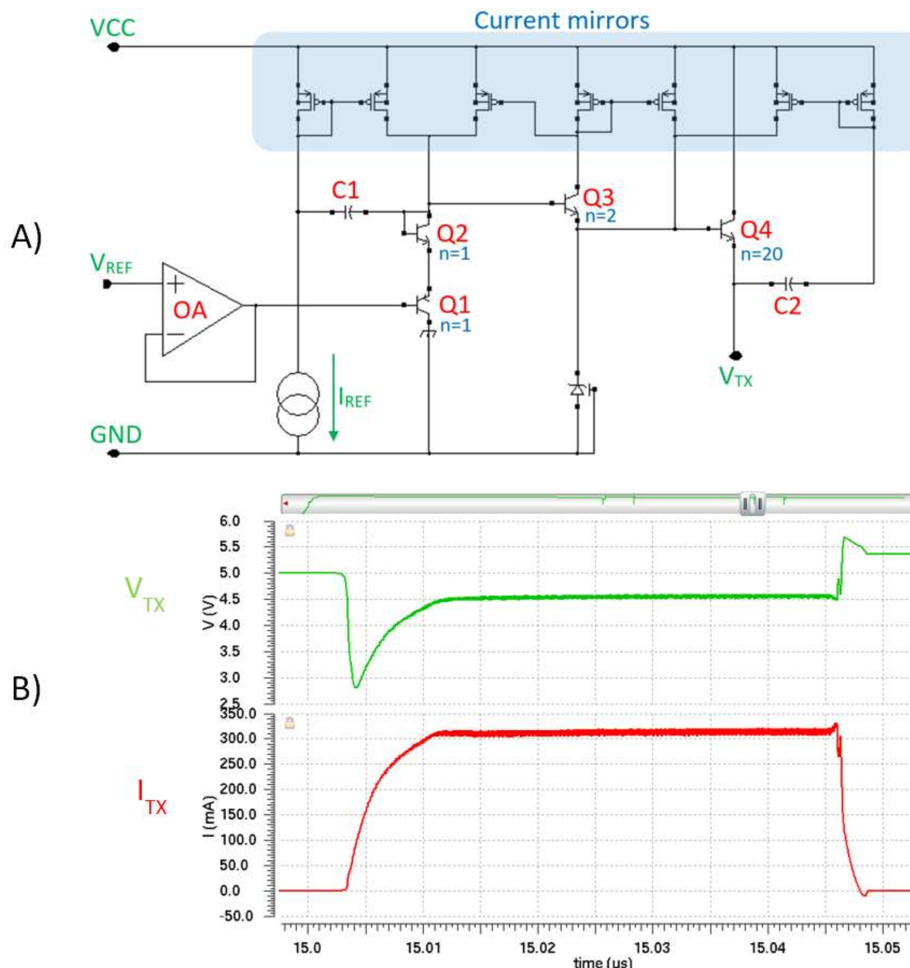

Fig. 5.3. Transmitter power supply: A) Simplified schematic diagram B) Simulated output voltage and current waveforms during transmission.

The transmitter supply voltage (V_{TX}) is generated by the voltage follower formed by the Q1, Q2, Q3 and Q4 transistors. The operational amplifier (OA) transforms the high-impedance V_{REF} voltage to a low-impedance voltage source for the Q1 base of the value

equal to V_{REF}. Owing to that, the V_{TX} voltage disturbance does not interfere with the V_{REF} voltage reference. The current mirrors are connected so as to multiply the current gain of the Q1, Q2, Q3 and Q4 transistors under high current conditions. The C1 and C2 capacitors serve as dynamic feed-forward loops that compensate the V_{TX} undershoot at the transmitter activation. An extra bond pad has been inserted in order to enable potential bypassing of the V_{TX} voltage by an external blocking capacitor. The transmitter power is supplied from an external voltage source (VCC). The VCC acceptable range is 8 to 20 V.

5.2.3 Transmitter Logic

The transmitter logic translates the input control signal into pulses which are transmitted to the high side die. In order to enhance noise immunity and to normalize the input control signal to the internal 5 V supply domain, the input signal is initially processed by the Schmitt Trigger. The normalized control signal is then connected to the edge detector discussed in Section 4.5.3 which controls the transmitter.

5.2.4 Voltage Reference and Under-Voltage Lock-Out (UVLO)

The low voltage die features the under-voltage lock-out (UVLO) function to disable the output gate driver during low supply voltage conditions. Below the minimum supply voltage, the function and performance of the gate driver is undefined, making the system behavior unpredictable. The UVLO circuit typically includes some hysteresis in order to prevent cyclic turn on and off of the device due to supply voltage instability.

In this particular design, the UVLO implementation takes on the form of the VCC supply voltage being divided by a voltage divider and compared to the internal voltage reference. The hysteresis is realized by shorting of several resistor segments in the voltage divider.

The ONC25BCD process offers 5.5 V undersurface zener diode which may serve as a voltage reference. Since the UVLO thresholds exceed 5.5 V and also no additional demand to possess precise voltage reference exists, the reference voltage is generated by the zener diode. The 5 V internal supply domain is formed by the M1 source follower depicted in Fig. 5.4. The 0.8 V threshold voltage of the M1 MOSFET is subtracted from the sum of the voltages on the DZ1 zener and DS1 schottky diodes.

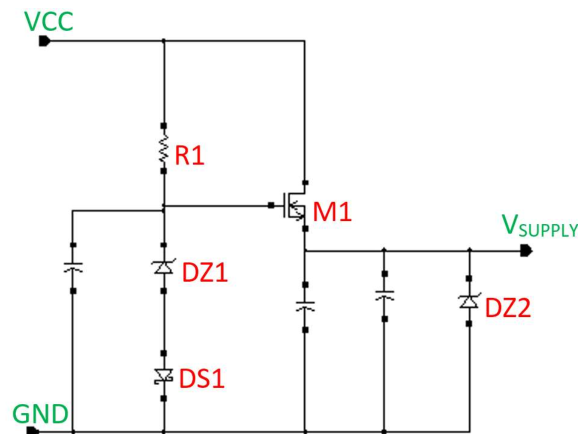

Fig. 5.4. Internal supply domain generator.

5.2.5 ESD Protection

In order to protect the low voltage die against the Electro-Static Discharge (ESD), the ESD protection has been implemented. In this design, the central clamp architecture is utilized (Fig. 5.5). All the I/O (Input/Output) pins are connected to the central ESD clamp (Z1) through high voltage ESD diodes (D1 through D4), so the ESD current is shunted as illustrated in Fig. 5.5.

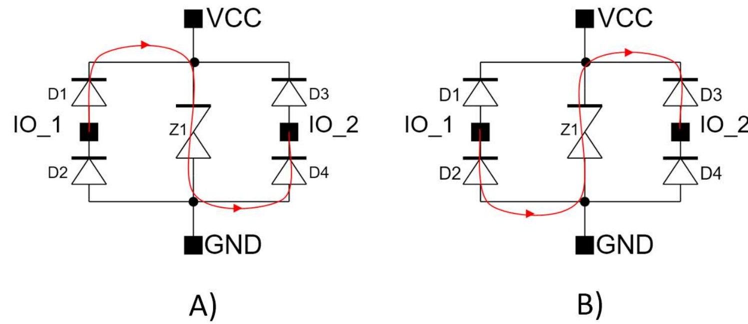

Fig. 5.5. The central clamp architecture of ESD protection: A) Positive ESD pulse on IO_1 versus IO_2 grounded. B) Negative ESD pulse on IO_1 versus IO_2 grounded.

5.2.6 Output Driver

The output driver is responsible for driving an external MOSFET. As discussed in Section 2.1.5, the output gate driver must meet several requirements. One of these demands is the source and sink current capability. In this design, the output driver possess 2 A source and sink capability, which is an ample value for target half bridge applications.

The standard push-pull topology has been utilized in the output driver as illustrated in Fig. 5.6. The output source and sink transistors are represented by M1 and M2, respectively. Since the gate oxide withstands 5 V bias only, the buffers driving the M1 transistor require the FGND floating ground provided by the floating 5 V power supply. The input signal is also level-shifted from the GND reference to the FGND reference.

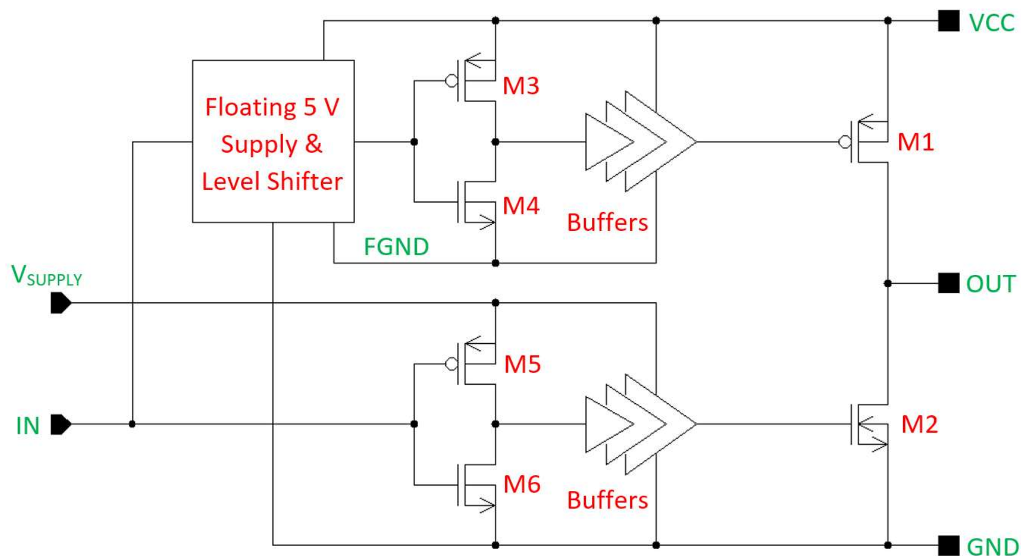

Fig. 5.6. Schematic diagram of output gate driver.

The simulation results illustrating the gate voltages of the M1 and M2 transistors at VCC = 15 V are depicted in Fig. 5.7. As can be seen, the voltage on the output of the driver swings between the ground and VCC potentials. The gate voltage of the M1 PMOS transistor swings between VCC and VCC – 5 V potentials.

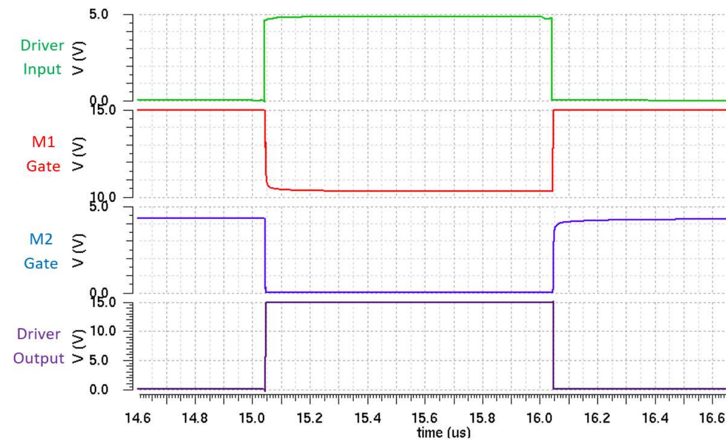

Fig. 5.7. Simulation results of output driver. The M1 gate voltage swings between VCC and VCC – 5 V potentials.

5.3 High Voltage Die

The high voltage die houses circuits responsible for the high side driver operation and the reception of the high side driver control signal. The layout overview of the high voltage die is shown in Fig. 5.8.

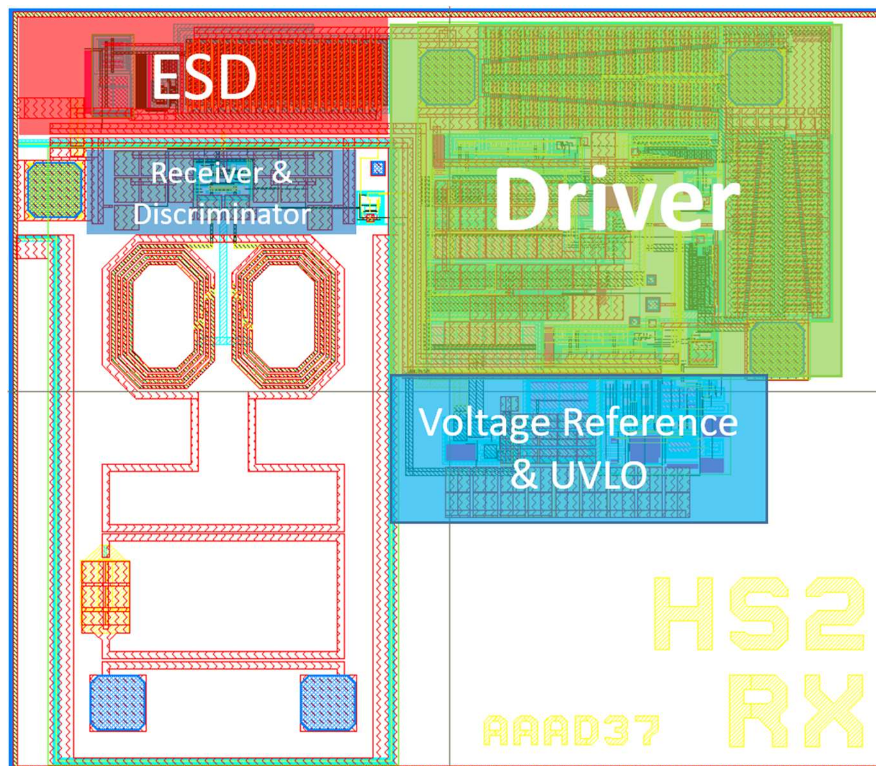

Fig. 5.8. Layout of high voltage die of 800 V half bridge driver for industrial applications.

Since the high side gate driver must possess the same electrical characteristics as the low side gate driver, several circuits designed for the low voltage die are also utilized on the high voltage die. The identical circuits are listed below:

- Voltage Reference and Under-voltage Lock-out (UVLO),
- output driver, and
- ESD protection.

5.3.1 Receiver with Discriminator

The received signal on the high side part of the transmission line is processed by the receiver discussed in Section 4.4. The width of the pulses on the receiver output is practically identical to those generated by the transmitter logic, as illustrated in Fig. 5.9. The output of the receiver is connected to the discriminator which demodulates the pulses, thereby generating the gate driver control signal.

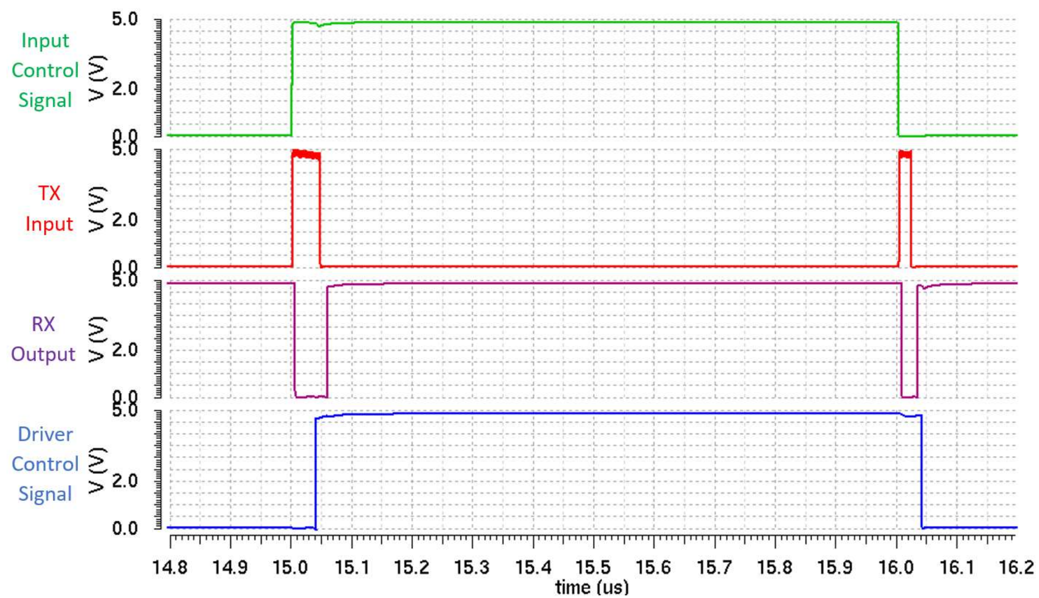

Fig. 5.9. Simulation results of control signal propagation from low voltage die input to high voltage die gate driver input.

The schematic diagram of the discriminator is depicted in Fig. 5.10 A). The D input of the D flip-flop is connected to the input signal. The inverted falling edge of the input signal (IN) is delayed and connected to the clock input (CK) of the D flip-flop. Owing to that, the logic state is determined by the delay time – the longer and shorter pulses are translated as the logic high and logic low state, respectively, as illustrated in Fig. 5.10 B), C).

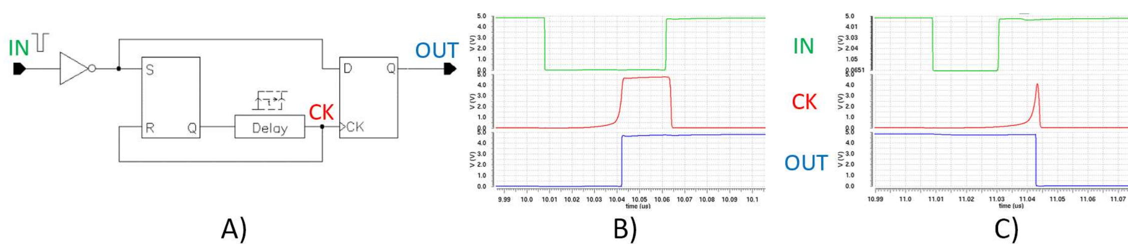

Fig. 5.10. Discriminator: A) Schematic diagram. B) Detail of set pulse. C) Detail of reset pulse.

5.4 Evaluation of the Half Bridge Driver

The design of the 800V galvanically isolated half bridge driver for industrial applications has been prototyped and encapsulated in a fashion similar to the galvanically isolated translator discussed in Chapter 4. The SOIC-16 Dual Flag package utilizing the standard bond-wire assembly approach has been utilized to assembly low voltage and high voltage dice as a multi-chip module, as illustrated in Fig. 5.11. Both the low voltage and high voltage dice are housed on separated flags of the lead frame, as illustrated in Fig. 5.11 B), thereby allowing for HV bias between their reference potentials.

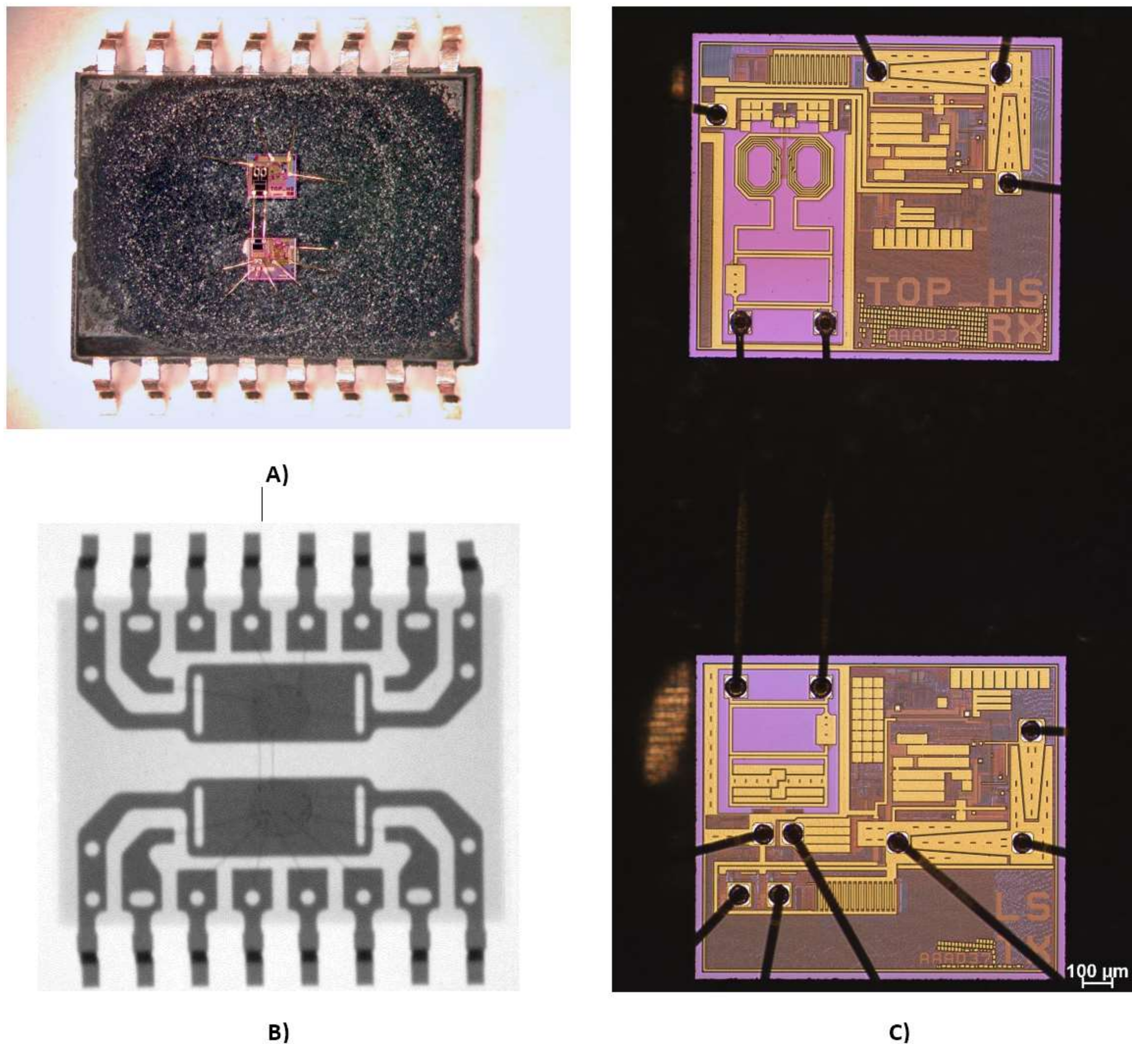

Fig. 5.11. Half bridge driver for industrial applications. A) Locally de-capsulated IC. B) X-ray photo of the IC depicting two galvanically isolated flags of the lead frame. C) Zoom-in on low voltage and high voltage dice (lower and upper respectively).

Several tests have been performed in order to obtain the fundamental parameters of the half bridge driver:

- The input to output propagation delay and delay matching,
- the gate driver current source and current sink capability, and
- the common mode transient immunity.

Finally, the half bridge driver has been tested in the real LLC application.

5.4.1 Input to Output Propagation Delay

The input-to-output propagation delay of both the high side and low side gate drivers has been evaluated by employing the test configurations illustrated in Fig. 5.12. The high side ground is DC biased to +/-1600 V in the test configuration depicted in Fig. 5.12 B).

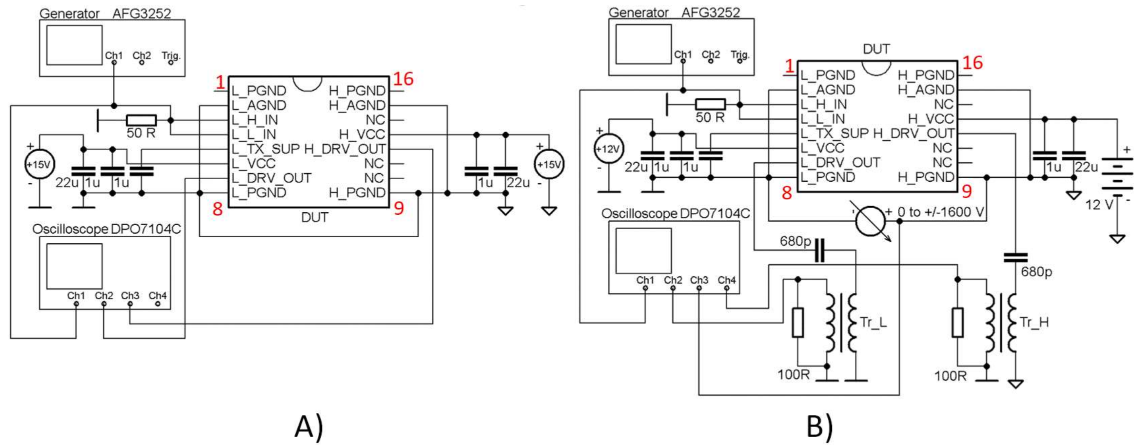

Fig. 5.12. Schematic diagram of test configuration for propagation delay measurement. A) Both low side and high side drivers grounded. B) High side driver ground biased to +/-1600 V. Pulse transformers (Tr_L and Tr_H) are utilized to transfer output driver edges to oscilloscope.

In order to evaluate the designed half bridge driver under dynamic conditions, the test configuration has been further modified as depicted in Fig. 5.13 A). The high side ground oscillation is controlled by the NCP1399 application board [59]. The continuous measurement results are demonstrated in Fig. 5.13 B). The fluctuation of the high side propagation delay does not exceed 0.5 ns, and is most likely induced by the noise generated by the applied dynamic signal. The oscilloscope is synchronized to the low side driver output signal, thus the depicted fluctuation of the high side propagation delay is effectively the sum of the high side and low side propagation delay variations.

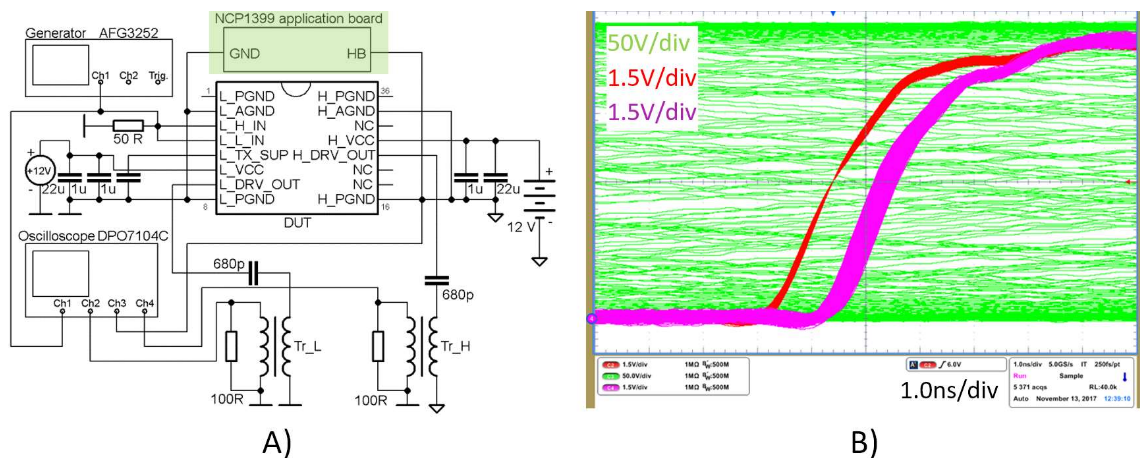

Fig. 5.13. Test configuration for the dynamic measurement. A) Schematic diagram. High side ground is dynamically biased by NCP1399 application board. B) Continuous measurement illustrating propagation delay variation. Red – low side driver output, violet – high side driver output, green – high side ground.

The results of the propagation delay measurement are listed in Table 5.1 and demonstrate that the propagation delay of the high side driver is not dependent on the high-side ground bias.

Table 5.1. Results of propagation delay measurement.

	Grounds shorted		High Side ground biased	
	Rising edge [ns]	Falling edge [ns]	Rising edge [ns]	Falling edge [ns]
Low Side	54.1	50.4	54.1	50.4
High Side	55	51.7	55	51.7
Matching (HS - LS)	0.9	1.3	0.9	1.3

5.4.2 Gate Driver Current Capability

The measured values of the gate driver current sink and current source driving capability are listed in Table 5.2. The rise time and fall time values are measured on the 1 nF load capacitor.

Table 5.2. High side and low side gate driver current capability.

	Rise time [ns]	Fall time [ns]	Source [A]	Sink [A]
Low Side	5.9	5.5	2.9	2.6
High Side	5.9	5.4	2.6	2.7

5.4.3 Common Mode Transient Immunity

The CMTI of the high side driver has been evaluated in the test configuration depicted in Fig. 5.14 A). The NCP1392 controller [60] has been utilized as a floating pulse generator to provide driver control signals. In order to minimize potential parasitic capacitance of a power supply, 12 V batteries have been employed as the power sources. An example of the waveform in Fig. 5.14 B) illustrates the 160 V/ns slope of the CMTI test signal applied between the low side and high side grounds. The probe of the oscilloscope is referred to the high side ground.

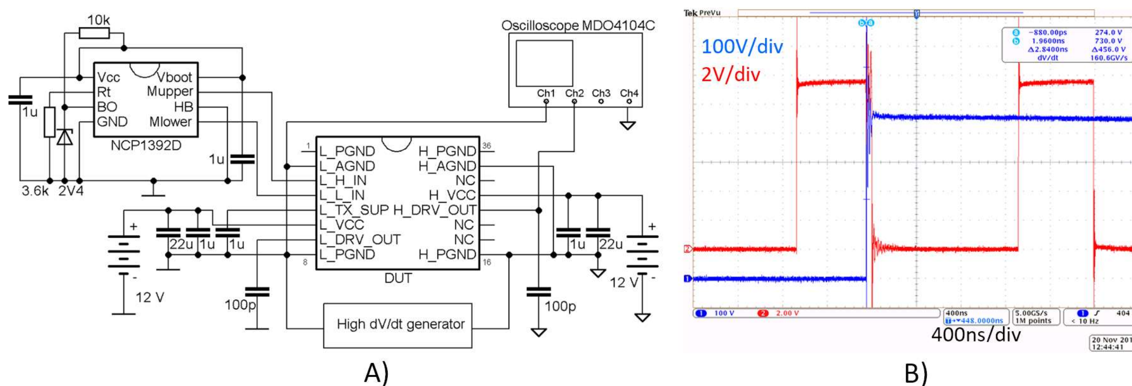

Fig. 5.14. CMTI measurement. A) Schematic diagram of CMTI test configuration. B) CMTI test waveform demonstrating 160 V/ns slope applied between high side and low side ground terminals (blue).

Two sets of the CMTI test signals have been applied by the 600 V high-dV/dt generator in order to evaluate the CMTI:

- 160 V/ns,
- 650 V/ns.

Examples of the 650 V/ns CMTI test waveforms are depicted in Fig. 5.15.

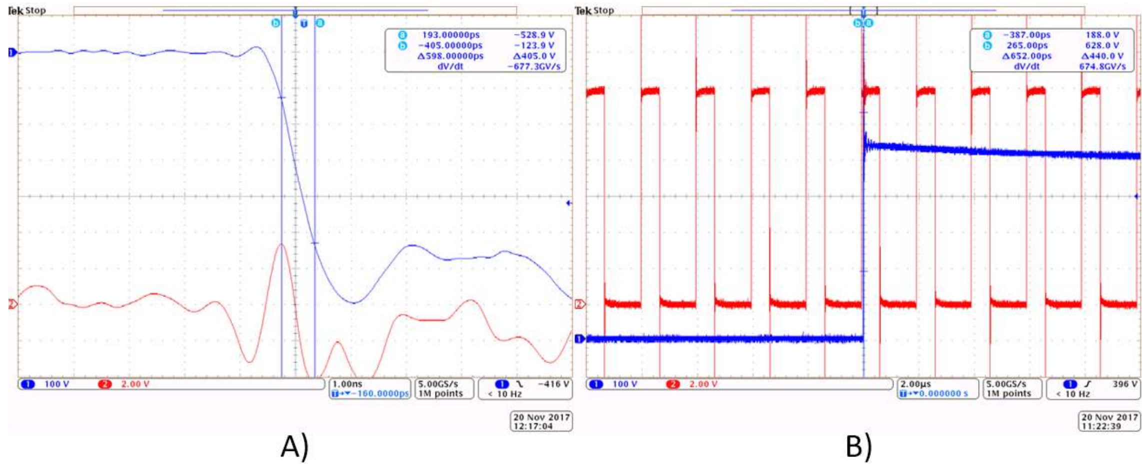

Fig. 5.15. CMTI test waveforms. A) Detail of the high-dV/dt signal demonstrating blue waveform possessing 677 V/ns slope. B) Example of CMTI test signal (blue) interfering with driver output.

The CMTI measurement has proved that the designed galvanically isolated half bridge driver is immune to the common mode transients sloping up to 650 V/ns.

5.4.4 LLC Resonant Converter Application

In this test, the designed half bridge driver has been employed in the LLC resonant converter discussed in Section 2.1.4. The NCP1395 controller [61] has been utilized, since it requires an external half bridge gate driver. The LLC application has been tested under full-range load conditions. As illustrated in Fig. 5.16, no gate driver malfunction has been observed.

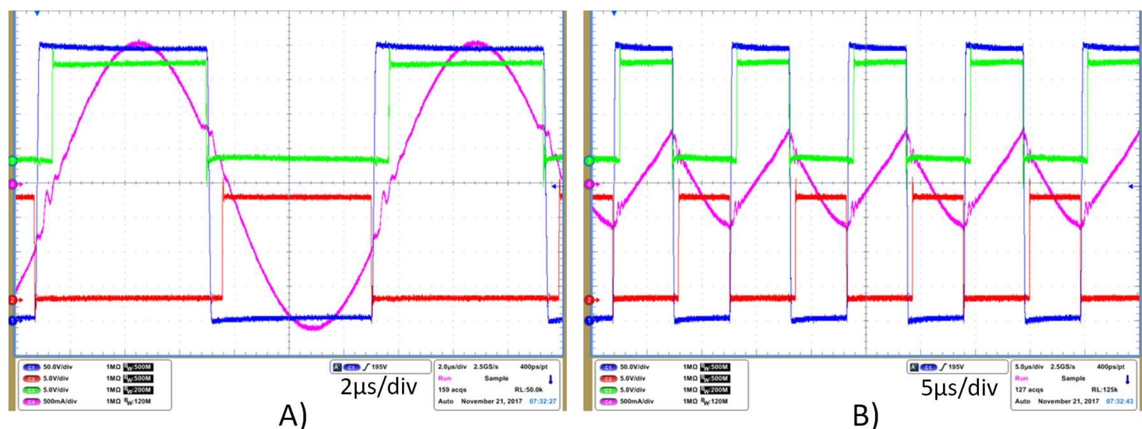

Fig. 5.16. Measured waveforms of LLC application. Blue – bridge node voltage, green – high side MOSFET gate voltage, red – low side MOSFET gate voltage, violet – primary side current. A) Full load. B) Light load.

5.4.5 Current Consumption

The measured current consumption is listed in Table 5.3. Three sets of the load capacitors have been evaluated. The measurement results indicate that the maximum operating frequency of the half bridge driver amounts to 500 kHz, since the current consumption increases rapidly at 1 MHz.

Table 5.3. Measured current consumption of the low side (I_{LS}) and high side (I_{HS}) driver.

Frequency	C_{LOAD} = 0		C_{LOAD} = 100 pF		C_{LOAD} = 1 nF	
	I_{LS} [mA]	I_{HS} [mA]	I_{LS} [mA]	I_{HS} [mA]	I_{LS} [mA]	I_{HS} [mA]
No switching	0.18	0.13	0.18	0.13	0.18	0.13
100 kHz	2.75	0.30	3.00	0.54	4.26	1.58
500 kHz	12.8	0.88	13.9	2.09	20.2	7.20
1 MHz	25.1	1.59	27.3	3.83	39.9	14.2

5.5 Results and Discussion

The galvanically isolated half bridge driver for industrial applications has proved itself a viable target application for galvanically isolated translators utilizing lateral resonant coupling. The presented design of the half bridge driver amply satisfies the listed industrial application requirements:

- High breakdown voltage,
- high negative transient immunity, and
- high CMTI.

The half bridge driver has been tested in LLC resonant converter application under both normal operation and heavy overload conditions. No gate driver malfunction has been observed. The measured high side and low side propagation delay equals 50 ns with perfect matching between the drivers. The propagation delay is not sensitive to the high voltage bias, either under static or dynamic conditions. The current consumption measurement revealed that the maximum operating frequency of the presented half bridge driver design is 500 kHz. Such value is adequate for target applications utilizing MOSFET devices. The driver current capability is also equivalent for the target applications.

6 DESIGN OF GALVANICALLY ISOLATED TRANSLATOR FOR HV APPLICATIONS

In the second phase of the development, a different coupling device has been utilized in order to attain a higher value of the isolation voltage. The target isolation voltage is at least 4 kVrms, applied and measured on the galvanic isolator over the time interval of one minute, as required by the international standards [62], [63]. Similarly to the design discussed in Chapter 4, the multi-die system is utilized as illustrated in Fig. 6.1.

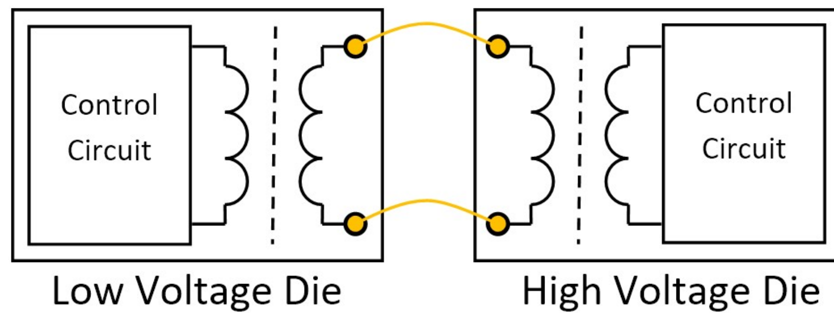

Fig. 6.1. Block diagram of multi-die system of galvanically isolated translator for HV applications.

6.1 Fabrication Process

The galvanically isolated translator for HV applications utilizes the ONC25BCD technology discussed in Section 2.2.2 which is extended by an additional 6th metal layer. The high isolation voltage is increased by the thick oxide formed between the 5th and the 6th metal layers as demonstrated in Fig. 6.2.

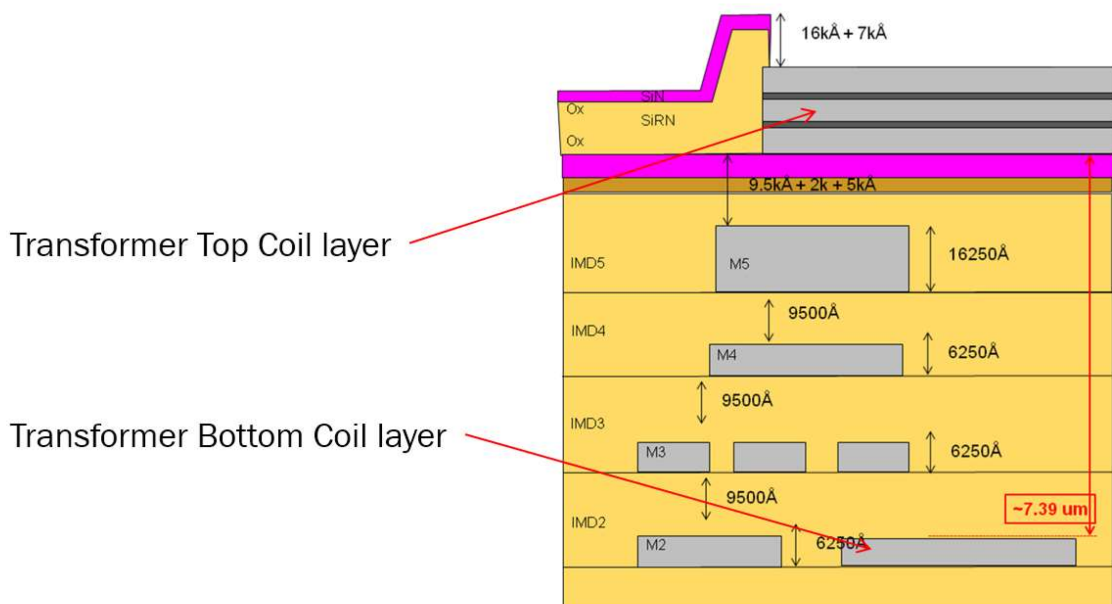

Fig. 6.2. Cross section of the 6th metal layer ONC25BCD fabrication process. M3, M4 and M5 layers are excluded from the transformer design in order to increase galvanic isolation.

In order to maximize the isolation barrier, the 3rd and 4th metal layers are not employed in the transformer design. Consequently, the thickness of the isolation barrier is approximately 7.4 µm, which is an adequate value for attaining at least 2.2 kV_{rms} reliable isolation voltage. Two identical transformers connected in series, one on each die, are employed in the design, thereby doubling the isolation voltage to 4.4 kV_{rms}. Nevertheless, the measurement indicates that the achieved isolation voltage amounts almost to a value twice as high - 7.8 kV_{rms} [64].

6.2 Transformer Design

The layout of the differential coreless transformer with a center-tapped primary coil is depicted in Fig. 6.3. The primary side coil is formed by the 1st and 2nd metal layers in parallel in order to reduce the serial resistance. The thickness of the top metal forming the secondary coil is 3 µm, which provides comparable serial resistance to the primary coil. As can be seen in Fig. 6.3, the direction of the upper coil turns is reverse to the direction of the lower coil turns. Owing to that, currents generated by an external electromagnetic field are subtracted from each other, thus providing EMI (Electromagnetic Interference) immunity. The transformer dimensions amount to 770 x 650 µm.

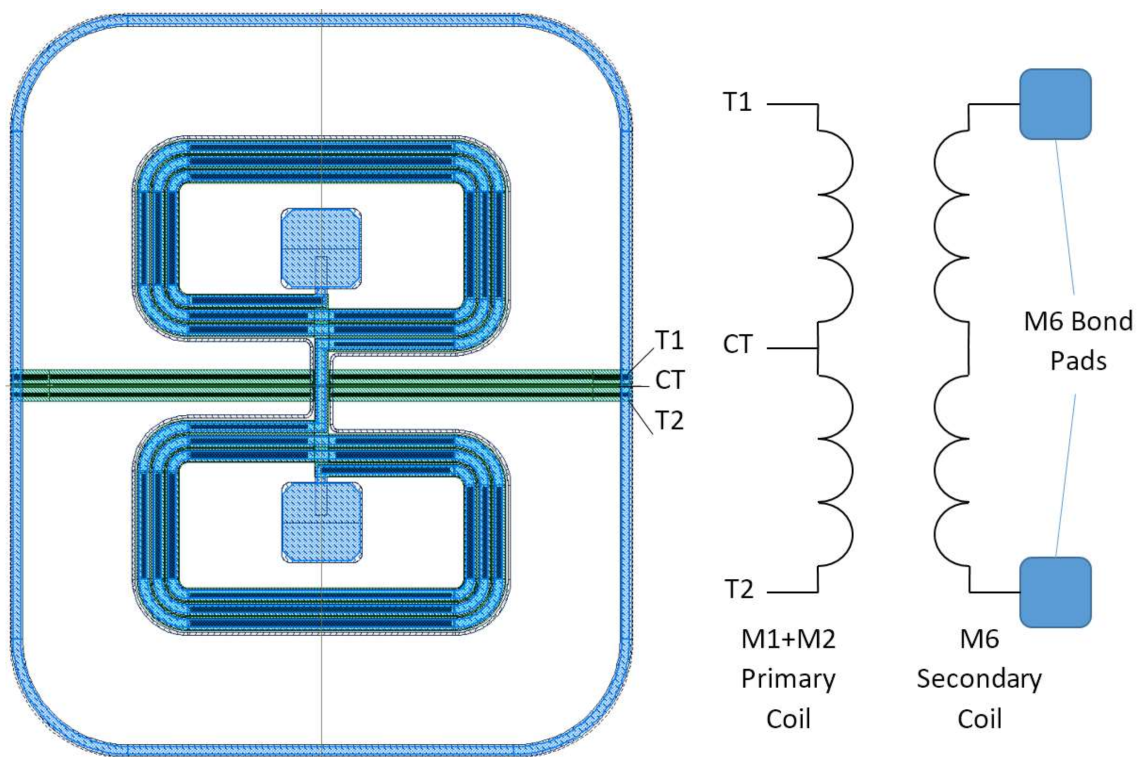

Fig. 6.3. Layout of differential coreless transformer with center-tapped primary coil.

Two different designs utilizing the differential coreless transformer have been prototyped and evaluated in this work:

- Bidirectional digital galvanic isolator, and
- analog galvanic isolator.

6.3 Communication through the Isolator

In comparison with the translator discussed in Chapter 4, the transformer-based translator is capable of transmitting a single pulse signal from the primary to the secondary side. Therefore, the ultra-wideband (UWB) pulse polarity modulation (PPM) is utilized in the designs discussed in this chapter, enabling a high data rate, low power consumption and low propagation delay communication through the isolator. The simulation results of the UWB modulation are depicted in Fig. 6.4. The logic high is assigned to the positive pulse and the logic low is assigned to the negative pulse. Fig. 6.4 B) demonstrates that the pulse width reaches approximately 320 ps, thus the transmitted amount of energy is significantly lower when compared to PWM or OOK modulation.

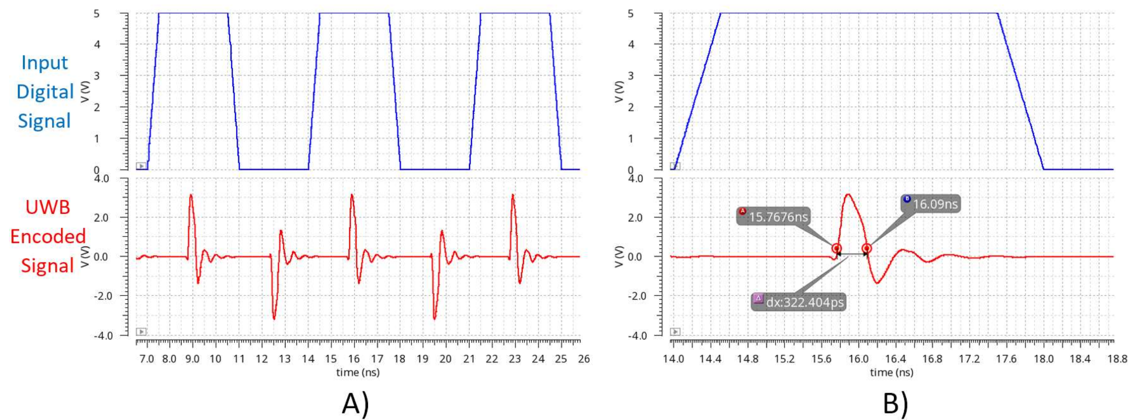

Fig. 6.4. UWB modulation. A) Simulation results. B) Detail of positive pulse representing logic high. Pulse width is approximately 320 ps.

6.4 Bidirectional Digital Galvanic Isolator

Contemporary bidirectional galvanic isolator products employ two individual unidirectional isolators, with one isolator assigned to the forward path signal flow and the other one to the reverse path, resulting in a duplex design that consumes a significant area. In order to merge the functionality of two inductively coupled channels into a single one between the two chips that transmit in both directions, time-division-duplexing (TDD) realized with UWB pulse polarity modulation transceiver is introduced. The block diagram is illustrated in Fig. 6.5.

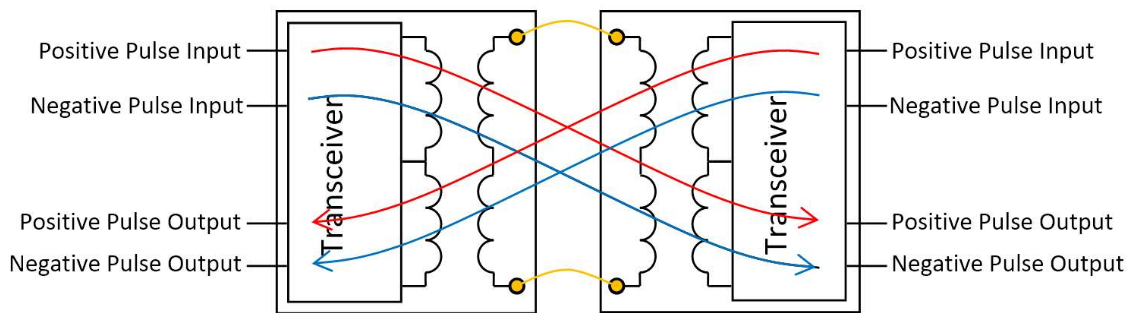

Fig. 6.5. Block diagram of implemented bidirectional digital galvanic isolator. Signal on positive and negative input is transmitted to positive and negative output of opposite transceiver, respectively.

The implemented design includes two identical chips interconnected via two bond wires. Each chip consists of a differential coreless transformer with a center-tapped primary coil and a transceiver connected to this primary coil of the transformer. The rising and the falling edge detector is connected to the positive and negative pulse input respectively. Depending on the input, the transmitter encodes the input data rising edge and falling edge to a differentially positive and negative impulse respectively. Encoding the input data rising and falling edges to short impulses (UWB) minimizes the transmit and receive signal time length, and also allows the channel to remain idle as long as the data value remains unchanged, which is desirable for TDD.

The schematic diagram of the transceiver is depicted in Fig. 6.6. The primary winding of the center-tapped transformer introduced in Section 6.2 is connected to the T1 and T2 terminals. The center tap (CT) is grounded. The 2.5 µA reference current for the receiver is provided internally by the current generator. Since the receiver is nearly insensitive to the reference current exact value, a basic generator utilizing a resistor and the VGS voltage of an NMOS transistor is designed. The output buffering inverters are inserted in order to provide the driving capability for driving either the input capacitance of the oscilloscope probe or off-chip decoder circuit.

Fig. 6.6 illustrates that the transmitter's output is directly connected to the receiver's input, thus essentially three blocks are responsible for the transmission, reception and distinction between the transmitted and received signals respectively:

- Transmitter,
- receiver, and
- blanking circuit.

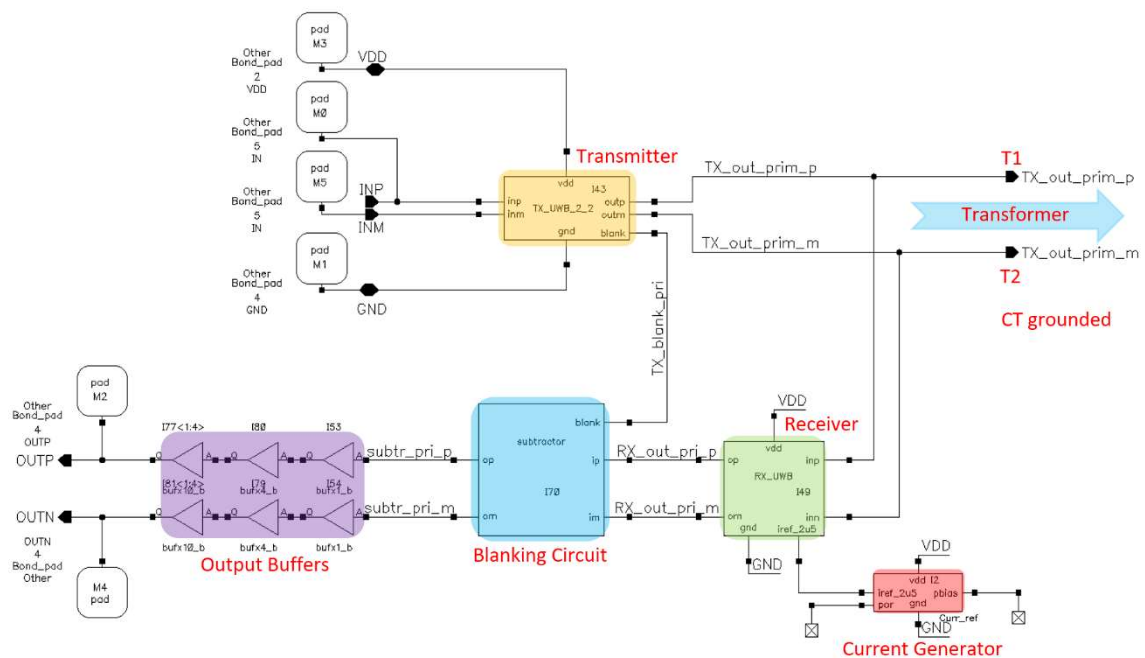

Fig. 6.6. Schematic diagram of the transceiver. Transceiver is connected to center-tapped primary coil by T1 and T2 terminals. Center tap is grounded.

The bond pads are also depicted in Fig. 6.6, illustrating that both the positive and negative branches of the input and output are bonded separately in order to attain system versatility.

6.4.1 UWB Transmitter

The transmitter generates UWB pulses in response to the input signal. The schematic diagram in Fig. 6.7 illustrates that the transmitter consists of two identical transformer drivers (OUTP, OUTM) differing in the edge detectors on their inputs. The upper and lower driver generates the UWB pulse on every rising and falling edge of the input control signal, respectively. Since the T1 and T2 transformer terminals are excited against the GND alternately, only a positive pulse is generated on both OUTP and OUTM outputs.

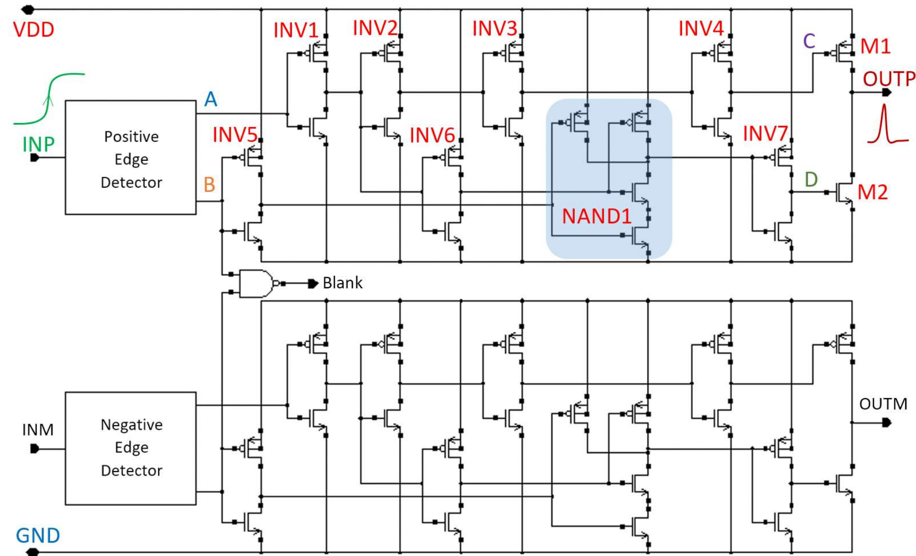

Fig. 6.7. Schematic diagram of the transmitter.

The simulation results are depicted in Fig. 6.8. The INV1 through INV4 are the buffering inverters utilized in order to provide the driving capability for the M1 output PMOS transistor. Owing to that, the C signal is in phase with the A signal, thereby driving the M1 to generate a positive pulse on the OUTP output. The D signal is a logic conjunct of the prolonged and inverted image of the A signal (B) and the A signal image on the output of the INV6 inverter. Consequently, the M2 NMOS transistor serves as an active snubber controlled by the INV7 buffering inverter (D) as depicted in Fig. 6.8 A) and B).

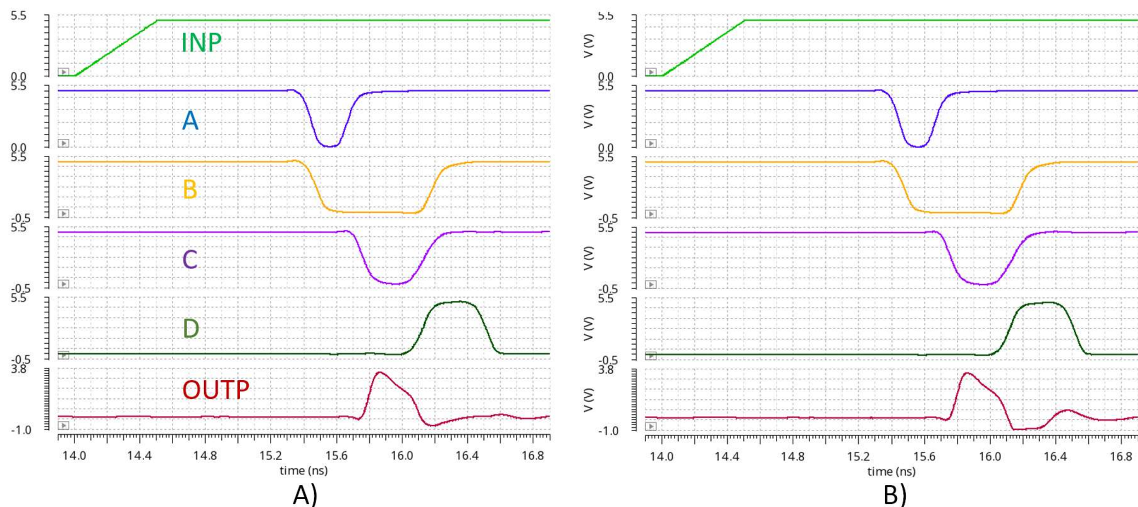

Fig. 6.8. Simulation results of UWB pulse generation in the transmitter: A) OUTP signal with M2 snubber active. B) OUTP signal with M2 snubber deactivated.

6.4.2 UWB Receiver

The UWB receiver provides demodulation of the UWB pulses. The schematic diagram of the receiver is depicted in Fig. 6.9. The T1 and T2 differential inputs are connected to the primary coil of the center-tapped transformer in a fashion similar to the transmitter. The received positive and negative pulse is outputted on the OUTP and OUTM receiver's outputs respectively.

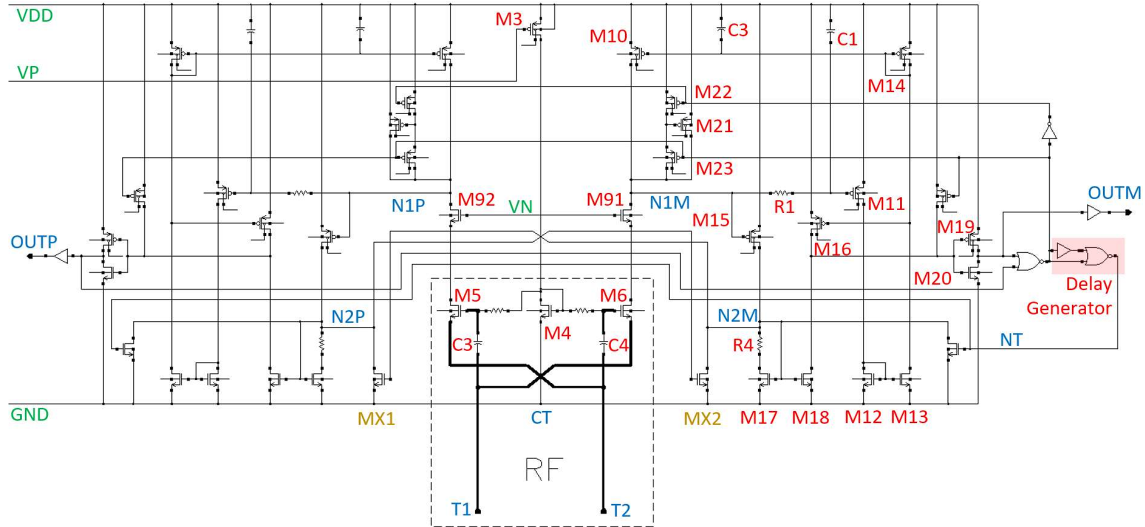

Fig. 6.9. Schematic diagram of the receiver.

The receiver utilizes the identical fundamental concept as the receiver discussed in Section 4.4. Since the aim of the UWB PPM demodulation is to differentiate between positive and negative pulses, the receiver's input stage is divided into positive and negative branches by cascoding the M5 & M6 input transistors separately. Subsequently, the second stage is doubled so that the positive and negative differential signal is processed individually. For the sake of clarity, the M9 cascode transistor and N1 node in Fig. 4.11 and Fig. 4.12 corresponds to the M91 & M92 transistors and the N1M & N1P nodes, respectively. The M3 current source is adjusted by the VP voltage and the M91 & M92 cascode is biased by the VN voltage in the same manner as depicted in Fig. 4.11. The transmitted and received pulse waveforms obtained in simulation are depicted in Fig. 6.10. As may be seen, the received pulse is substantially distorted; only the rising edge defines the pulse polarity. On that account, the receiver is first-edge-sensitive.

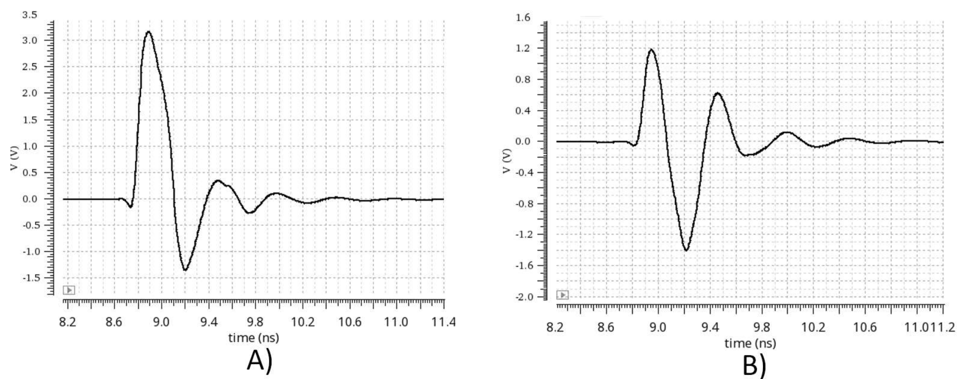

Fig. 6.10. Simulation results of UWB PPM pulses: A) Transmitted pulse. B) Received pulse.

As soon as the first edge of the received signal is detected and processed, both N1M and N1P nodes are clamped to VDD – V_{GS} voltage of M21 by switching the M22 and M23 transistors, thereby ignoring the remaining waveform of the received signal. The M21 and M11 transistors are matched and biased under identical voltage and current conditions, hence the N1M (N1P) node clamp voltage value is identical to that of the idle mode. The R2, R3 and C2 components (Fig. 4.11) are therefore removed in order to maintain the M10 V_{DS} voltage equal to the V_{GS} voltage of M11.

Fig. 6.11 illustrates the signal waveforms on the nodes highlighted in Fig. 6.9. As can be seen, in response to the polarity of the received signal, a negative pulse is generated on the N1M and N1P nodes. A positive feedback provided by the MX1 & MX2 cross-coupled transistors in Fig. 6.9 ensures that the order of the N1M and N1P negative transients determines whether a positive pulse is generated on the N2M or N2P node. Upon the N2M positive pulse creation, the N2P node is grounded by the MX1 transistor. Identically, the MX2 transistor grounds the N2M node if the N2P positive pulse has been generated sooner. The NT signal is formed by the delay generator in response to the logical disjunction of the OUTN and OUTP signals, in order to determine the OUTN or OUTP pulse width and to reset the receiver into the idle mode as soon as possible.

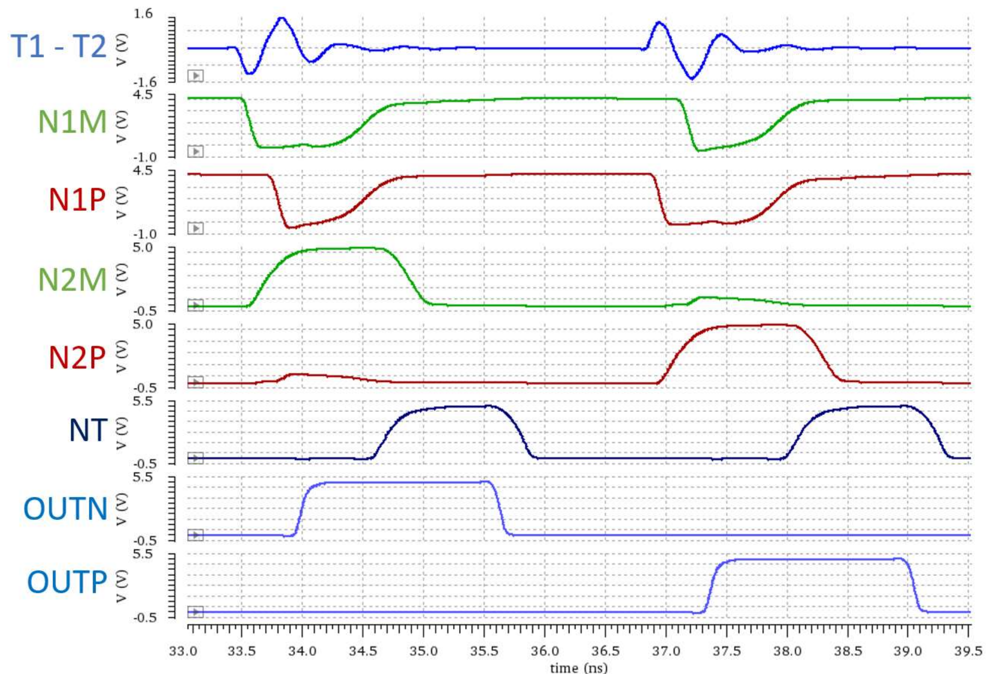

Fig. 6.11. Simulation results illustrating operation of the receiver. T1 – T2 differential input signal and several induced signals on nodes highlighted in Fig. 6.9 are depicted.

The simulation results shown in Fig. 6.11 also demonstrate that the receiver requires approximately 0.5 ns to propagate the first edge of the input signal to the OUTN or OUTP rising edge, that the OUTN and OUTP pulses on the output of the receiver reach 1.5 ns in width, and that the NT signal is terminated 0.5 ns after the OUTN or OUTP termination. That yields to a 2.5 ns active mode during which the receiver is occupied with the reception and is not able to process any other input signal, thereby limiting the bandwidth to 400 MHz.

6.4.3 Blanking Circuit

The blanking circuit, depicted in Fig. 6.12, is connected between the negative and positive receiver outputs and the respective chip's outputs to mute the receiver outputs during data transmission and hence to avoid self-interference from the chip's transmitter. The blanking circuit is triggered on the rising edge of the blank input signal generated in the transmitter (the blank output in Fig. 6.7) and mutes the output for a total time period determined by the DB delay generator. The DM and DP delay generators define the output pulse widths for each received impulse. It has been ensured that the pulses are wide enough to be detected by an external decoder (e.g. SR latch).

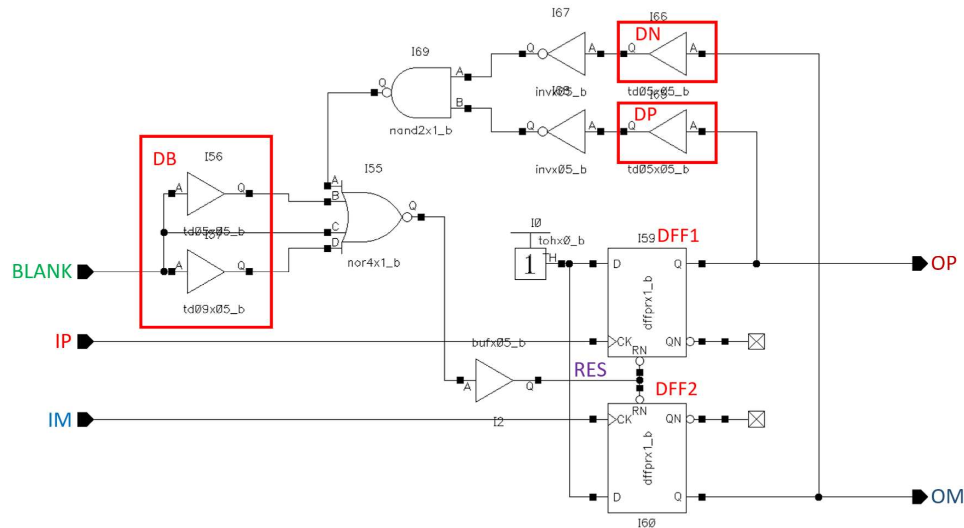

Fig. 6.12. Schematic diagram of the blanking circuit.

The simulation results in Fig. 6.13 demonstrate the circuit operation. The IP and IM input signals are gated by the DFF1 and DFF2 D flip-flops, which are reset by the RES signal lasting for the time interval given by the DB delay generator in response to the BLANK input. The connection of the IP and IM inputs to the CK input of the D flip-flops forms an edge-sensitive pass gate, thus the D flip-flops must be reset during the rising edge of the interfering signal only; it does not matter whether the IP or IM pulse lasts longer than the RES pulse. The Fig. 6.13 B) demonstrates that the incoming pulse from the opposite transmitter is not blanked, since the RES signal is high (i.e. not active) at that time.

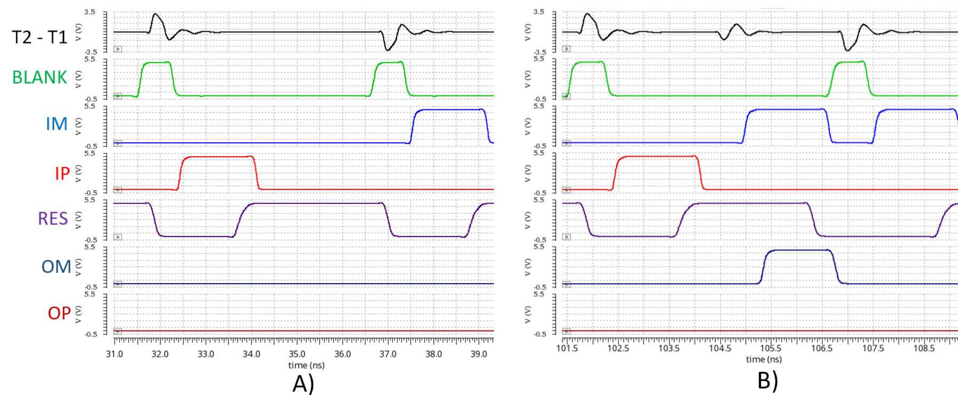

Fig. 6.13. Simulation results of the blanking circuit: A) Unidirectional operation. Interfering signals are blanked by RES signal logic low. B) Bidirectional communication. Negative pulse received from opposite chip is not blanked.

6.4.4 Evaluation of the Bidirectional Digital Galvanic Isolator

The bidirectional digital galvanic isolator has been prototyped and encapsulated in a fashion similar to the galvanically isolated systems discussed in Chapters 4 and 5. The SOIC-16 Dual Flag package has been utilized to assembly low voltage and high voltage dice as a multi-chip module, as illustrated in Fig. 6.14.

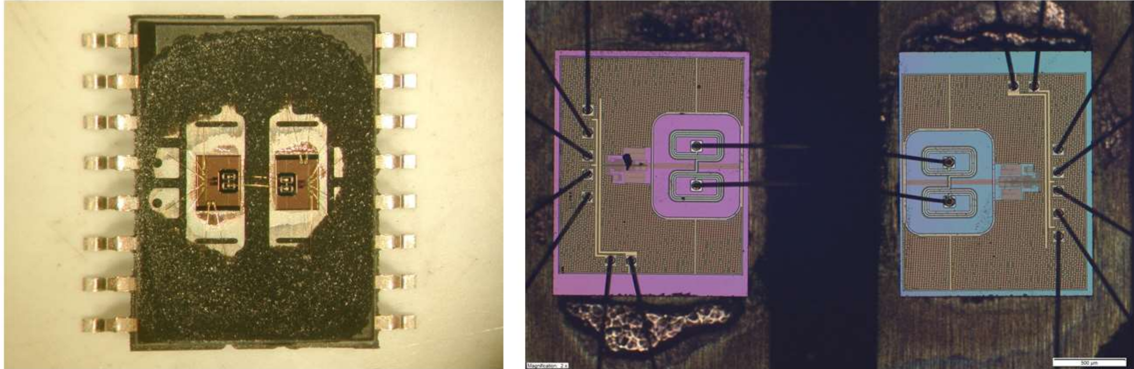

Fig. 6.14. System module assembled in SOIC-16 Wide Body package. A) Locally de-capsulated IC. B) Micrograph with both chips.

The galvanic isolator has been evaluated in the test configuration depicted in Fig. 6.15. The external RS1 and RS2 flip-flops have been inserted to decode the output pulses back to a square wave signal. The high side is also equipped with the V5 voltage regulator in order to provide 5 V floating power supply during CMTI measurements. The low and high side inputs are terminated by 50 ohm resistance to match the characteristic impedance of the transmission line between a pulse generator and the test board. Both the pulse and square wave output signals are accessible on the LS and HS output terminals. The high dV/dt generator for the CMTI measurements is connected to the CMTI terminals.

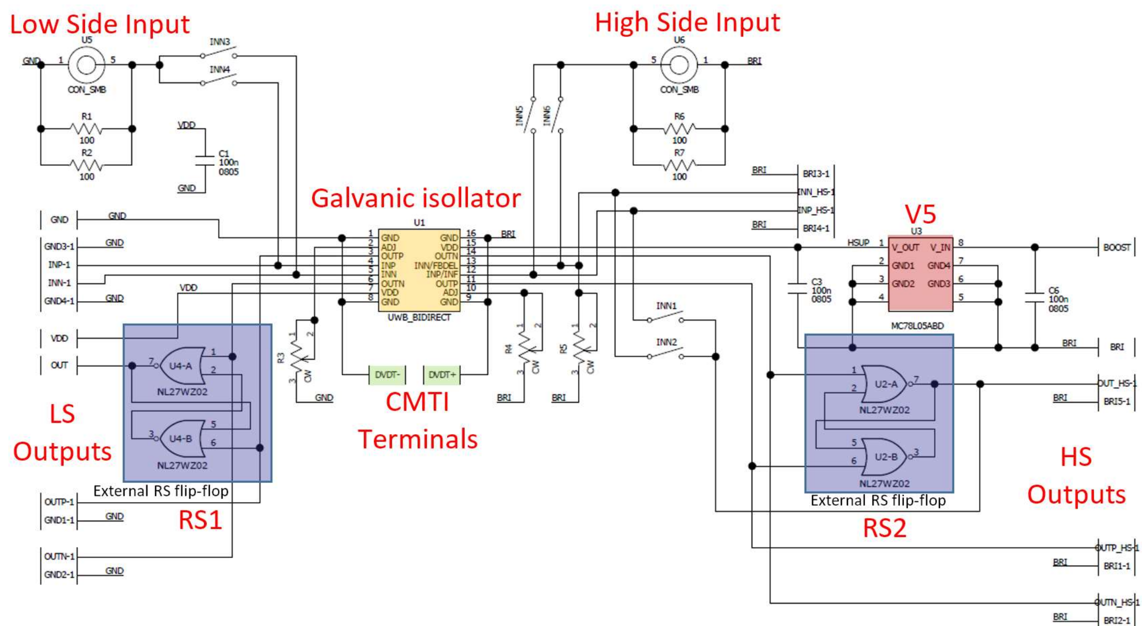

Fig. 6.15. Schematic diagram of the bidirectional digital galvanic isolator test configuration.

The measured waveforms of the unidirectional operation are illustrated in Fig.6.16. The RS flip-flop has not been utilized and both positive and negative inputs have been shorted together in the measurement. The galvanic isolator reaches stable operation for the 150 MHz input control signal frequency that results in 300 Mb/s data rate, since each input pulse generates two output pulses – OUTP and OUTN at the rising and falling edge of the input signal, respectively.

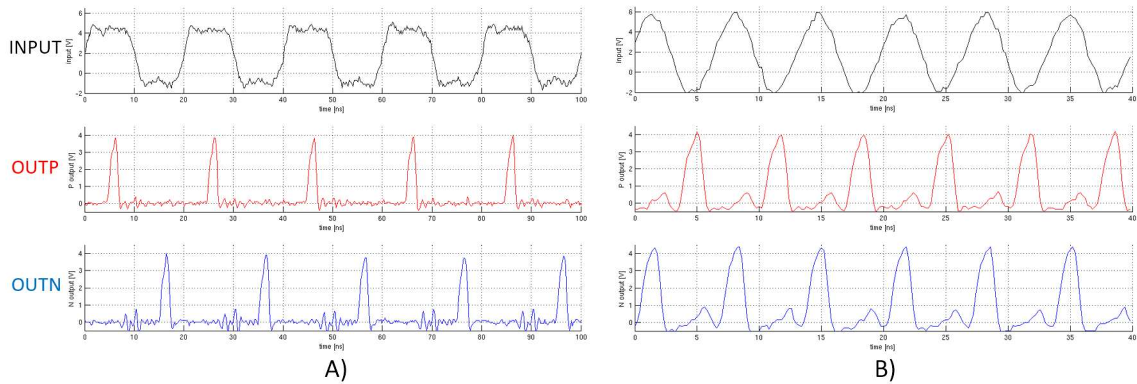

Fig.6.16. Measured waveforms of unidirectional operation of the galvanic isolator without external R-S flip-flop. A) 50 MHz operation. B) 150 MHz operation.

The bidirectional operation is demonstrated in Fig.6.17. The positive and negative control signal inputs are shorted together to provide both positive and negative output pulses in response to a single control signal. The external RS flip-flops generate a significant phase shift as may be seen in Fig.6.17 A). Fig.6.17 B) illustrates that in the bidirectional mode, the galvanic isolator achieves stable operation for the 68 MHz input control signal frequency resulting in 136 Mb/s simultaneous data rate in both directions. Certainly, for the bidirectional operation, precise timing is essential in order to avoid the transmitted and received pulses interfering with each other.

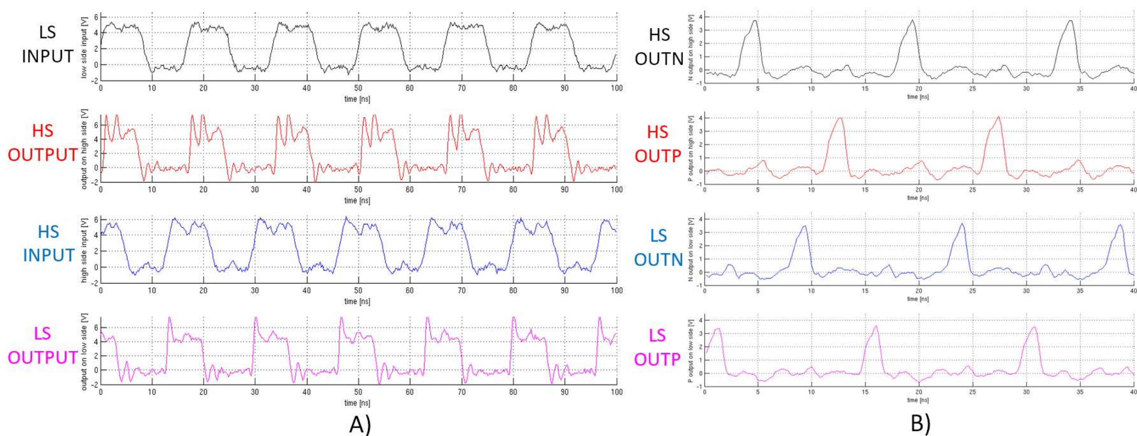

Fig.6.17. Measured waveforms of bidirectional operation of the galvanic isolator. A) 60 MHz operation utilizing external RS flip-flops. B) 68 MHz operation without external RS flip-flops. Only outputs are shown due to limitation of oscilloscope probes number.

The measured propagation delay of the control signal from the input to the output through the galvanic isolation barrier amounts to 4.3 ns.

A closed-loop configuration has been utilized to evaluate the CMTI of the bidirectional galvanic isolator. Both low and high side RS flip-flops has been employed to provide the rectangular output signal. The output of the high side RS flip-flop has been connected to the positive and negative high side inputs, both shorted together, thus the high side output signal is instantly transmitted back to the low side and showing on the low side output. The high dV/dt generator has been connected to the CMTI terminals (Fig. 6.15) to provide the positive and negative slope of the test signal. Examples of the measured waveforms are depicted in Fig. 6.18.

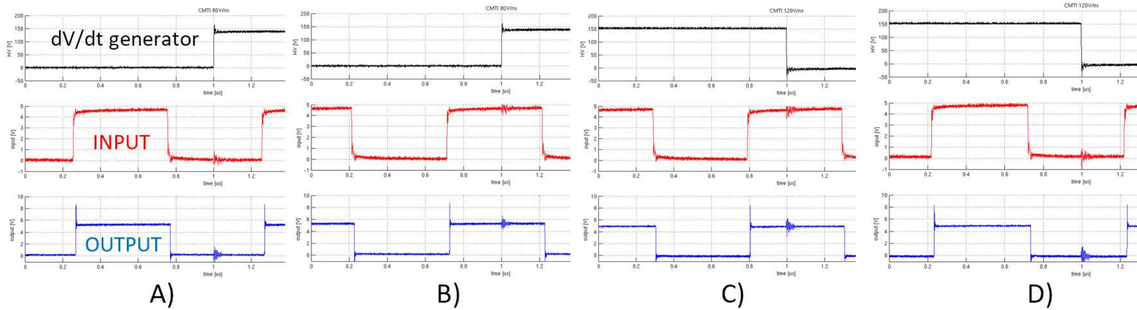

Fig. 6.18. CMTI measurement. A) Positive dV/dt slope at input low. B) Positive dV/dt slope at input high. C) Negative dV/dt slope at input high. D) Negative dV/dt slope at input low.

The galvanic isolator operates stably at 80 and 120 V/ns positive and negative slope, respectively. The current consumption is listed in Table 6.1.

Table 6.1. Bidirectional digital galvanic isolator current consumption.

Data Rate [Mb/s]	20	100	200	300
TX current [mA]	0.74	3.55	7.09	11.1
RX current [mA]	0.47	2.20	4.40	7.40

6.4.5 Results and Discussion

The galvanic isolator reaches stable unidirectional operation for the 150 MHz input control signal frequency that results in a 300 Mb/s data rate. In the bidirectional mode, the galvanic isolator achieves stable operation for the 68 MHz input control signal frequency resulting in a 136 Mb/s simultaneous data rate in both directions. The attained data rate is limited by the internal blanking circuit adapted for the oscilloscope probe measurement, which constrains the pulse widths provided by the outputs of the isolator. A higher frequency operation is expected in full integration designs.

The measured propagation delay does not even reach 5 ns, which represents an excellent value in comparison with contemporary galvanic isolator designs.

The CMTI measurement reveals greater sensitivity to common mode transients. The CMTI to the positive and negative slope amounts to 80 and 120 V/ns, respectively. These values are most likely limited by the external components and connections. Nevertheless, in order to attain greater CMTI values, a more complex coding must be implemented.

The measured current consumption at 100 MHz, representing 200 Mb/s, amounts to 7 mA on the transmitter and 4.4 mA on the receiver when receiving. The receiver in the idle mode consumes less than 100 µA.

6.5 Analog Galvanic Isolator

In order to establish sufficient voltage and current regulation, converters generally employ feed-back loop systems. In the case of AC-DC converters supplied from the AC mains, it is also essential meet the international standards [39], [40] to protect users from a potential electric shock in case of application failure. Therefore, the secondary low voltage circuits must be galvanically isolated from the primary high voltage circuits in order to remain user-safe in case of a direct contact. The typical AC-DC applications do not transmit a digital signal through the isolation barrier due to the necessity for an Analog-to-Digital (A-D) and Digital-to-Analog (D-A) converters, thereby increasing the application complexity, current consumption and cost. It is significantly less complex to generate, send and process an analog signal. The opto-coupler is the typical device employed for this purpose, ensuring outstanding galvanic isolation while keeping the complexity of the application at a low level.

However, the opto-coupler is usually one of the more expensive devices in the system. For that reason manufacturers embrace any other cost-effective designs. Moreover, omitting the rest of passive devices, the typical AC-DC system consists of primary and secondary side controllers and the opto-coupler. These three devices are from the communication standpoint in direct connection, thus it is preferable to integrate them together within a single package. Nevertheless, owing to the opto-coupler manufacturing process complexity and its cost, combined integration of these three devices is not a sensible concept.

This section introduces the design of the analog galvanic isolator which utilizes the galvanically isolated translator discussed in Section 6.4. The aim of this design is to find a replacement of the standard opto-coupler employed in typical isolated flyback applications. Such approach is highly suitable for the full module integration of the primary and secondary side controllers into the one single package. The block diagram of such opto-coupler replacement test structure is shown in Fig.6.19.

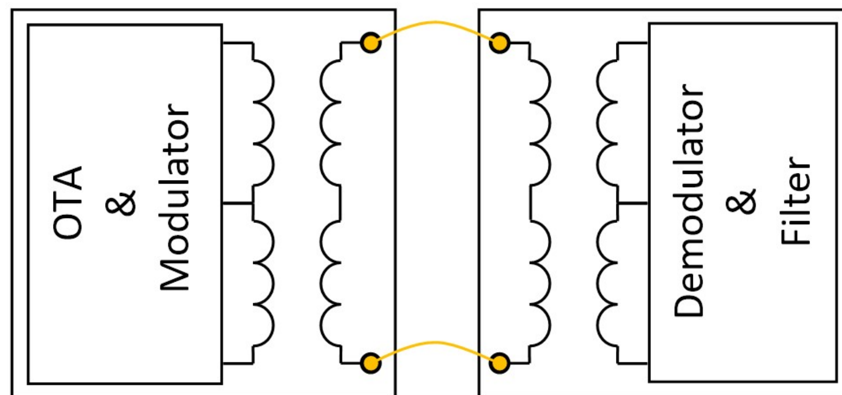

Fig.6.19. Block diagram of analog galvanic isolator test structure. Low voltage die houses operational transconductance amplifier and modulator. Demodulator and output filter are located on high voltage die.

6.5.1 Low Voltage Die

The schematic diagram of the low voltage die bearing the operational transconductance amplifier, modulator and transmitter is depicted in Fig. 6.20. The transmitter and its connection is identical to the one utilized in the bidirectional isolator in Section 6.4. The analog and digital power domains are separated to avoid potential interference.

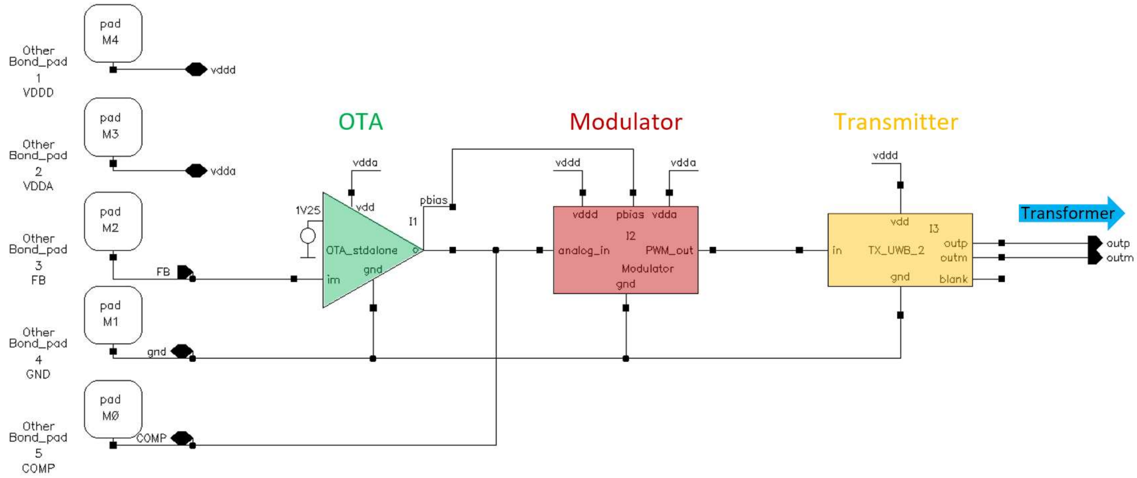

Fig. 6.20. Schematic diagram of low voltage die.

6.5.2 Operational Transconductance Amplifier and Modulator

The operational transconductance amplifier (OTA) is typically utilized in the feedback systems of the non-isolated DC-DC converters. Since the galvanic isolator is employed in this application, the OTA becomes a sensible candidate to be utilized as the negative feedback amplifier. The 1.25 V reference and the FB feedback voltages are applied to the positive and negative inputs of the OTA, respectively. The current mode output of the OTA charges or discharges an external compensational capacitor, which is connected to the COMP terminal, in response to the FB voltage value. The input terminal of the modulator senses the COMP voltage and compares its value with the voltage provided by a sawtooth wave generator, thus the modulator encodes the COMP voltage value into the PWM signal, as illustrated in Fig. 6.21. The generated PWM signal is transmitted to the high voltage die in a fashion similar to the bidirectional isolator in Section 6.4.

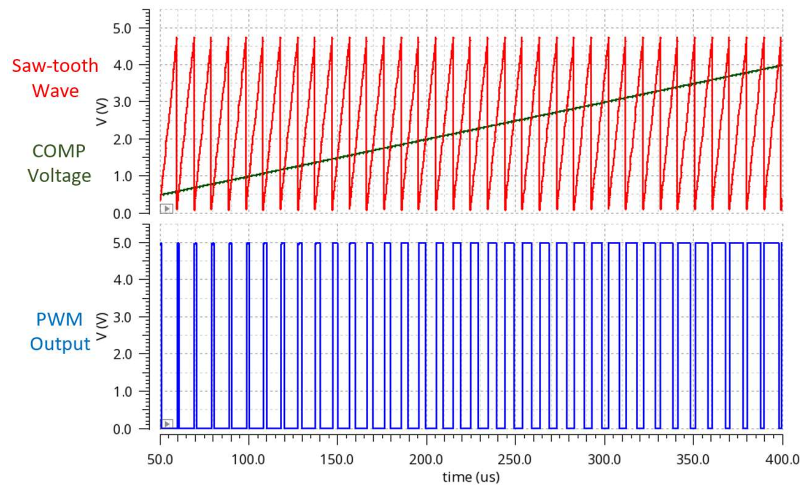

Fig. 6.21. Encoding of COMP voltage value into PWM signal.

6.5.3 High Voltage Die

The schematic diagram of the high voltage die, depicted in Fig. 6.22, utilizes the identical receiver and current reference designs as the bidirectional isolator discussed in Section 6.4. The positive and negative output of the receiver is connected to the set and reset terminal of the RS flip-flop, respectively, thus the PWM signal representing the analog COMP value is obtained on the output of the RS flip-flop.

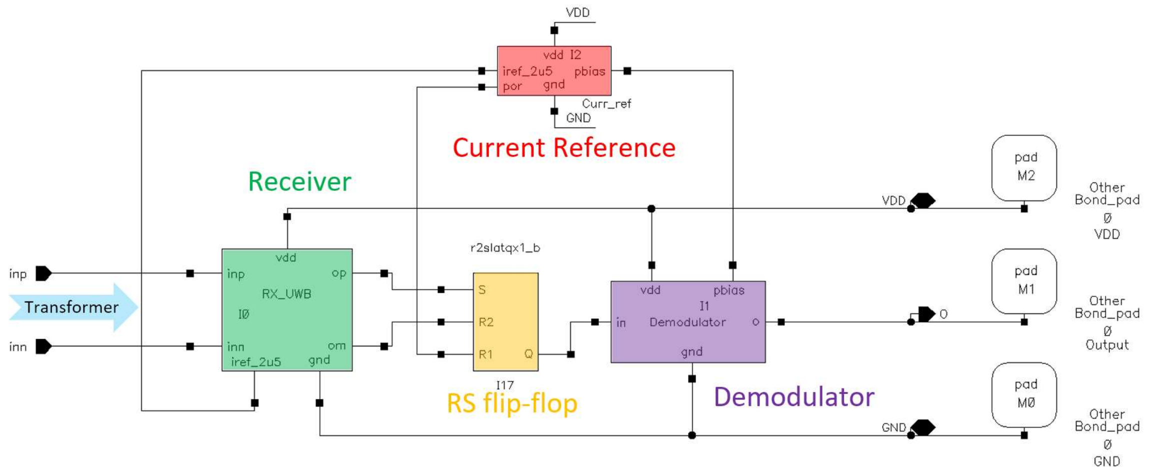

Fig. 6.22. Schematic diagram of high voltage die.

6.5.4 Demodulator

The demodulator decodes the PWM to analog COMP voltage and provides that value to the output of the high voltage die. The schematic diagram of the demodulator is depicted in Fig. 6.23. The PWM signal directly controls the four switches that charge or discharge the four capacitors (storage elements) to the instant value of the low-pass filtered signal. As the result, the minimum and maximum value of the filtered signal ripple is stored in the 3rd and 4th capacitor, respectively. The capacitor voltages are buffered by the operational amplifiers and the average of the minimum and maximum ripple value, representing the analog COMP value, is obtained on the common connection of the R resistors possessing the identical value. In order to provide sufficient driving capability for external circuit components, the COMP analog value is coupled to the output of the high voltage die through the buffering operational amplifier (not shown).

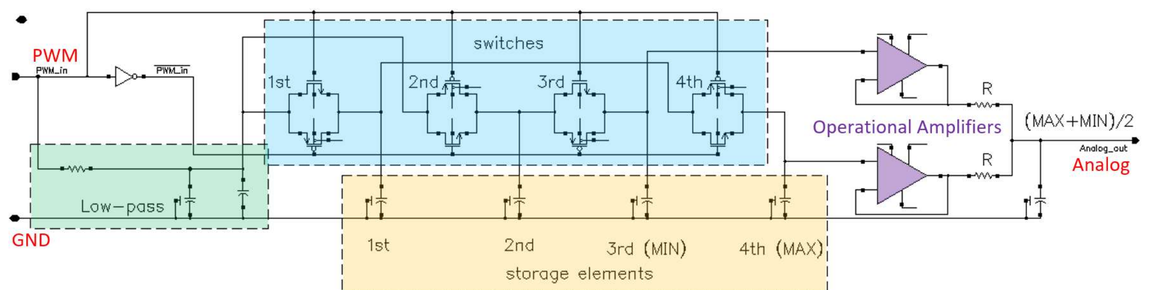

Fig. 6.23. Schematic diagram of demodulator. Storage elements (capacitors) are charged or discharged by switches, to instant value of low-pass filtered signal, controlled by PWM input signal. Analog COMP value is obtained on the common node of R resistors.

The simulation results illustrating the operation of the demodulator are depicted in Fig. 6.24. As is shown, the transmitted PWM COMP signal is demodulated and the analog COMP value is restored on the output of the demodulator.

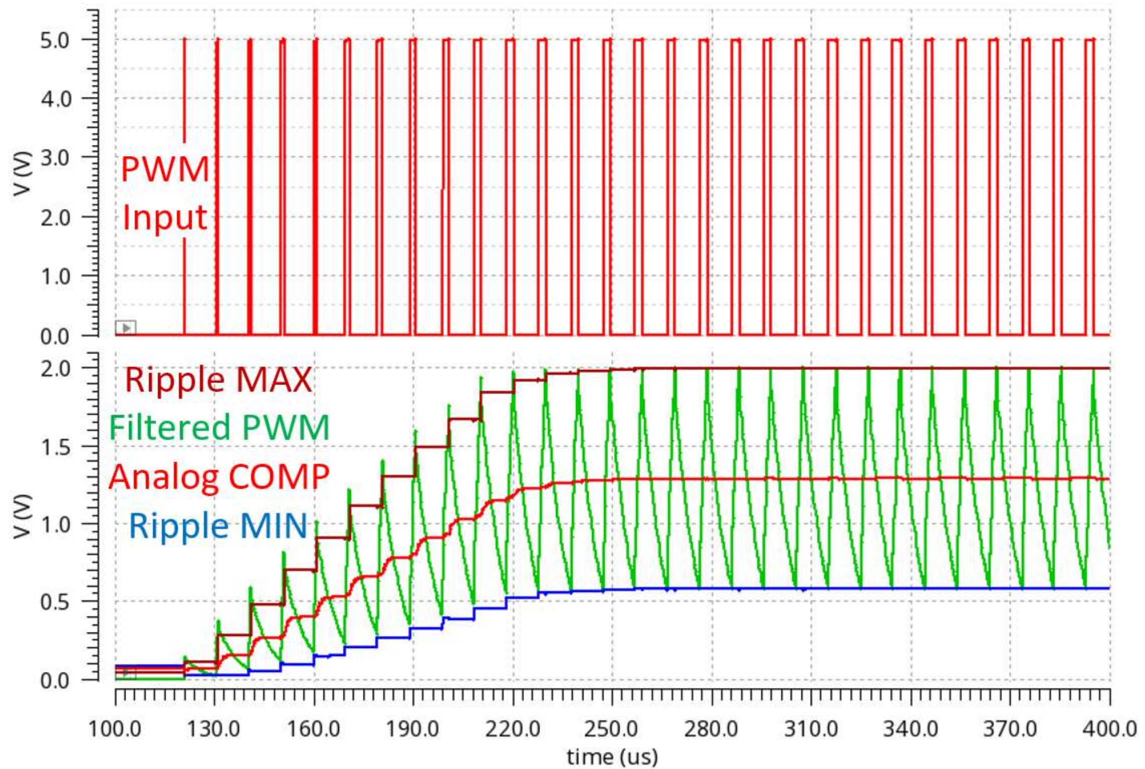

Fig. 6.24. Simulation results of demodulator. Ripple MIN and ripple MAX waveforms are generated on 3rd and 4th capacitor in Fig. 6.23, respectively. Analog COMP waveform is obtained by averaging of MIN and MAX waveforms.

The demodulator design has been submitted to the US patent office by the author of this Thesis.

6.5.5 Evaluation of the Analog Galvanic Isolator

The analog galvanic isolator has been prototyped and encapsulated in the same manner as the bidirectional digital isolator illustrated in Fig. 6.14. Two sets of tests have been performed to evaluate the modulation, transmission and demodulation of an analog signal:

- Transmission of a sine wave applied on the COMP terminal,
- employment of the design in the real isolated flyback application.

The carrier frequency of the modulator has been set to 100 kHz as a compromise value between the resulting time constant of the isolator system and power consumption. The measured current consumption at 100 kHz amounts to approximately 60 µA on the transmitter side, which represents a significantly lesser value in comparison with the standard opto-coupler designs that require current in the order of mA. The receiver side current consumption amounts to 90 µA, which also does not exceed the current consumption of the designs utilizing the opto-couplers.

Fig. 6.25 illustrates the measured response to sine wave signals applied on the COMP terminal. The aim of this test was to evaluate the phase angle between the input and output sine wave signals. The measured time delay amounts to approximately 17 µs, which corresponds with the 7.4 kHz pole. Such value is sufficiently high not to affect the feedback loop stability of the typical flyback converter.

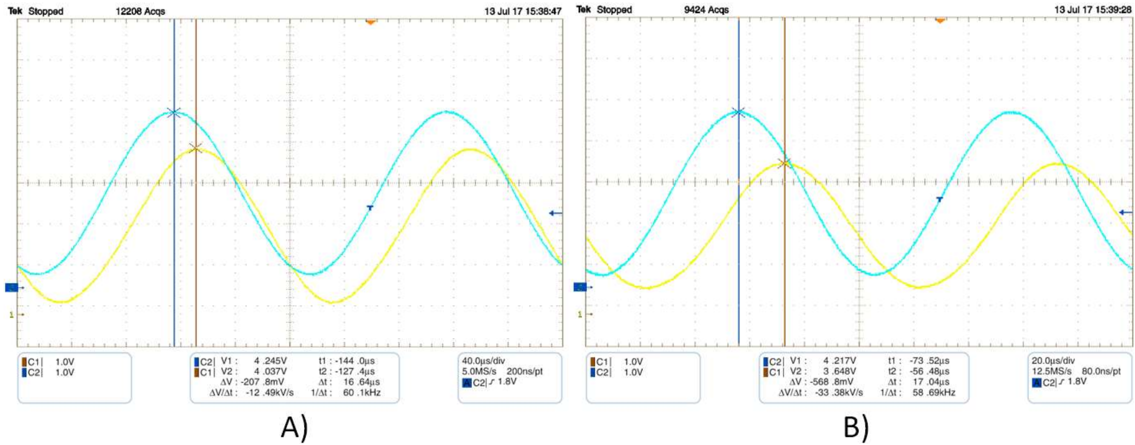

Fig. 6.25. Measured response to sine wave signal applied on the COMP terminal. Blue – COMP input, yellow – demodulator output. Waveforms are averaged. A) 5 kHz. B) 10 kHz. Measured time delay amounts to 17 µs.

In the final test, the analog galvanic isolator was inserted into the typical flyback converter design employing the NCP1234 controller [65], depicted in Fig.6.26.

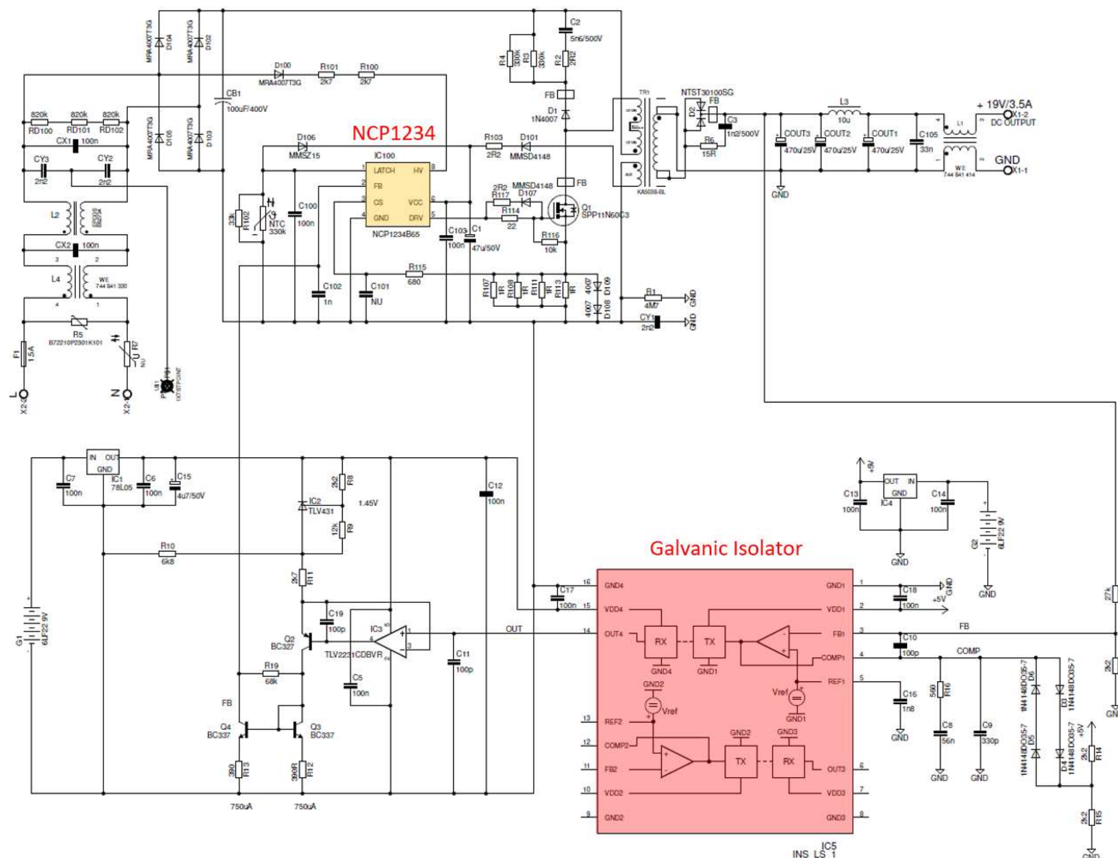

Fig.6.26. AC-DC converter application utilizing analog galvanic isolator.

The load step response from 100 mA to 1.5 A of the AC-DC flyback converter utilizing the analog galvanic isolator is depicted in Fig.6.27. As may be seen from the waveforms, the analog isolator replaces the opto-coupler adequately. The controller provides a stable step response from light to full and full to light load conditions.

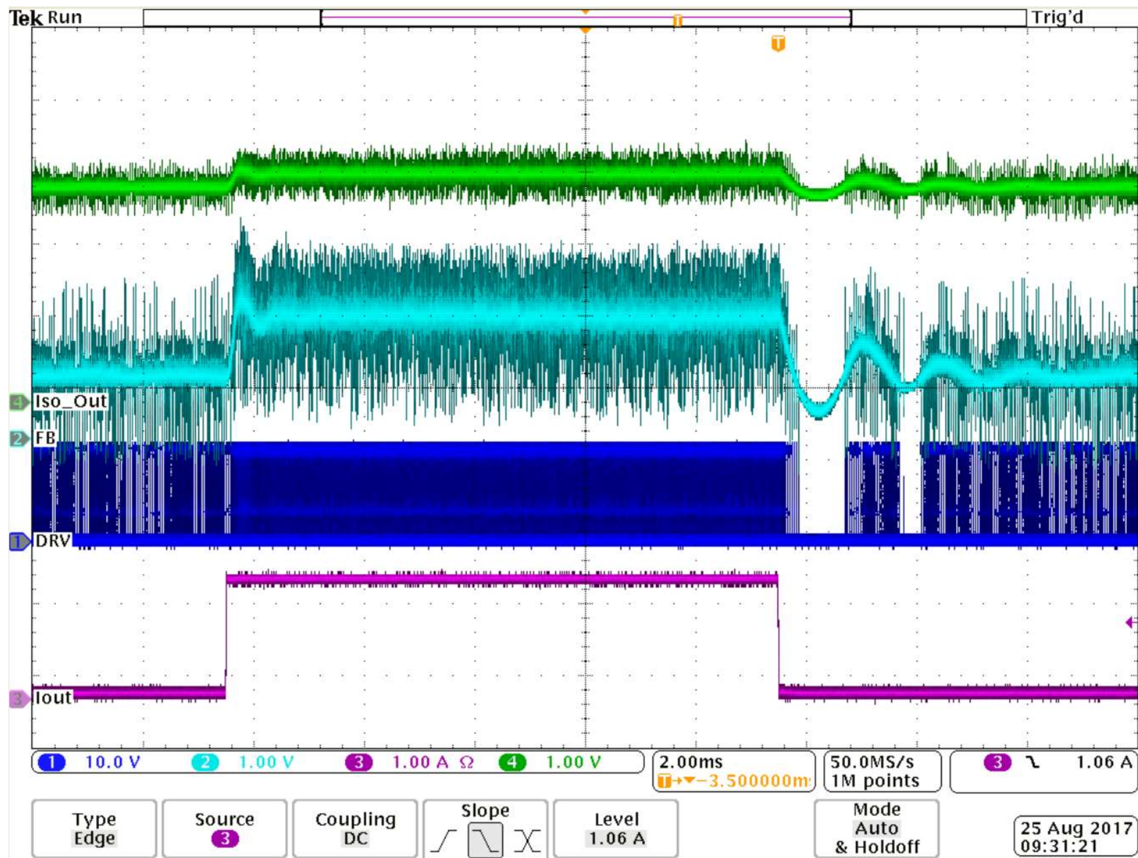

Fig.6.27. Measured waveforms of AC-DC flyback converter application utilizing the opto-coupler replacement – load step response. Green – demodulator output, cyan – FB terminal of NCP1234, blue – DRV terminal of NCP1234, violet – load current.

6.5.6 Results and Discussion

The analog galvanic isolator is a part of the subsequent design stemming from the bidirectional galvanic isolator. The analog isolator has been tested in real AC-DC converter application as a replacement of the standard opto-coupler. A stable step response, from the light (100 mA) to full (1.5 A) and full to light load conditions, has been achieved. The bandwidth of the analog galvanic isolator is reduced by the introduction of an extra pole, whose frequency is directly given by the carrier frequency modulating the analog signal. In the discussed flyback application, the 100 kHz carrier frequency has been utilized, thereby achieving the 7.4 kHz pole. Such value is comparable to the frequency of an extra pole introduced by the standard opto-coupler, thus is adequate for the typical flyback applications. For applications requiring a higher pole frequency, the carrier frequency must be increased. The measured current consumption at 100 kHz amounts to approximately 60 μA on the transmitter side, which represents a significantly lesser value in comparison with the standard opto-coupler designs that require current in the order of mA. The receiver side current consumption amounts to 90 μA, which also does not exceed the current consumption of the designs utilizing the opto-couplers.

7 CONCLUSION

1) Design of 800 V Galvanically Isolated Translator

The first aim of this Thesis was to design a galvanic isolation suitable for HV applications that require either measuring high voltages or communicating between different voltage domains. The development was divided into two consecutive steps:

- Design of the galvanically isolated translator.
- Design of the galvanically isolated HB driver for industrial applications.

The design of the galvanically isolated translator was divided into three basic blocks:

- Transmission line,
- transmitter,
- receiver.

Transmission Line
Instead of the typical vertical transformer or a high voltage capacitor, the proposed method utilizes lateral on-chip spacing between resonant structures to provide galvanic isolation. In order to achieve low signal attenuation, all transmission line components, such as the adjacently coupled resonators, have been tuned precisely to the same resonant frequency using extra test structures:

- Capacitor value skews of the coupled resonators.
- Reduced transmission line with one coupled resonator removed.
- Transmitter generating pulse bursts.
- Transmitter generating continuous signal.
- Receiver outputting digital signal.
- Receiver outputting analog signal corresponding to received signal strength.

To the best of the author's knowledge, this case of CMOS lateral resonant coupling being utilized and investigated in chip-to-chip communication is yet unprecedented. This technique has been proved as a viable way to increase the maximum achievable isolation rating in fully-integrated CMOS galvanic isolation designs.

Transmitter
In order to avoid the need of using extra on-chip inductors, the transmitter oscillator was connected directly to the first coupled resonator of the transmission line. The oscillator frequency was tuned to the resonant frequency of the adjacently coupled resonators.

Receiver
A completely novel design of an RF detector featuring very low stand-by current consumption and high sensitivity has been introduced by the author of this Thesis.

Communication through the Galvanically Isolated Translator
The galvanically isolated domains communicate with each other via the means of digital signals. For that purpose, two AC carrier techniques relying on modulation and demodulation have been utilized:

- OOK, and
- PWM.

The OOK digital modulation seemed a sensible candidate for high-bitrate applications. For low power applications, the PWM communication has been selected.

Design of Galvanically Isolated Half Bridge Driver for Industrial Applications
The galvanically isolated half bridge driver for industrial applications has proved itself a viable target application for the galvanically isolated translator utilizing lateral resonant coupling. Two parts of the half bridge driver have been designed:

- Low voltage die employing the transmitter,
- high voltage die employing the receiver.

The presented design of the half bridge driver amply satisfies the industrial application requirements such as high negative transient immunity and high CMTI.

2) Design of GI Translator for HV Applications Complying with the Safety Standards

In order to achieve as high galvanic isolation level as possible, the second goal set by this Thesis was the design of a galvanically isolated translator utilizing two vertical transformers connected in series. Although a communication scheme similar to the one utilized for lateral coupling may be employed, the UWB pulse polarity modulation has been utilized instead, enabling a high data rate, low power and low propagation delay communication through the isolator. The core of the receiver design, developed for the lateral coupling in the first phase of this work, has also been employed in the UWB receiver. In order to evaluate this concept, two structures have been designed:

- Bidirectional digital galvanic isolator, and
- analog galvanic isolator.

The design of the bidirectional digital isolator reliably allows using only a single galvanic isolator for communication in both, low-to-high and high-to-low, directions. This approach greatly reduces the area consumed by the isolator.

The analog galvanic isolator was introduced as a part of the subsequent design stemming from the bidirectional galvanic isolator. The analog isolator has been tested in a real AC-DC converter application as a replacement of the standard opto-coupler. This design enables full integration of primary and secondary side controllers in a single package, thereby reducing the complexity and cost of the AC-DC converters.

Future Work

The current consumption of the transmitter in the galvanically isolated translator must be optimized in the future design. The 2.8 GHz oscillator frequency seems to be a boundary value for the 5 V MOSFET transistors available in the ONC25BCD process, resulting in high current requirements of the oscillator. Another fabrication process providing transistors featuring higher transit frequency must be selected.

The GI translator for HV applications must be proven in target applications. Sensible candidates are:

- The half bridge driver, and
- AC-DC primary side controller integrated with the secondary side controller in a single package.

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