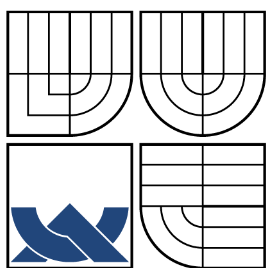

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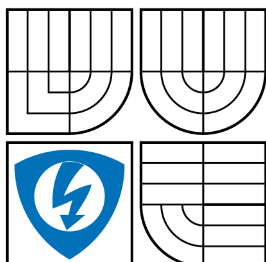

FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION
DEPARTMENT OF MICROELECTRONICS

FAKULTA ELEKTROTECHNIKY A KOMUNIKAČNÍCH TECHNOLOGIÍ
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HIGH-VOLTAGE DEVICES IN SMART POWER TECHNOLOGY

VYSOKONAPĚŤOVÉ SOUČÁSTKY V MODERNÍCH BIPOLÁRNÍCH TECHNOLOGIÍCH

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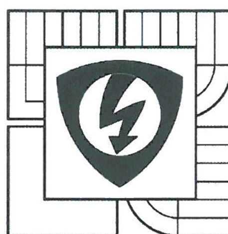

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Study on the design of high-voltage components in advanced BCD technology. Focus on their function and use in integrated circuits.
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ABSTRACT

This work describes fundamental characteristics of LDMOS transistors. In the first part of work are described properties of LDMOS transistors, the basic parameters and techniques to improve parameters of transistors. The next section discusses the reliability of LDMOS transistors. This section describes the safe operating area (SOA), hot carrier injection (HCI) and negative bias temperature instability (NBTI). The last theoretical section describes models used to simulate ESD events. The practical part is focused on simulation of the basic parameters PLDMOS and NLDMOS transistors and comparison of simulated and measured concentration profiles. Furthermore the thesis deals with simulation of the impact of changes in geometrical parameters of the PLDMOS transistor and the impact of these changes on the electrical parameters. The last part contains TLP simulations which examines electrical properties of PLDMOS transistor when is used as ESD protection.

KEYWORDS

TCAD, LDMOS, ESD, sensitivity to geometrical parameters

ABSTRAKT

Tato práce se zabývá popisem základních vlastností LDMOS tranzistorů. V první části práce jsou rozebrány vlastnosti LDMOS tranzistorů, jejich základní parametry a techniky pro vylepšení parametrů těchto tranzistorů. V další části je rozebrána spolehlivost LDMOS tranzistorů, tato část popisuje bezpečnou pracovní oblast (SOA), injekci horkých nosičů (HCI) a negativní teplotní stabilitu (NBTI). Poslední teoretická část popisuje používané modely pro simulaci ESD událostí. Praktická část práce je zaměřena na simulaci základních parametrů PLDMOS a NLDMOS tranzistorů, porovnání simulovaných a změřených koncentračních profilů. Dále se práce zabývá simulacemi změny geometrických parametrů PLDMOS tranzistoru a vliv těchto změn na elektrické parametry. Poslední část práce tvoří TLP simulace, které zkoumají elektrické vlastnosti PLDMOS tranzistoru při použití jako ESD ochrana.

KLÍČOVÁ SLOVA

TCAD, LDMOS, ESD, citlivost k geometrickým parametrům

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DECLARATION

I declare that I have written my master's thesis on the theme of "High-Voltage Devices in Smart Power Technology" independently, under the guidance of the master's thesis supervisor and using the technical literature and other sources of information which are all quoted in the thesis and detailed in the list of literature at the end of the thesis.

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Brno ....

(author's signature)

CONTENTS

Introduction **11**

1 Lateral Diffused MOSFET **12**
1.1 Lateral Diffused NMOSFET . . . 12
1.2 Current Transport . . . 13
1.3 Breakdown Voltage and R_{DSon} . . . 13
1.4 Parasitic Bipolar Transistor . . . 14
1.5 Reduced Surface Fields Principle . . . 15

2 Safe Operating Area **17**
2.1 Electrical Safe Operating Area . . . 17
2.2 Hot Carrier Injection . . . 17
2.3 Negative Bias Temperature Instability . . . 19

3 Electrostatic Discharge **21**
3.1 Human Body Model . . . 21
3.2 Machine Model . . . 22
3.3 Transmission-line Pulse Testing . . . 23
3.4 Snapback Devices . . . 24

4 Application of High Voltage Devices **25**
4.1 Lateral Diffused MOSFET . . . 25
4.2 Bipolar Transistor . . . 26
4.3 High Voltage Diode . . . 26

5 TCAD simulation **27**
5.1 Device structure . . . 27
5.2 Breakdown voltage . . . 29
5.3 Threshold voltage . . . 31
5.4 Saturation regime and R_{DSon} . . . 32
5.5 Concentration profile . . . 34
5.6 Sensitivity to geometrical parameters . . . 36
5.6.1 Simulation of L_{G} change impact . . . 36
5.6.2 Simulation of L_{STI} change impact . . . 37
5.6.3 Simulation of L_{ACC} change impact . . . 38
5.6.4 Simulation of L_{EPI} change impact . . . 40
5.7 Electrostatic Discharge Simulation . . . 41

6 Calculation of Save Operating Area **44**

7 Conclusion **47**

Bibliography **49**

List of symbols, physical constants and abbreviations **51**

List of appendices **53**

A Threshold voltage dependence on geometrical parameters **54**

B BV_{DSS} and R_{DSon} dependence on L_{POV} and L_{FP} **56**

LIST OF FIGURES

1.1 LDMOS cross section [1] . . . 12
1.2 LDMOS cross section with parasitic NPN transistor [4] . . . 14
1.3 RESURF diode [5] . . . 15
1.4 RESURF diode – breakdown at the $p+/n-$ junction. [5] . . . 15
1.5 Electric field peaks for the RESURF condition [5] . . . 16
2.1 Safe operating area diagram [7] . . . 17
2.2 Various effects produced by hot carriers [9] . . . 18
2.3 Representation of RD model [12] . . . 19
2.4 Hole tunneling, capture and dissociation of Si-H bonds and subsequent diffusion of hydrogen [13] . . . 19
3.1 HBM equivalent circuit [15] . . . 21
3.2 Current waveform of HBM ESD event [15] . . . 22
3.3 MM Model scheme [15] . . . 22
3.4 Current waveform of MM ESD event [15] . . . 23
3.5 TLP pulse [15] . . . 23
3.6 Schematic of a constant/current TLP tester [15] . . . 24
3.7 I/V curve of the snapback device [15] . . . 24
4.1 Typical ESD protection with LDMOS [15] . . . 25
4.2 Typical ESD protection with high voltage diode [18] . . . 26
5.1 PLDMOS layout and simulation domain . . . 27
5.2 2D cross section . . . 28
5.3 Device structures of 45 V LDMOS . . . 28
5.4 Simulated breakdown voltage of the NLDMOS . . . 29
5.5 Simulated breakdown voltage of the PLDMOS . . . 29
5.6 Total current density under breakdown conditions . . . 30
5.7 Impact ionization under breakdown conditions . . . 30
5.8 Simulated threshold voltage of the NLDMOS . . . 31
5.9 Simulated threshold voltage of the PLDMOS . . . 31
5.10 Simulated output characteristics of the NLDMOS . . . 32
5.11 Simulated output characteristics of the PLDMOS . . . 32
5.12 Total current density in the saturation regime . . . 33
5.13 Electric field in the saturation regime . . . 33
5.14 Doping concentration across PLDMOS drain region . . . 34
5.15 Doping concentration across PLDMOS body region . . . 35
5.16 Doping concentration across the Ndrift45 and Presurf45 region for the NLDMOS . . . 35
5.17 PLDMOS geometry . . . 36
5.18 Simulation and measured data of BV_{DSS} dependence on L_{G} distance . . . 36
5.19 Simulation and measured data of R_{DSon} dependence on L_{G} distance . . . 37

5.20 Simulation and measured data of BV_{DSS} dependence on L_{STI} distance . . . 37
5.21 Simulation and measured data of R_{DSon} dependence on L_{STI} distance . . . 38
5.22 Simulation and measured data of BV_{DSS} dependence on L_{ACC} distance . . 38
5.23 Total current density under breakdown condition for different L_{ACC} 39
5.24 Impact ionization under breakdown conditions for different L_{ACC} 39
5.25 Simulation and measured data of R_{DSon} dependence on L_{ACC} distance . . . 40
5.26 Simulation and measured data of BV_{DSS} dependence on L_{EPI} distance . . . 40
5.27 Simulation and measured data of R_{DSon} dependence on L_{EPI} distance . . . 41
5.28 Simualted I/V characteristic of PLDMOS transistor for different gate voltages under ESD pulse 42
5.29 Drain voltage and Max temperature under ESD stress 42
5.30 Temperature distribution in PLDMOS after ESD stress for $V_{\mathrm{GS}} = 0$ V . . . 43
6.1 Lifetime in years of V_{T}-Extrapolated Parameter for 45 V PLDMOS transistor, $V_{\mathrm{DS}} = 0$ V 45
6.2 Percent change over use profiles 46
6.3 Automotive temperature use profile 46
A.1 Simulation and measured data of V_{T} dependence on L_{G} distance 54
A.2 Simulation and measured data of V_{T} dependence on L_{STI} distance 54
A.3 Simulation and measured data of V_{T} dependence on L_{ACC} distance 54
A.4 Simulation and measured data of V_{T} dependence on L_{EPI} distance 55
A.5 Simulation and measured data of V_{T} dependence on L_{FP} distance 55
A.6 Simulation and measured data of V_{T} dependence on L_{POV} distance 55
B.1 Simulation and measured data of BV_{DSS} dependence on L_{POV} distance . . 56
B.2 Simulation and measured data of R_{DSon} dependence on L_{POV} distance . . . 56
B.3 Simulation and measured data of BV_{DSS} dependence on L_{FP} distance . . . 56
B.4 Simulation and measured data of R_{DSon} dependence on L_{FP} distance 57

LIST OF TABLES

5.1 The properties of TLP pulse in the simulation 41
6.1 Test condition for calculation of SOA 44
6.2 Extracted parameters for 45 V PLDMOS transistor 45
7.1 Simulated and measured parameters of 45 V LDMOS devices 47
7.2 Proposed changes of geometrical parameters 48

INTRODUCTION

Many applications require a higher voltage than is the supply voltage of CMOS devices. Typical voltage ranges are $30-40$ V for display drivers, 70 V for automotive and 100 V for high voltage telecommunication. Smart Power ICs integrate power components (drivers, controllers protections, sensors) and every other circuits in the same silicon die. Smart Power ICs are composed of Bipolar Junction Transistors (Bipolar), Complimentary Metal-Oxide-Semiconductor Field-Effect Transistors (CMOS), and Double Diffused Metal Oxide Semiconductor Field-Effect Transistor (DMOS).
The power capability is achieved by using lateral or vertical DMOS transistors in the basic CMOS process. Lateral MOS (LDMOS) is mostly used as these transistors are relatively easy to integrate in CMOS process. LDMOS transistors have been developed with a structure different from conventional CMOS transistors. To reduce R_{DSon} while maintaining a high breakdown voltage and high switching speed, the reduced surface fields (RESURF) technology has been used in high voltage LDMOS transistors. On the other hand, because LDMOS transistor operate under large drain and gate voltage and higher temperature, they are prone to hot carrier degeneration and Negative Bias Temperature Instability.
This work is focused on high-voltage LDMOS transistors which are used in Smart Power Technology. In theoretical part is described the structure of these transistors and the basic electrical parameters such as breakdown voltage BV_{DSS} and resistance R_{DSon}. There is described the influence of parasitic bipolar transistor and RESURF technique which allows to achieve higher breakdown voltage. Also is described a Safe Operating Area (SOA) of transistors and effects of Hot Carrier Injection and Negative Bias Temperature Instability which affects the reliability and lifetime of MOS transistors. The work also describes the basic model to simulate ESD events such as Human Body Model (HBM), Machine Model (MM) and Transmission-Line Pulse (TLP).
The practical part deals with the simulation of the basic electrical parameters (breakdown voltage BV_{DSS}, threshold voltage V_{T} and resistance R_{DSon}) of PLDMOS and NLDMOS devices and comparing simulated concentration profiles with measured profiles by using the SIMS method.
Further, the practical part is focused on simulating changes of the basic geometric parameters such as L_{G}, L_{ACC}, L_{STI}, L_{POV}, L_{FP}, L_{EPI} for PLDMOS transistor and impact of these changes on the electrical parameters. These simulations are then compared with measured data.
The last practical part contains the simulation of ESD events using the TLP model and example of calculating Safe Operating Area.

1 LATERAL DIFFUSED MOSFET

This chapter describes the basic structure of LDMOS transistors, the basic electrical parameters, influence of the parasitic bipolar transistor and RESURF technique that allows to an increase breakdown voltage while maintaining a low resistance R_{DSon}.

1.1 Lateral Diffused NMOSFET

A typical LDMOS (Lateral Diffused MOSFET) is a four terminal device, the terminal are called Gate, Drain, Source and Body. Fig. 1.1 illustrates the schematic cross section of LDMOS structure.

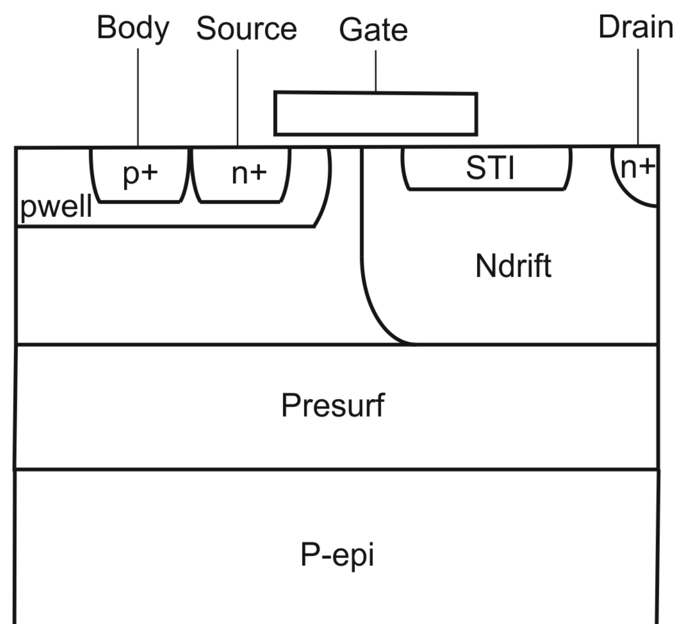


Fig. 1.1: LDMOS cross section [1]

The NLDMOS has a long, lightly doped n-type drift region between the Drain contact and the channel of the device. The n-drift region is oriented laterally referenced to silicon surface [1]. The drift region acts as a voltage variable resistor and creates a voltage drop, when the transistor is turned on. This voltage drop causes that potential in the drain region below the gate is less the applied DC bias in order to preserve the integrity of gate oxide and ensure that hot carrier injection is limited [1]. The region under the gate, bordered by source and drift region is called the channel region. An appropriate voltage at the gate terminal produces an inversion layer in channel region. The inversion layer connects the drain and source terminals by providing a conductive path between them. Charge carriers flow from source to drain through channel and drift region.
A STI (Shallow Trench Isolation) in the drift region is used to reduce risk of gate oxide breakdown at high drain voltages [2].

1.2 Current Transport

LDMOS devices behave the same as a standard MOS transistor with regard to transistor operation. The output characteristics can be characterized as have cutoff, linear and saturation regime. Current equation for the linear region can be approximated by [1]

$$I_{\mathrm{D}} = \frac{\mu_{\mathrm{s}} C_{\mathrm{ox}} W}{L} \left[\left(V_{\mathrm{GS}} - V_{\mathrm{T}} \right) V_{\mathrm{DS}} - \frac{1}{2} V_{\mathrm{DS}}^{2} \right], \tag{1.1}$$

where I_{D} is the drain current, μ_{s} is the surface mobility of charge carriers, C_{ox} is the gate oxide capacitance per unit area, W is the total gate width, L is the effective gate length, V_{GS} is the gate voltage, V_{T} is the threshold voltage and V_{DS} is the drain voltage. For small drain voltages, the V_{DS}^{2} term can be dropped from equation. For saturation region the drain current is given as [1]

$$I_{\mathrm{D}} = \frac{\mu_{\mathrm{s}} C_{\mathrm{ox}} W}{2L} \left(V_{\mathrm{GS}} - V_{\mathrm{T}} \right)^{2}. \tag{1.2}$$

Due to the graded doping profile within channel, there is an additional electric field induced drift current component which is not present in standard MOSFET [1]. Additional electric field providing an additional boost to the mobility and g_{m}.

1.3 Breakdown Voltage and R_{DSon}

BV_{DSS} is the breakdown voltage between drain and source of a LDMOS when the transistor is turned off. The drain-source breakdown in a LDMOS occurs when the electric field across the n-drain/n-source exceeds the critical value for avalanche breakdown. When p/n junction is reversed biased a depletion region extends into each side of the junction and creates a balance of charge. There are no free majority electrons (n-type) or holes (p-type) hence they are depleted of mobile carriers. Without these mobile carriers, the impurity atoms within the silicon lattice present a fixed charge. There fixed charge set an electric field across the depletion region. If is increased drain-source voltage, depletion region reveals additional fixed charge resulting in an increase of the electric field [1].
The depletion regions are continuously generated electron-hole pairs which are swept from the depletion region by the electric field resulting in the leakage currents. If the electric field exceeds a critical value, the carriers gain sufficient energy, and in the collision with the lattice atoms generate electron-hole pair [1]. These newly generated carriers repeat this process and the current increases exponentially for a sufficiently high voltage. This action is termed avalanche breakdown [1]. The breakdown voltage is dependent on the dopant level, depth and length of the n-drift region.
The output characteristics can be divided into two main regions: saturation and linear. The reciprocal of the slope of the current-voltage curve in the linear region is referred to as R_{DSon}. R_{DSon} is an important parameter of the LDMOS transistor and determines the

power density and efficiency. The specific R_{DSon} is given as

$$R_{\mathrm{DSon}} = R_{\mathrm{CH}} + R_{\mathrm{ACC}} + R_{\mathrm{D}} + R_{\mathrm{S}} + R_{\mathrm{DRIFT}}, \tag{1.3}$$

where R_{CH} is the resistance of the channel, R_{ACC} is the resistance of the overlap area between the drift region and the gate, R_{S} is the resistance of the source, R_{D} is the resistance of drain and R_{DRIFT} is the resistance of drift region. R_{DRIFT} is the largest resistance because it is lightly doping due to higher breakdown voltage.

1.4 Parasitic Bipolar Transistor

LDMOS structure with parasitic bipolar transistor is shown in fig. 1.2. The emitter is the $n+$ source, the base is the body of the structure and the collector is the drain. If the impact ionization is initiated and avalanche breakdown occurs, there is an increased concentration of electrons and holes in the drain [3]. The built-in electric field pushes electrons out of the drain region, and holes are injected into the base of parasitic bipolar transistor. The potential of the body is increased in the source due to intrinsic body resistance. When the body potential exceed the threshold to open source-body junction, more electrons are injected across the channel and into the high field drain region which creates more holes and electrons due to avalanching [1]. This further increases the forward biasing of the body-source junction and arises positive feedback which leads to the junction breakdown.

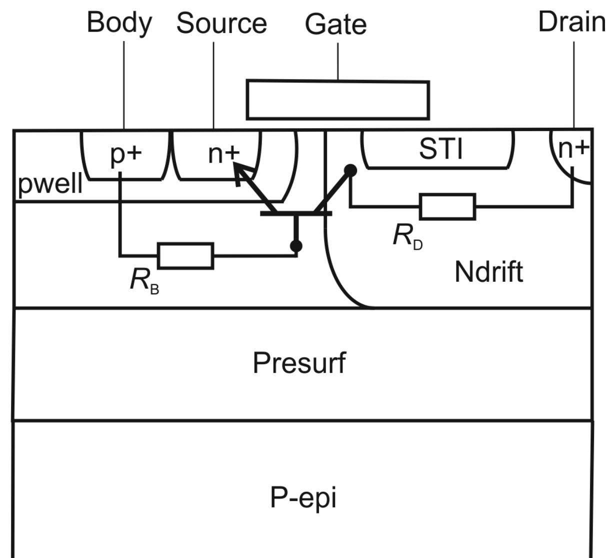


Fig. 1.2: LDMOS cross section with parasitic NPN transistor [4]

Parasitic resistor R_{B} reduces triggering voltage V_{t1} and increases discharge current I_{t2} of the device [4]. Increasing resistivity of R_{B} can be achieved by increasing the Body to Source contact space. Parasitic resistor R_{D} effective improves second breakdown current I_{t2} of the device [4]. R_{D} increase in resistance can be achieved by increasing the

Gate to Drain contact space or by increasing the resistivity of the path current flowing through.

1.5 Reduced Surface Fields Principle

RESURF (REduced SURface Fields) technique is based on a rapid two dimensional expansion in the deplete region width with increasing drain bias that keeps the peak electric field below critical field for impact ionization [1]. This technique allows to achieve very high values of breakdown voltages while maintaining the low R_{DSon}. Fig. 1.3 shows the structure of a RESURF diode which consists of a lateral $p+/n-$ diode and vertical $p-/n-$ diode.

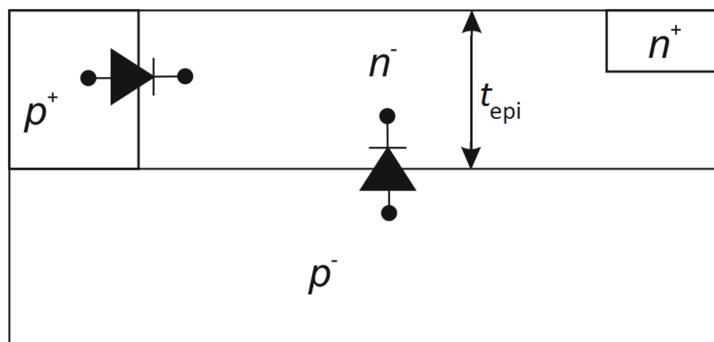


Fig. 1.3: RESURF diode [5]

If not used RESURF technique, junction breakdown occurs at the $p+/n-$ junction, as is shown in fig. 1.4. In the $p+$ region the depletion region cannot penetrate, resulting into a high electric field for low voltages.

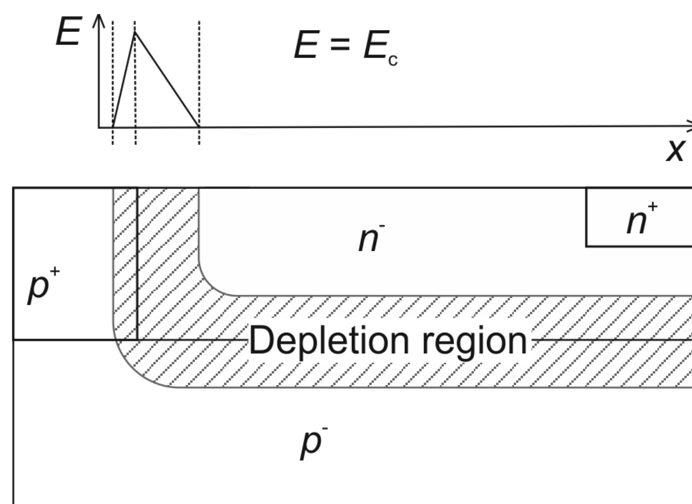


Fig. 1.4: RESURF diode – breakdown at the $p+/n-$ junction. [5]

Using the RESURF technique, the doping density of the $n-$ region and its thickness

is adjusted so that the depletion region of vertical diode reaches the surface before the breakdown limit of the lateral diode appears [5]. This results in a redistribution of the electric field and reducing the maximum electric field below the critical level, as shown in fig. 1.5.

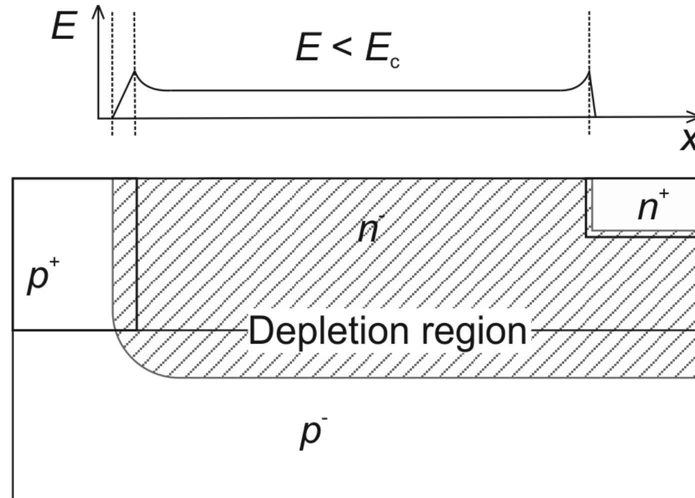


Fig. 1.5: Electric field peaks for the RESURF condition [5]

The maximum electric field appears at the $p+/n-$ junction and at the edge of $n+$ region. RESURF condition is dependent on the doping concentration N_{epi} and the thickness t_{epi} of $n-$ layer. An approximate net charge Q_{n} of $n-$ layer is given by [6]

$$Q_{\mathrm{n}} = N_{\mathrm{epi}} \cdot t_{\mathrm{epi}}. \tag{1.4}$$

The breakdown voltage depends on the net charge Q_{n} of the $n-$ layer. The optimum Q_n is found by assuming that the vertical depletion must reach the surface before the lateral junction breaks down. The breakdown voltage is also influenced by concentration of the substrate N_{sub} and the distance between $n+$ and $p+$ (drift region) [5].

2 SAFE OPERATING AREA

This chapter describes the construction of Safe Operating Area for MOS transistors, Hot Carrier Injection and Negative Bias Temperature Instability. These two phenomena adversely affect electrical parameters of MOS transistors and reduce their lifetime.

2.1 Electrical Safe Operating Area

SOA curves define the maximum of drain-source voltage and drain current that guarantees safe operation. Typical characteristic of the SOA has four borders as shown in fig. 2.1.

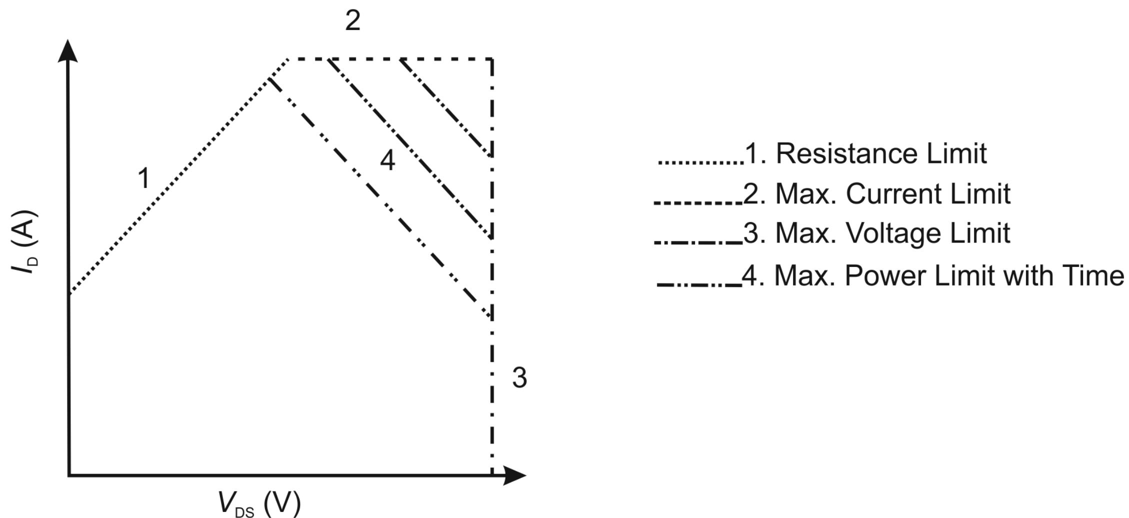


Fig. 2.1: Safe operating area diagram [7]

1. R_{DSon} limit-line - gives a linear dependency between V_{DS} and I_{D}. The slope of the line is simply the maximum R_{DSon} of the MOSFET.
2. Maximum current line - the maximum allowable current the part can tolerate.
3. Maximum power limit-line - maximum allowable power in the part caused by normal switching mode operation and heat.
4. Breakdown voltage limit-line - on the right hand-side the limit of the SOA is given by the generally the breakdown voltage.

Parallel lines in area 4 (fig. 2.1) are the maximum drain-source current for different pulse width, these currents are determined by the transient thermal impedance [7].

2.2 Hot Carrier Injection

Hot carrier damage is one of the important degradation mechanisms for MOSFETs [8]. Hot carriers are particles that attain very high kinetic energy gained by an electric field.

These energetic carriers can be injected into the oxide to become oxide trapped charge; they can drift through the oxide and causing gate current [9]. These effects lead to a shift of the parameters of components (threshold voltage, transconductance, R_{DSon}). HCI degradation is more evident in NMOS transistors due to the higher mobility of the majority charge carriers. The various effects of hot carriers produced are shown in fig. 2.2.

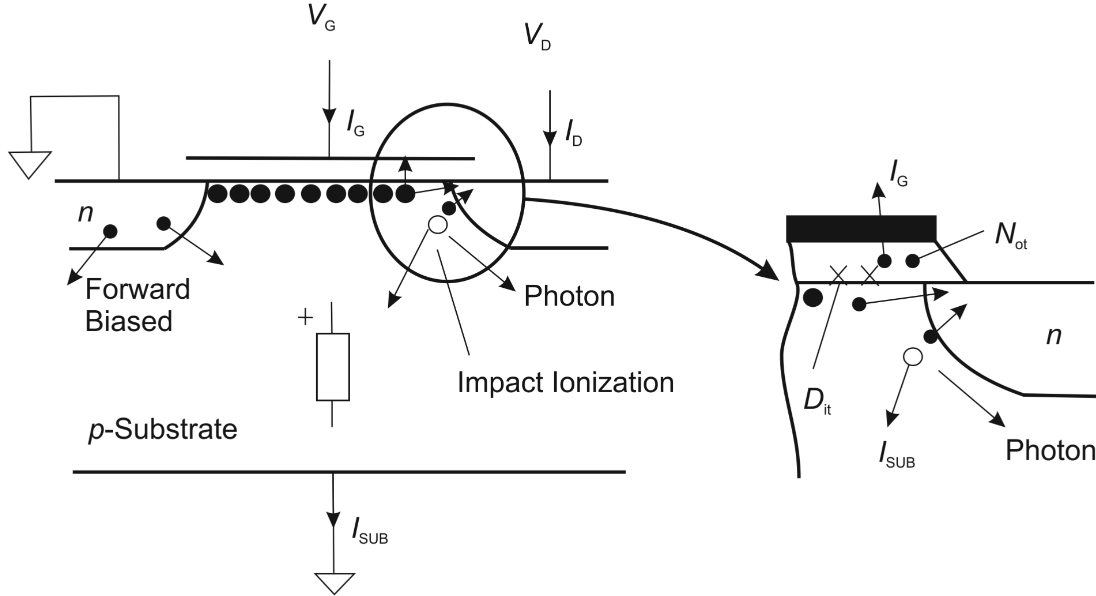


Fig. 2.2: Various effects produced by hot carriers [9]

The carriers gain their energy due to a high electric field in the drain region. These particles in the drain cause impact ionization. The generated hot carriers can be injected into the oxide (N_{ot}), can flow through the oxide (I_{G}), can generate interface traps (N_{it}), can cause substrate current (I_{SUB}), and generate photons [9]. Interface traps and carriers injected into the oxide to cause degradation of the threshold voltage, mobility and R_{DSon}. Generated photons can propagate in the device, can be absorbed and generate new electron-hole pair. Substrate current produces a voltage drop in the substrate which turns on parasitic BJT transistor, as described in Section 1.4.
Degradation induced by the HCI can be described by [10]

$$\Delta V_{\mathrm{t}} = At^{n}, \tag{2.1}$$

where ΔV_{t} is the shift of the threshold voltage, A is the material dependent parameter, t is the stress time and n is the empirically determined exponent, a function of stress voltage, temperature, and effective transistor channel length.
The time to failure is for NMOS transistor given by [10]

$$TTF = B\left(I_{\mathrm{G}}\right)^{-M} \mathrm{e}^{\frac{E_{\mathrm{AA}}}{\mathrm{k}T}}, \tag{2.2}$$

where B is the arbitrary scale factor (strong function of proprietary factors, such as doping profiles, sidewall spacing dimensions), I_{G} is the peak gate current during stressing,

$M = 2-4$, E_{AA} is the apparent activation energy (−0,2 to +0,4 eV), k is the Boltzmann's constant and T is the temperature in kelvins.

2.3 Negative Bias Temperature Instability

One of the most important reliability issue of modern unipolar technology is Negative Bias Temperature Instability (NBTI) degradation [11]. One of the most prevalent models proposed to explain NBTI mechanism is the Reaction-Diffusion (R-D) model [12] as shown in fig 2.3.

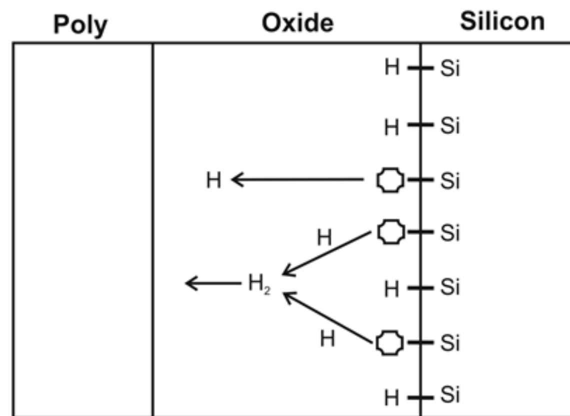


Fig. 2.3: Representation of RD model [12]

This model explains the physics of the degeneracy of the PMOS device, within terms of different sub-processes including the bond breaking process and generation of interface traps. The fig. 2.4 shows the breaking of hydrogen bonds silicon (Si-H) at the $Si-SiO_2$ interface which occurs when the negative gate voltage is applied.

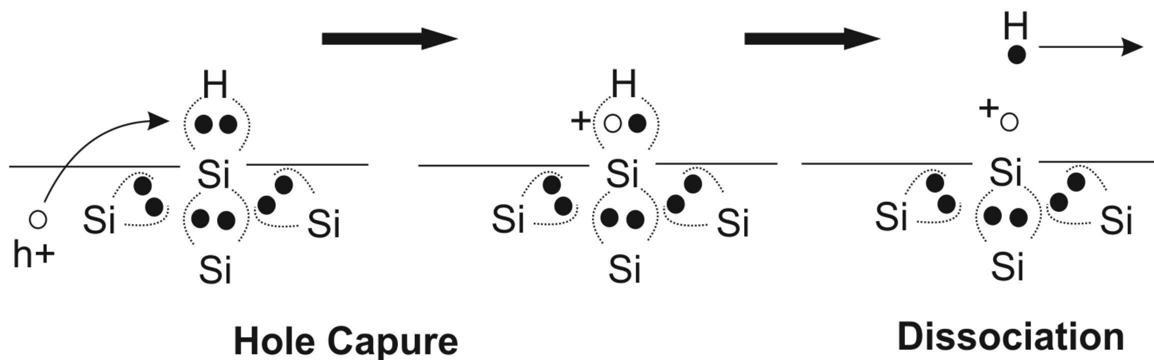


Fig. 2.4: Hole tunneling, capture and dissociation of Si-H bonds and subsequent diffusion of hydrogen [13]

The broken bond silicon (Si−) acts as interface traps that are responsible for higher threshold voltage and lower current drain. The generation of the interface traps is caused

by the dissociation of Si−H bonds in the Si−SiO_2 interface and subsequent diffusion of released hydrogen species away from the interface which leaves interface traps [13]. Holes from the inverse layer tunnel into the oxide and interact with Si−H bonds. The holes get captured and take away one electron from the Si−H bonds. The weakened Si−H bonds are then broken by thermal excitation [14]. The released hydrogen species either diffuse away from the Si−SiO_2 interface and leave behind Si− or react back with Si− and form Si−H. The H atoms released from the Si−H bonds can contribute to three sub-processes [13]:

- diffusion toward the gate,
- connection to another H atom to produce H_2,
- recovery of the broken bonds.

NBTI is usually observed only in PMOS devices and it seems that it is negligible for NMOS because interface traps can cause a positive or negative charge at the interface. Interface traps easy exchange charge (electrons or holes) with the substrate and introduce a positive or negative charge at the interface [13]. The net charge in interface traps in NMOS device is negative (positive gate voltage) and positive in PMOS device (negative voltage on the gate). The charge trapped in traps in the oxide is in NMOS and PMOS transistors mostly positive. Oxide charge can consist of various entities (mobile charge, oxide trapped charge and fixed charge), but oxide charge is not well understood [12]. Interface charge and oxide charge is positive charge for PMOS and negligible for NMOS. There are types of NBTI stress, it can be DC or AC stress. After removing the NBTI stress a fraction of interface traps self-anneal, leading to a partial removal of the threshold voltage shift [13]. The removal of the threshold voltage shift can be observed when the device is stressed pulsed waveforms, these conditions are called AC test. For DC stress, when the device is permanently stressed, the degradation rate is lower compared with AC stress [13]. The rate of degradation in AC stress conditions depends on the duty cycle of the applied signal.

To measure the effect of NBTI used the following configuration: source, drain and substrate are grounded, while the gate is negatively biased. Temperature range for the test is between 100°C and 200°C. Evaluates the shift of the threshold voltage after the test [10]

$$\Delta V_{\mathrm{t}} = A_0 \mathrm{e}^{\frac{E_{\mathrm{AA}}}{\mathrm{k}T}} \mathrm{e}^{\beta V_{\mathrm{GS}}} \mathrm{e}^{\gamma V_{\mathrm{DS}}} t^n \tag{2.3}$$

where ΔV_{t} is the shift of the threshold voltage, A_0 is the pre-factor dependent on the gate oxide process, E_{AA} is the apparent activation energy (eV), k is the Boltzmann's constant, T is the application channel temperature (K), V_{GS} is the application gate voltage, β is the measured gate voltage sensitivity, γ is the measured drain voltage sensitivity, V_{GS} is the application drain voltage and n is the measured time exponent.

3 ELECTROSTATIC DISCHARGE

When a charged object gets close to another object with different electrostatic potentials, charge transfer occurs. This process is called electrostatic discharge - ESD. When a charged person touches with a grounded circuit, current can reach values on the order of amperes for tens of nanoseconds. There are many ESD test models for describing the stress under actual working conditions.

3.1 Human Body Model

To determine the effectiveness of the protection circuit in an integrated circuit is primarily used HBM testing. This HBM pulse is intended to simulate the human body contact with the device which can occur during normal usage. The HBM is today the most widely used model in the microelectronics industry [15]. HBM attempts to simulate what happens when a pre-charged person begins to discharge by touching a conductive component lead. The equivalent HBM circuit includes the resistor (R = 1500 Ω), the capacitor (C = 100 pF), the serial inductor (L_S = 8 μH) and the parasitic capacitance of the resistor (C_S = 1.5 pF). The equivalent RLC circuit of HBM with parasitic elements is shown in fig. 3.1.

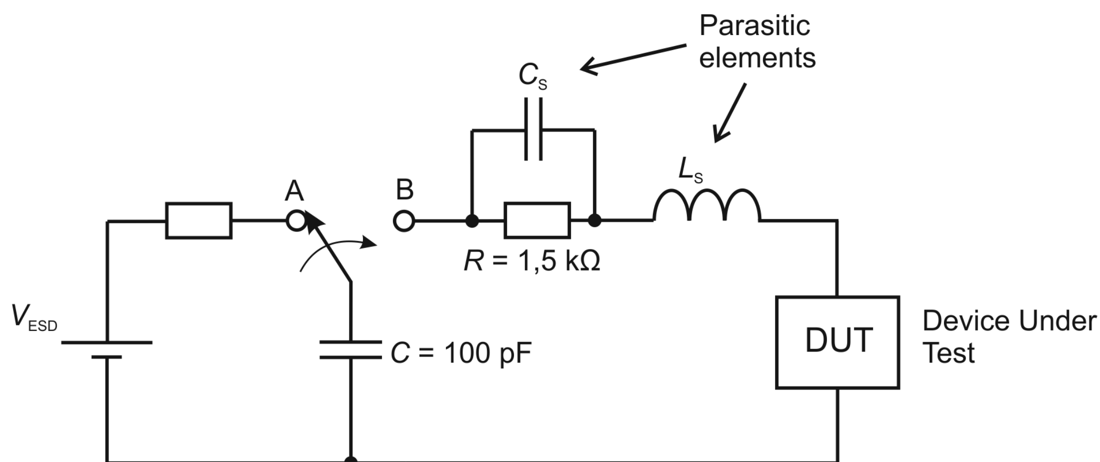


Fig. 3.1: HBM equivalent circuit [15]

ESD event can be simulated as a current source with the current waveform shown in the fig. 3.2 due to the large series resistance in the HBM model. The current peak is typically $1,2 - 1,48$ A for 2 kV HBM ESD stress, the rise time is $2 - 10$ ns and the decay time is $130 - 170$ ns [15]. Capacitance and resistance can be in real conditions differ from the values of the model. As a result, the real ESD waveform can be different from the HMB model.

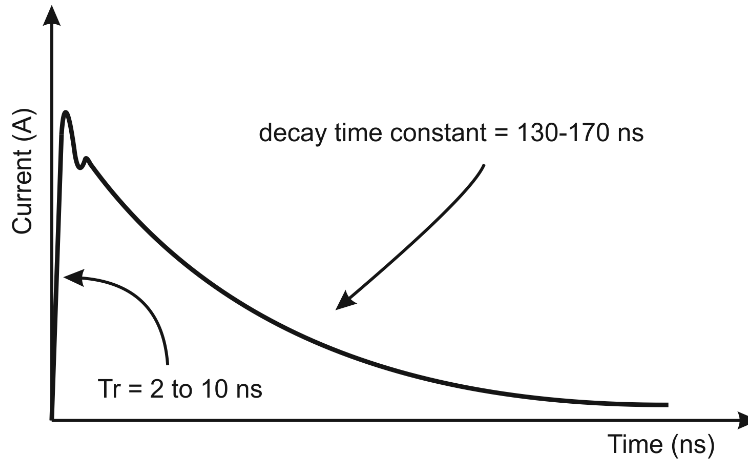


Fig. 3.2: Current waveform of HBM ESD event [15]

3.2 Machine Model

The Machine Model (MM) is similar to the Human Body Model and equivalent circuit includes the resistor ($R = 1500\ \Omega$), the inductor ($L_S = 750$ nH) and the capacitance ($C = 200$ pF) as shown in 3.3.

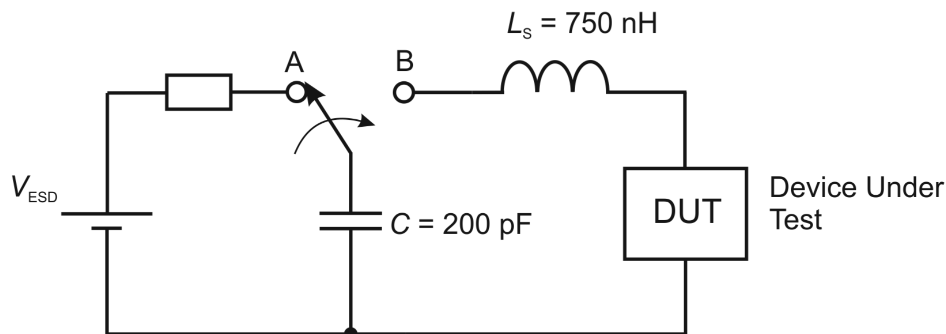


Fig. 3.3: MM Model scheme [15]

This model is intended to simulate ESD events that can occur in the industry. Lower impedance and higher capacity leads to much higher current density during MM discharge. Typical voltage values for MM model are from 100 V to 500 V [15]. An important parameter is the inductance value which controls the rise time of the current waveform. MM can be modeled as a voltage source because series resistance is very low. The comparison of HBM and MM current waveforms are shown in fig. 3.4. In real conditions the main problem is with non-zero resistance tester.

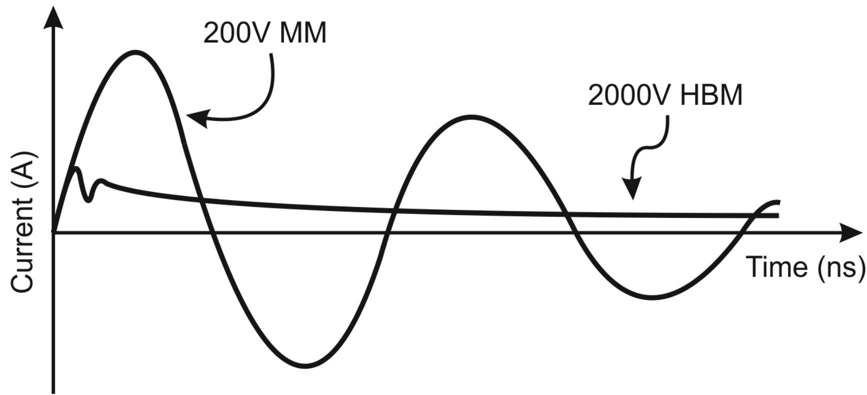


Fig. 3.4: Current waveform of MM ESD event [15]

3.3 Transmission-line Pulse Testing

TLP uses a rectangular test pulse or a square test pulse to simulate ESD events. A typical value of the rise time is $2 - 10$ ns and typical pulse width is 100 ns [15]. The rise time is similar as in the HBM model because different rise time can cause differences in device failure. The typical current waveform for TLP and HBM model is shown in fig. 3.5. TLP waveform does not represent any real ESD event, it is only a tool used by designers to analyse ESD protection circuit.

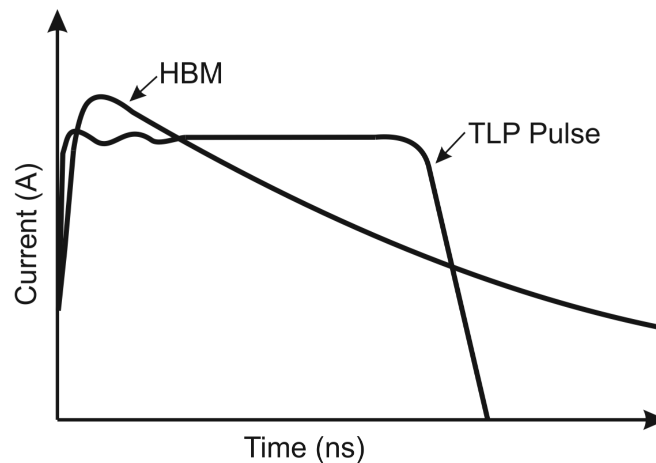


Fig. 3.5: TLP pulse [15]

To create a TLP waveform is used a high-voltage source with the transmission line. Schematic of a constant-current TLP tester is shown in fig. 3.6. A 50 Ω resistor provides a known load for transmission line. Resistor in series with the DUT converts the voltage from the transmission line to a constant current which is injected into the DUT. This type of TLP tester can produce a current of 10 A [15].
A TLP tester must built an I-V curve through numerous sets of measurements. This curve represents measurements of voltage across the device and the current through the

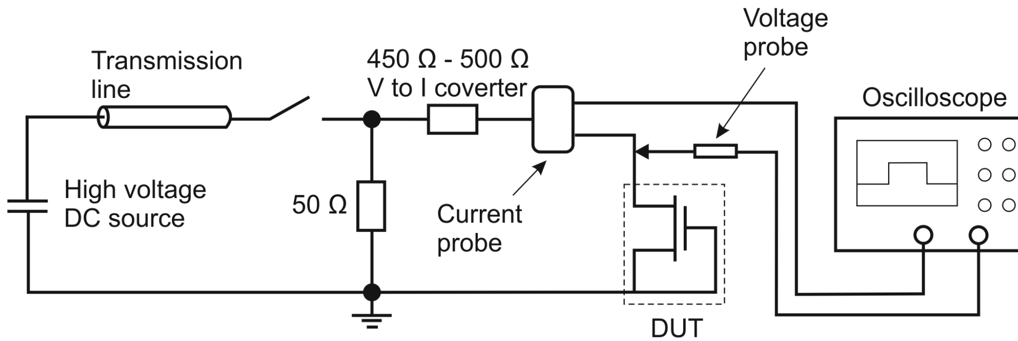


Fig. 3.6: Schematic of a constant/current TLP tester [15]

device by averaging data for same length time. For each point on the curve TLP tester applies a pulse to a device that is not powered.

3.4 Snapback Devices

The typical current-voltage characteristic of this type of protection is shown in fig. 3.7.

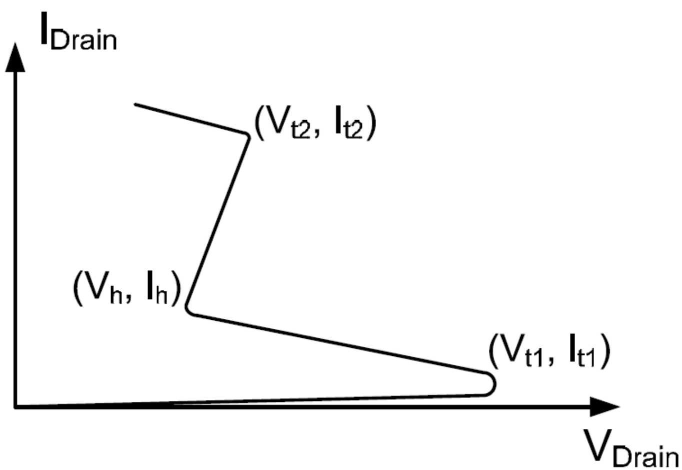


Fig. 3.7: I/V curve of the snapback device [15]

Protection closes on threshold voltage V_{t1}. Then moves to the negative differential resistance with a holding voltage V_h. At the same time creates a low resistance discharge channel which removes ESD current. The holding voltage must provide appropriate voltage drop to minimize power dissipation. This is a big advantage over protections with a simple current-voltage characteristic where is larger power dissipation. The holding voltage should not be lower than the operating voltage of the circuit. At higher currents occurs thermal breakdown illustrated by V_{t2} voltage, this value determines the level of ESD protection.

4 APPLICATION OF HIGH VOLTAGE DEVICES

This chapter describes application of high-voltage devices as Lateral Diffused MOS transistor, bipolar transistor and high-voltage diode in Smart Power Technology.

4.1 Lateral Diffused MOSFET

Lateral diffused MOS transistors are commonly used as output driver in the Smart Power Technologies. When compared with the bipolar transistor had LDMOS many advantageous as high-input impedance, easy to paralleling, higher gain, thermal stability (negative temperature coefficient) and high switching speed [16]. LDMOS transistor is often used as switch in switching power supply circuits, display drivers, communication circuits, DC a DC transform, fast switch transform, audio amplification, analog switches, high-speed core driver, motor control, automotive electronics, energy efficient lighting, induction heating, RF communications and other fields. LDMOS is also used as ESD protection circuit. Typical ESD protection with LDMOS is shown in fig. 4.1.

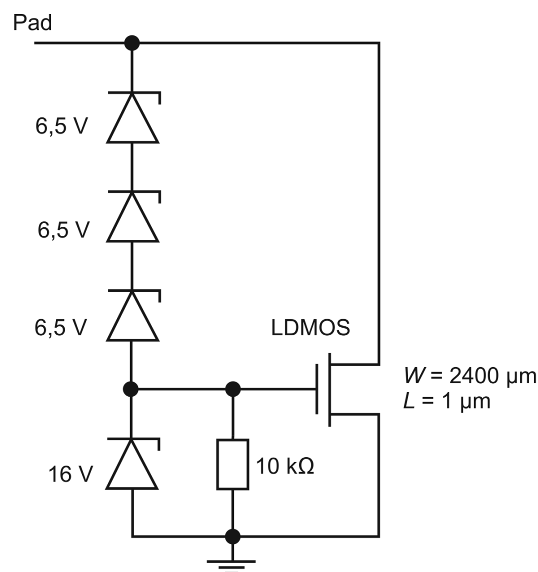


Fig. 4.1: Typical ESD protection with LDMOS [15]

LDMOS transistor is triggered by string of Zener diodes. Zener clamp is used to prevent the launch of parasitic bipolar transistor when ESD pulse appears at Drain electrode of LDMOS transistor. Under ESD pulse, LDMOS operates as a saturated MOSFET and a lower drain clamp voltage should result in better ESD performance. To improve ESD properties of this protection can be inserted a 10 kΩ resistor between the gate of LDMOS transistor and ground [15].

4.2 Bipolar Transistor

Bipolar transistor is commonly used in band gap reference. Band gap structures are used to generate temperature independent reference voltage in Smart Power Technology. Voltage reference has been used in many application as LDO regulator, comparator, D/A and A/D converters and RF circuits [17]. The principle to achieve temperature independent voltage is that the thermal voltage V_{Th} with a positive temperature coefficient compensates the voltage of emitter-base junction V_{BE} which has a negative temperature coefficient. Bipolar transistor is used in a band gap reference because it has a wide range of conditions and manufacturing processes where is temperature coefficient approximately constant $-2\ \mathrm{mVK}^{-1}$.
Bipolar transistor is also used in other applications as current mirrors, amplifiers, active loads and cascodes.

4.3 High Voltage Diode

High voltage diodes are used for general use and also are used as ESD protection. Typical static ESD protection circuit with double diodes for a pad is shown in Fig. 4.2.

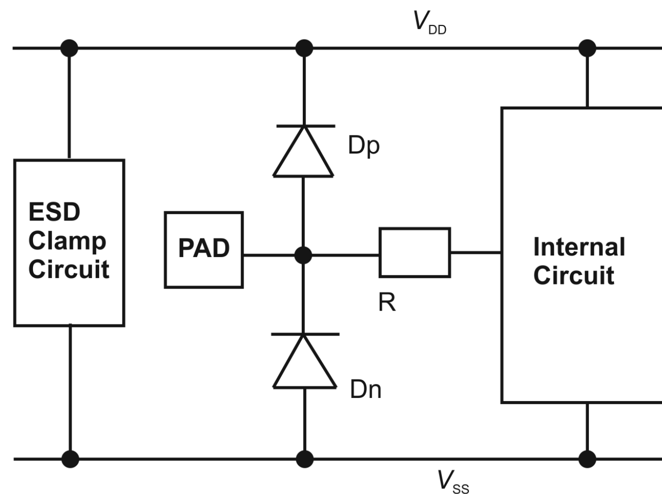


Fig. 4.2: Typical ESD protection with high voltage diode [18]

Protection is triggered when diodes are reverse biased during ESD events. Diode $\mathrm{D_n}$ is therefore triggered for ESD event which is positive to V_{SS} supply and diode $\mathrm{D_p}$ is triggered for ESD stress which is negative to V_{DD} supply [18].

5 TCAD SIMULATION

This section describes the simulation results of LDMOS devices in TCAD simulation program. Simulation of changes in geometrical parameters were calculated in SPROCESS program that simulates the complete manufacturing process of the device. Electrical parameters of devices were obtained using the program SDEVICE.

5.1 Device structure

The structure of components is simulated using the SPROCESS and electrical tests are simulated using sDEVICE. PLDMOS layout and simulation domain is shown in fig. 5.1.

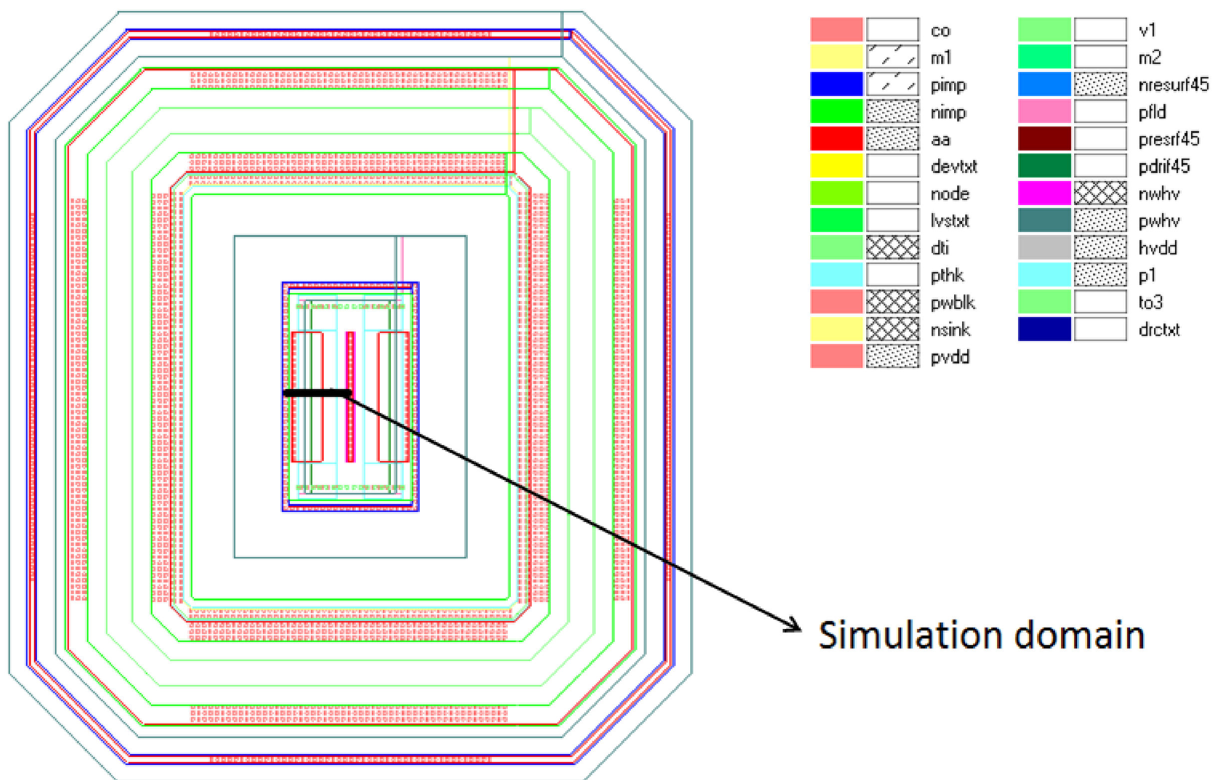


Fig. 5.1: PLDMOS layout and simulation domain

The 2D device structures of 45 V p-type LDMOS device is illustrated in fig. 5.2. The cross-section consists of the $P{+}{+}$ substrate, n-type epitaxial layer with NBL layer and p-type epitaxial layer in which the device is created. Detailed views of the created devices are shown in fig. 5.3. PLDMOS device consists of Pdrift45, Nresurf45, and Nwell layers, and NLDMOS device consists of Ndrift45, Presurf45 and Pwell layers.

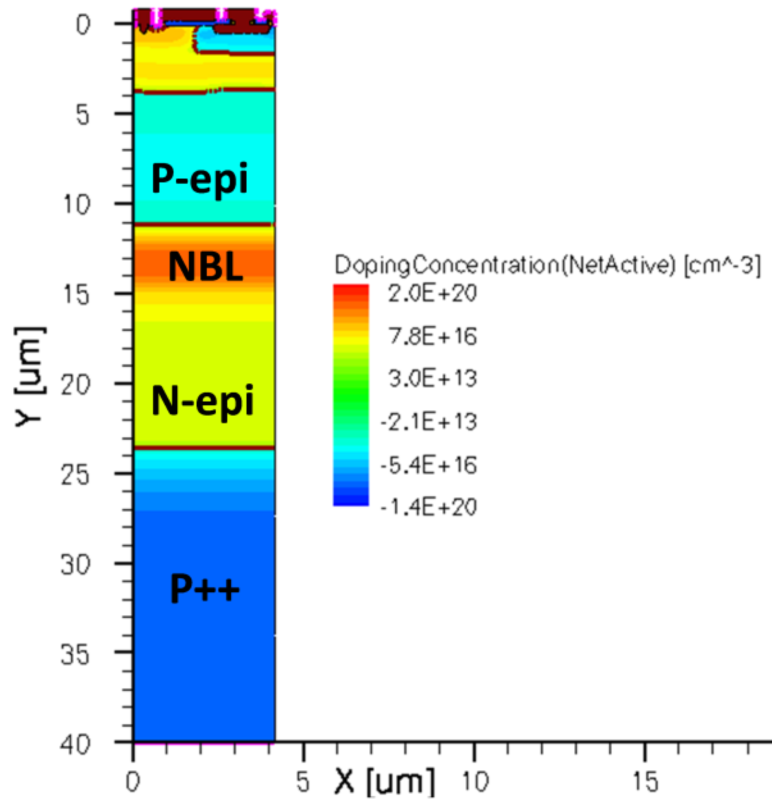
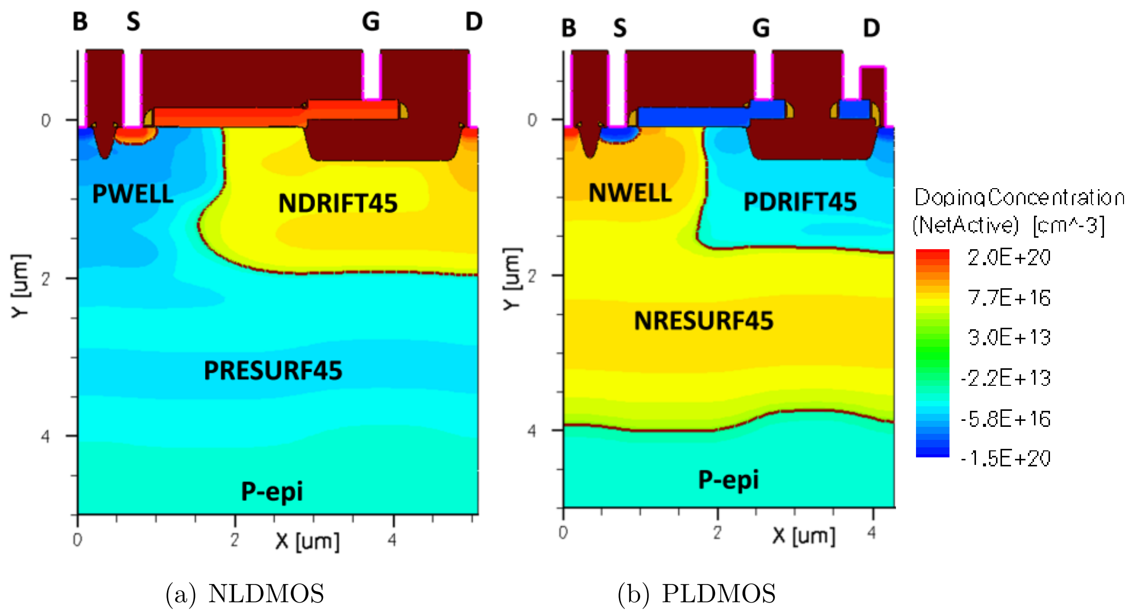


Fig. 5.2: 2D cross section



(a) NLDMOS (b) PLDMOS

Fig. 5.3: Device structures of 45 V LDMOS

5.2 Breakdown voltage

The breakdown voltage of the devices is simulated using SDEVICE. With the gate turned off, the drain voltage is ramped up until breakdown occurs. The breakdown characteristics are plotted in fig. 5.4 and fig. 5.5, $BV_{\mathrm{DSS}} = 61$ V for the NLDMOS and $BV_{\mathrm{DSS}} = -58,3$ V for the PLDMOS. The current limit is set to 1 nA. The measured breakdown voltage is 58 V for the NLDMOS and -58 V for the PLDMOS. Measured and simulated values of breakdown voltage are in good agreement.

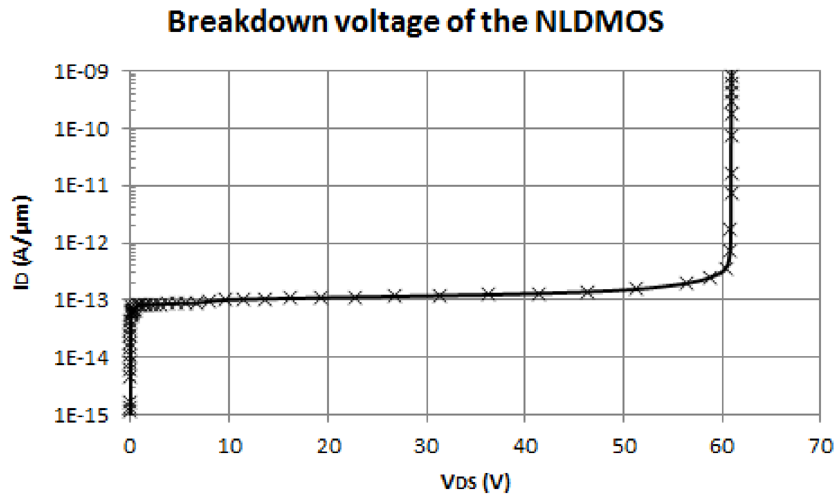


Fig. 5.4: Simulated breakdown voltage of the NLDMOS

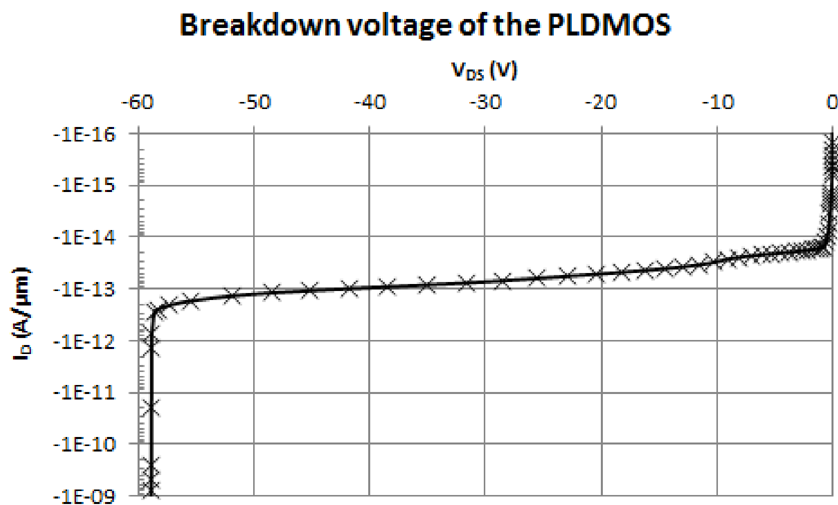
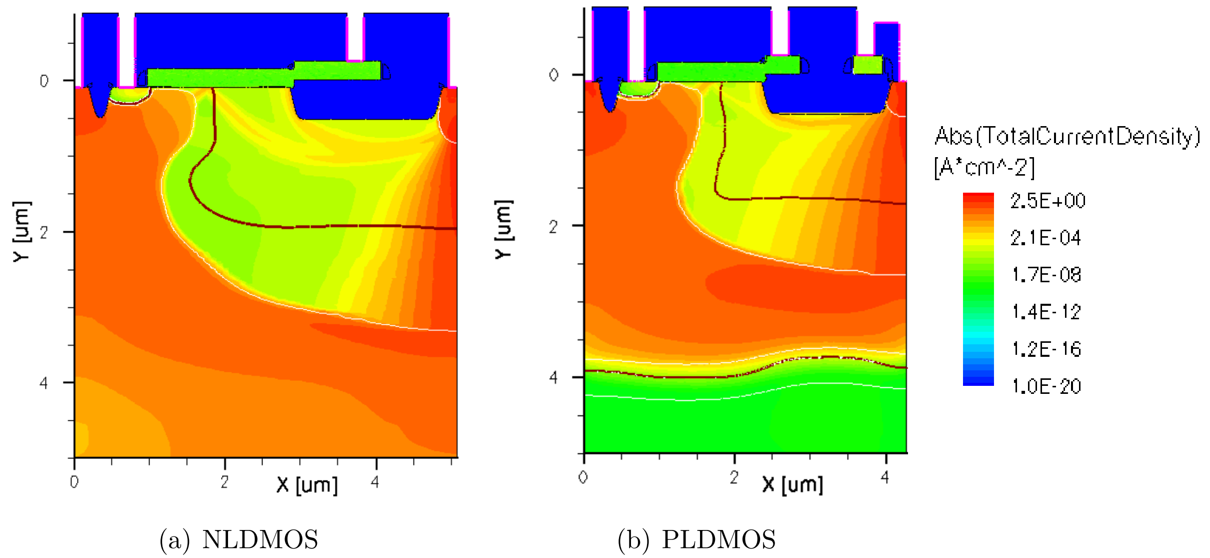


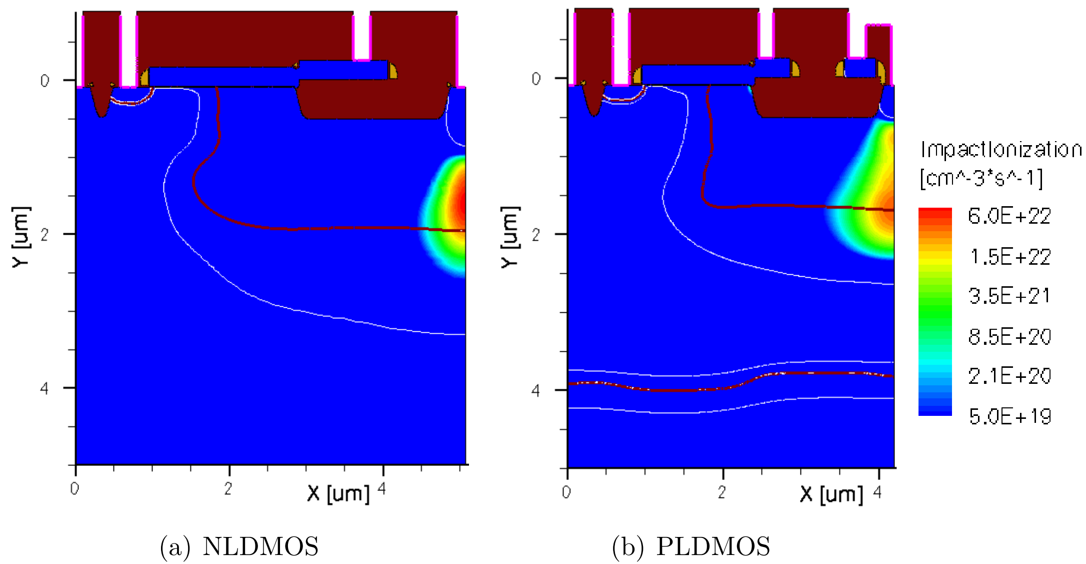
Fig. 5.5: Simulated breakdown voltage of the PLDMOS

Fig. 5.6 shows the current flow under breakdown conditions and fig. 5.7 shows the distribution of impact ionization under breakdown conditions.



(a) NLDMOS (b) PLDMOS

Fig. 5.6: Total current density under breakdown conditions



(a) NLDMOS (b) PLDMOS

Fig. 5.7: Impact ionization under breakdown conditions

The breakdown of the complementary LDMOS occurs at the bottom of the drift region at the Drain contact. Also, punch through of the channel does not occur in this design.

5.3 Threshold voltage

The threshold voltage is extracted by setting the drain voltage to 0,1 V and then the gate voltage is ramped up until conduction current is observed. The threshold voltage is extrapolated from I_D - V_G curve at point of maximum g_m. From this value is subsequently subtracted term $\frac{1}{2}V_{DS}$. Fig. 5.8 shows the threshold voltage for the NLDMOS device and fig. 5.9 shows the threshold voltage for the NLDMOS device.

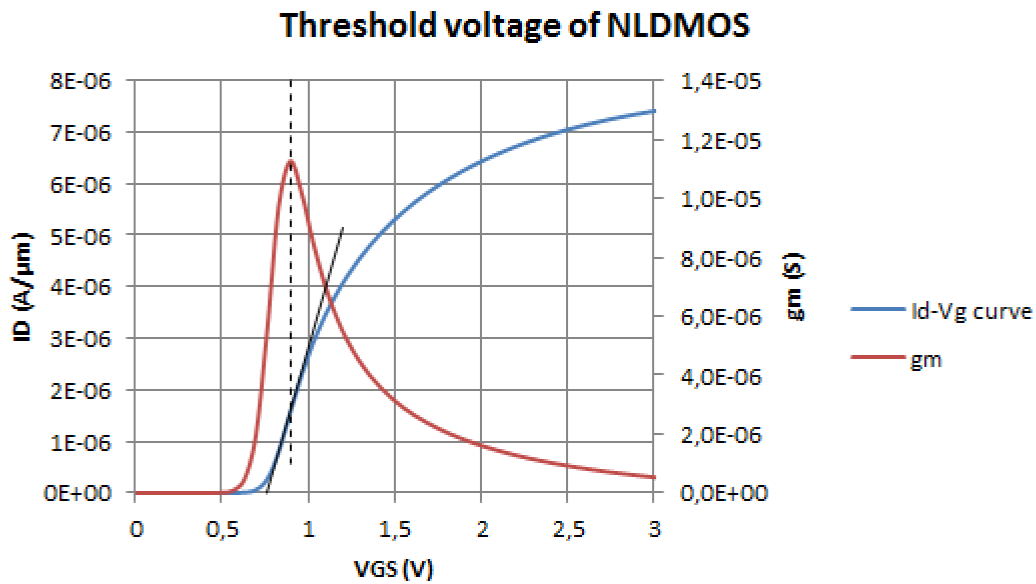


Fig. 5.8: Simulated threshold voltage of the NLDMOS

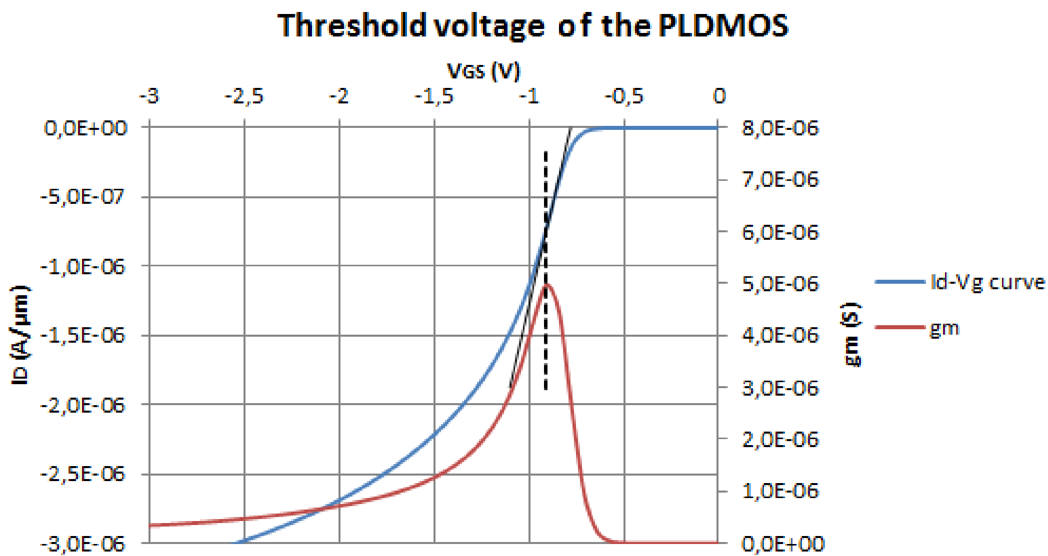


Fig. 5.9: Simulated threshold voltage of the PLDMOS

The threshold voltage is $V_T = 0,76$ V for the NLDMOS device and $V_T = -0,78$ V for

the PLDMOS device. The measured threshold voltage is 0,77 V for the NLDMOS and -0,75 V for the PLDMOS. Measured and simulated values of threshold voltage are in good agreement for both PLD and NLD device.

5.4 Saturation regime and R_{DSon}

The output characteristics of the NLDMOS and PLDMOS devices were simulated with different gate voltages and are illustrated in fig. 5.10 and fig. 5.11. The maximum gate voltages are 3,3 V for the NLDMOS and -3,3 V for the PLDMOS.

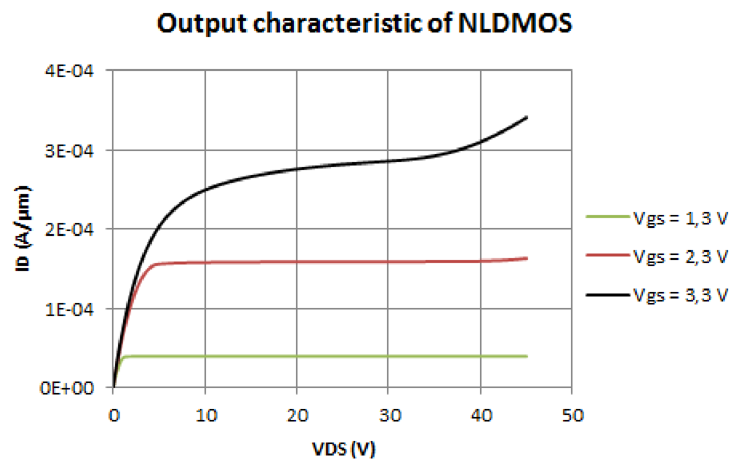


Fig. 5.10: Simulated output characteristics of the NLDMOS

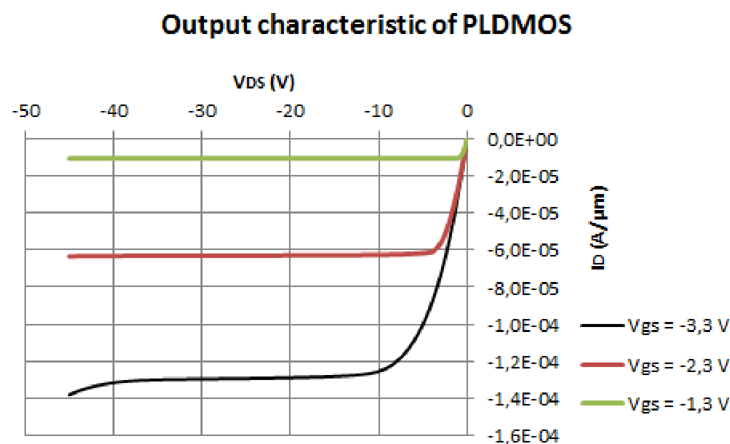
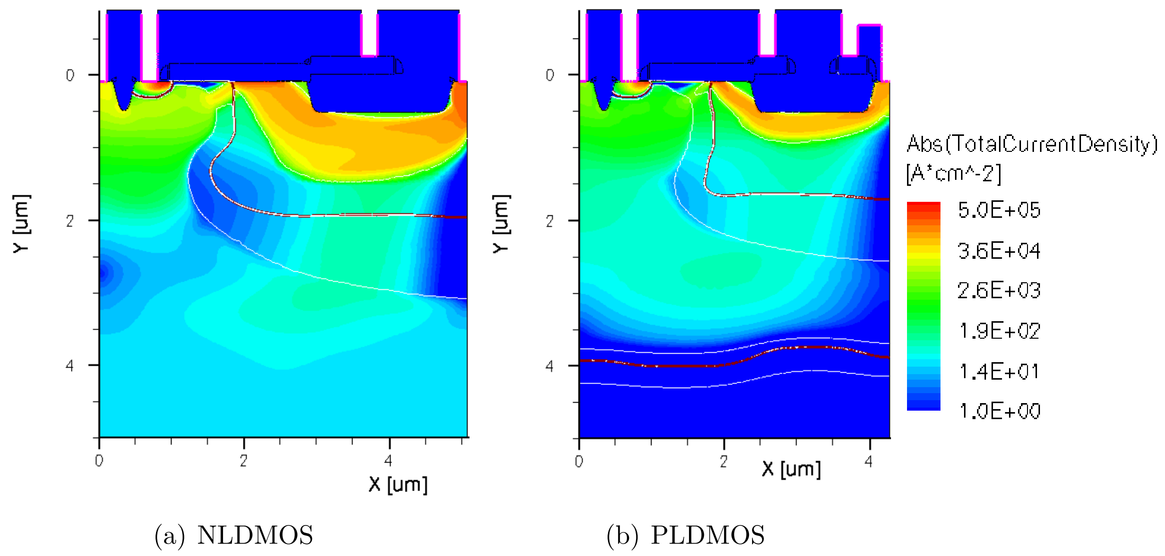


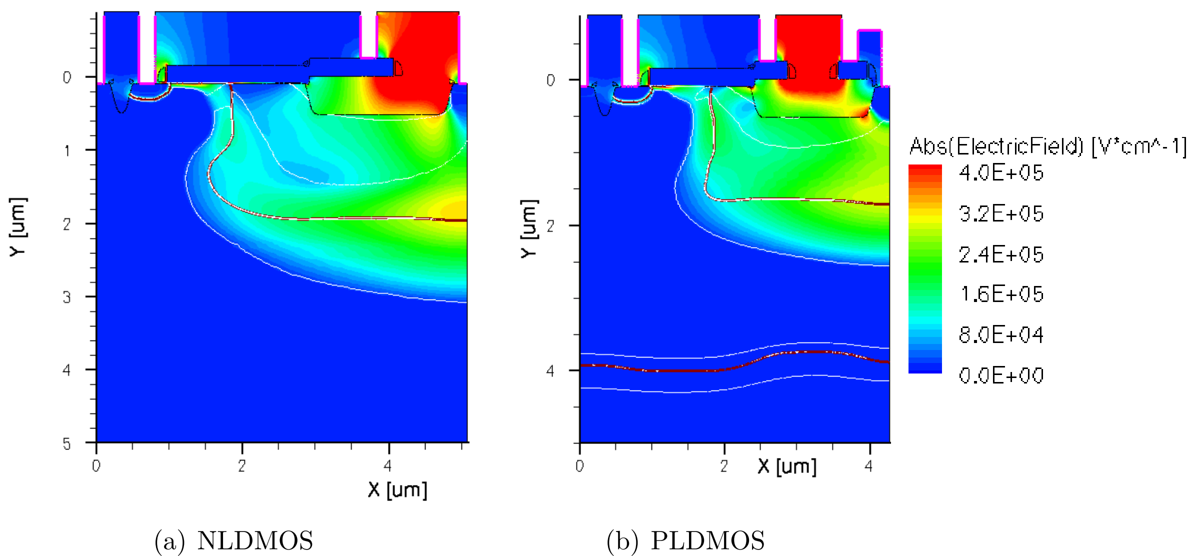
Fig. 5.11: Simulated output characteristics of the PLDMOS

Fig. 5.12 shows the current flow in the saturation regime and fig. 5.13 shows the distribution of the electric field in the structure.
The current flows from the drain contact through the drift region and the channel to the



(a) NLDMOS (b) PLDMOS

Fig. 5.12: Total current density in the saturation regime



(a) NLDMOS (b) PLDMOS

Fig. 5.13: Electric field in the saturation regime

source contact. Part of the current also flows into the body contact, typically about 5 % of the total current. The maximum electric field in the saturation regime is at the corner of STI isolation at the drain contact.
R_{on} can be extracted from the output characteristics for the maximum gate voltage in the linear regime.
R_{DSon} is given by

$$R_{\text{DSon}} = R_{\text{on}} N_{\text{g}} W L_{\text{hp}} 10^{-3} \tag{5.1}$$

where R_{on} is the measured on-state resistance (Ω), N_{g} is the number of gate polysilicon strips specified for the device layout, W is the gate width specified for the device layout (μm) and L_{hp} is the distance between center line of a body contact and the center line of the nearest drain contact (μm) and the unit of R_{DSon} is mΩ mm^2.
Simulated on-resistance is 56,9 mΩ mm^2 for the NLDMOS and 135 mΩ mm^2 for the PLDMOS. The measured R_{DSon} is 49 mΩ mm^2 for the NLDMOS and 132,1 mΩ mm^2 for the PLDMOS. Measured and simulated values are in good agreement.

5.5 Concentration profile

This section deals with the comparison of simulated concentration profiles and profiles measured by SIMS (Secondary Ion Mass Spectrometry). Doping concentration across PLDMOS drain region is shown in fig. 5.14.

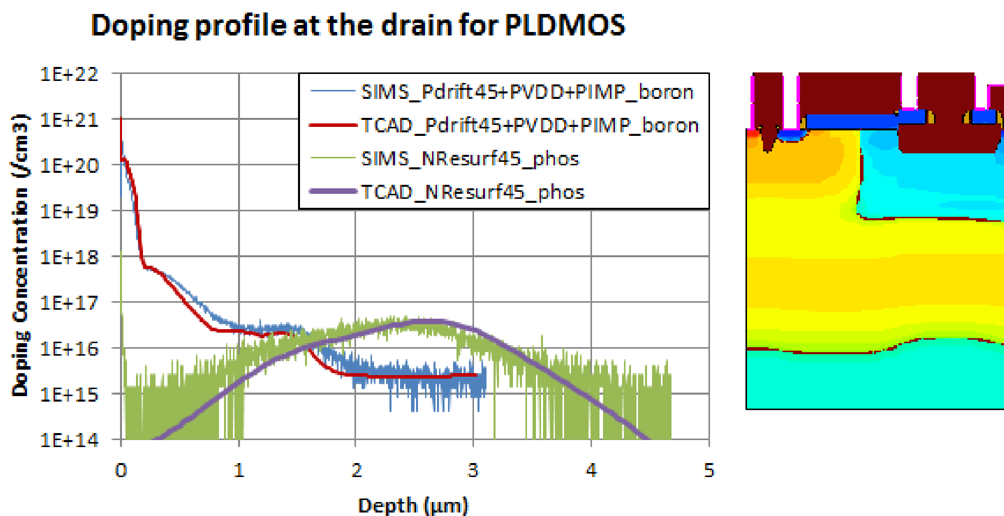


Fig. 5.14: Doping concentration across PLDMOS drain region

PVDD and Pdrift45 layers are shifted about 0, 18 μm to lower depth, PIMP layer accurately reproduces the measured profile and Nresurf45 layer is slightly shifted to greater depth. The doping concentration of each layer is consistent with measured data.
Doping concentration across PLDMOS body region is shown in fig. 5.15.

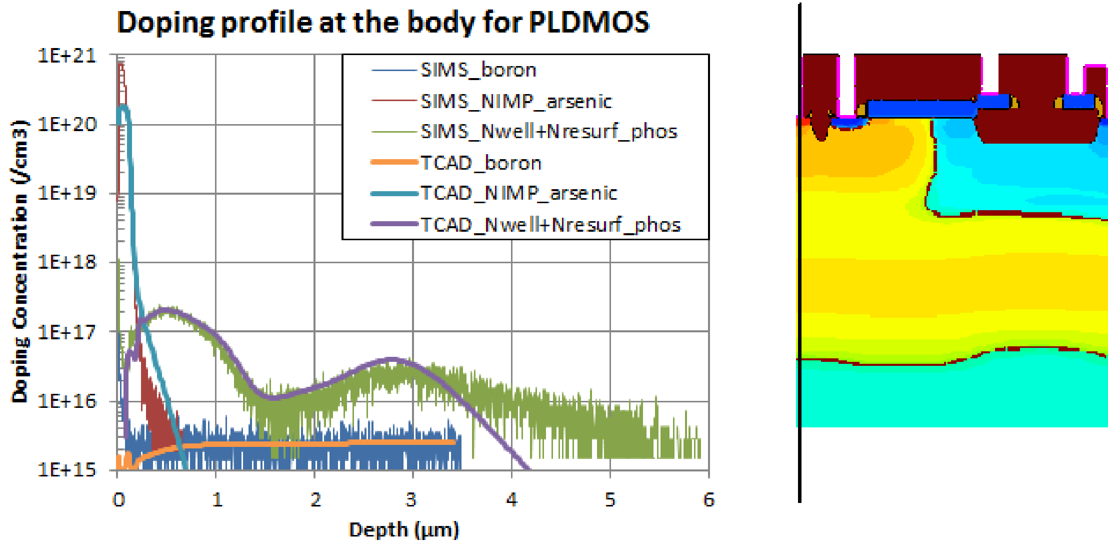


Fig. 5.15: Doping concentration across PLDMOS body region

Nwell+Nresurf layer copies data from SIMS to the depth 3 μm, then measured and simulated profile is very different. Boron concentration corresponds to measured data. NIMP layer has a lower concentration at the surface. Doping concentration across the Ndrift45 and Presurf45 region for the NLDMOS is shown in fig. 5.16.

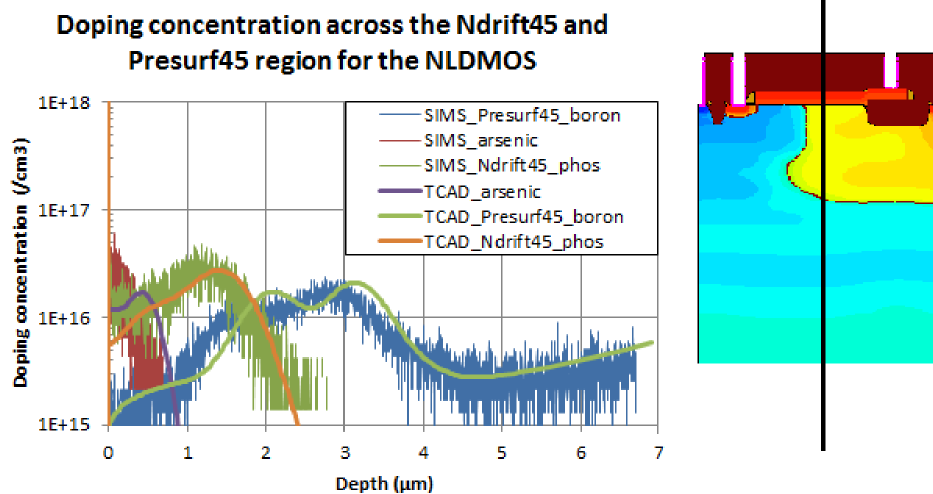


Fig. 5.16: Doping concentration across the Ndrift45 and Presurf45 region for the NLDMOS

All three simulated concentration profiles are shifted about 0, 2 μm to a greater depth, the doping concentration of layers NDRIFT45 and Presurf45 corresponds to measured data. Doping concentration of arsenic achieves lower levels at the surface.

5.6 Sensitivity to geometrical parameters

Lateral devices are sensitive to changes in geometrical parameters in general. The level of variability is given by manufacturing process, especially by photolithography. This chapter describes simulation of changes of geometrical parameters and their impact on basic electrical parameters of PLDMOS transistor. The geometrical parameters of PLDMOS transistor are shown in fig. 5.17.

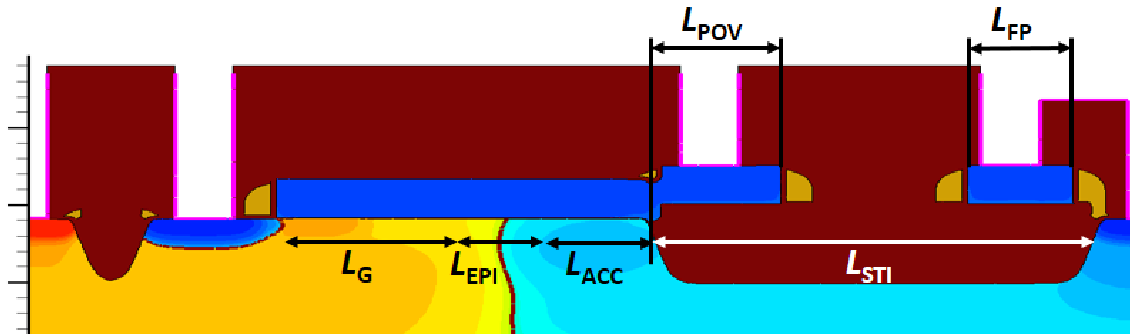


Fig. 5.17: PLDMOS geometry

Distance L_G defines gate length, L_{EPI} determines the distance between Nwell and Pdrift layer, L_{ACC} defines length of accumulation, L_{STI} determines STI length, L_{POV} defines polysilicon overlap of STI and L_{FP} defines length of field plate. Dependence of threshold voltage on change of geometrical parameters is shown in appendix A and dependence of the basic electrical parameters on L_{POV} and L_{FP} parameters is shown in appendix B.

5.6.1 Simulation of L_G change impact

Original value of L_G distance is 0,6 μm and evaluated window in range from 0,4 μm to 0,8 μm. Simulation of breakdown voltage dependence on L_G distance and comparison with measured data is shown in fig. 5.18.

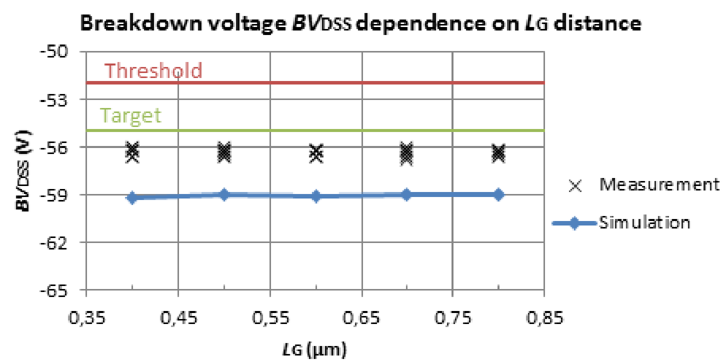


Fig. 5.18: Simulation and measured data of BV_{DSS} dependence on L_G distance

Minimum simulated value of breakdown voltage is −58,98 V and maximal value is −59,18 V,

breakdown voltage is higher than target value. This parameter is insignificantly dependent on L_G distance. Electrical breakdown occurs at the bottom of drift region and change of gate length does not influences breakdown voltage. Simulated data are shifted about 3 V to measured data towards the higher values. This difference is cause due to specific physical model we used for simulation of electrical breakdown. Simulation of R_{DSon} resistance and comparison with measured data is shown in fig. 5.19.

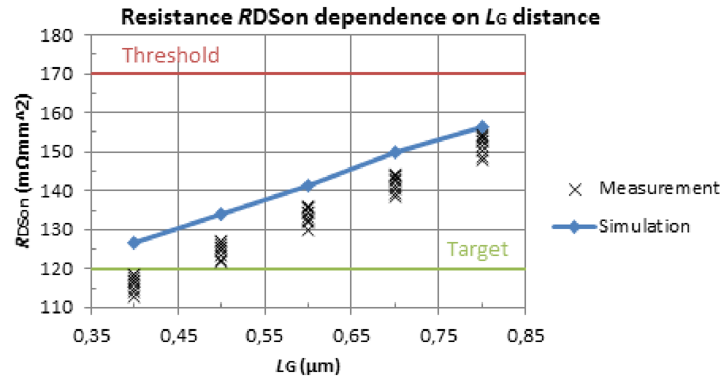


Fig. 5.19: Simulation and measured data of R_{DSon} dependence on L_G distance

The minimum simulated value of resistance R_{DSon} is 126,45 mΩmm^2 and maximal value is 156,45 mΩmm^2, values of R_{DSon} are within the allowed range. Resistance R_{DSon} is linearly increases with higher L_G distances due to increasing the resistivity of the current path flowing through the Nwell region. Simulated data are about 8 mΩmm^2 higher than measured data and also slope of simulated curve is lower than measured.

5.6.2 Simulation of L_{STI} change impact

Length of Shallow Trench Isolation L_{STI} is in original design 1,7 μm and evaluation window in range from 1,5 μm to 1,9 μm. Simulation of breakdown dependence on L_{STI} distance and comparison with measured data is shown in fig. 5.20.

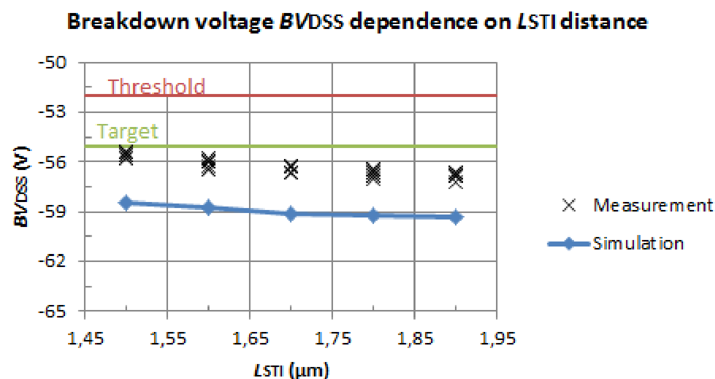


Fig. 5.20: Simulation and measured data of BV_{DSS} dependence on L_{STI} distance

Minimal simulated value of breakdown voltage is $-58{,}4$ V and maximal value is $-59{,}34$ V,

breakdown voltage is higher than target value. This parameter is increased with STI length. Simulated and measured data have the same slope, but simulated breakdown voltages are about 3 V higher than measured. Simulation of R_{DSon} resistance and comparison with measured data is shown in fig. 5.21.

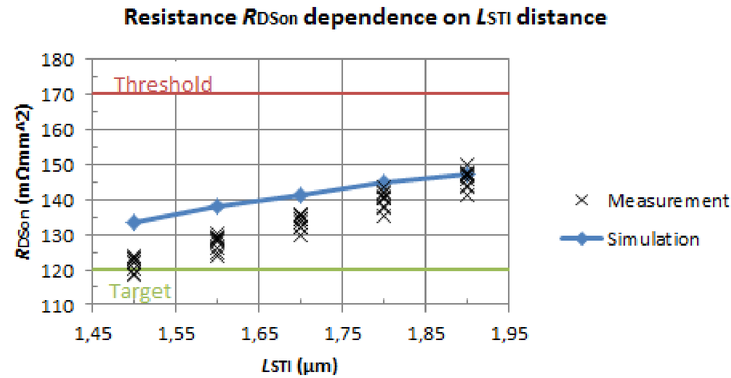


Fig. 5.21: Simulation and measured data of R_{DSon} dependence on L_{STI} distance

Minimal value of resistance R_{DSon} is 133,35 mΩmm^2 and maximal value is 147,1 mΩmm^2, values of R_{DSon} are within the allowed range. Resistivity is linearly increases with STI length due to increasing the resistivity of the current path flowing through the Pdrift region. Measured data has lower slope. Measured and simulated data are identical for $L_{\text{STI}} = 1,8\mu$m.

5.6.3 Simulation of L_{ACC} change impact

Original length of accumulation region is 0,4 μm and evaluation window in range from 0,2 μm to 0,6 μm. Simulation of breakdown dependence on L_{ACC} distance and comparison with measured data is shown in fig. 5.22.

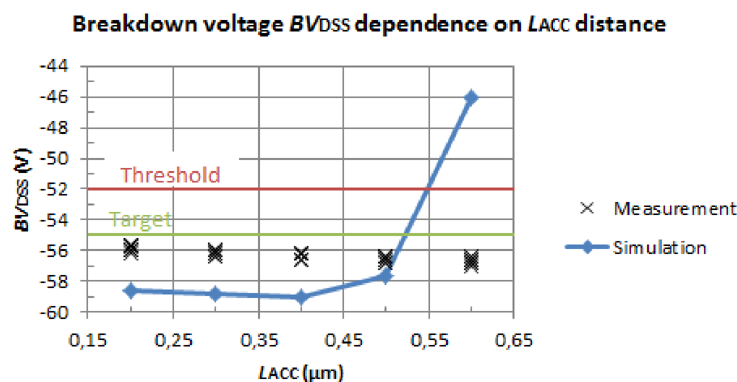
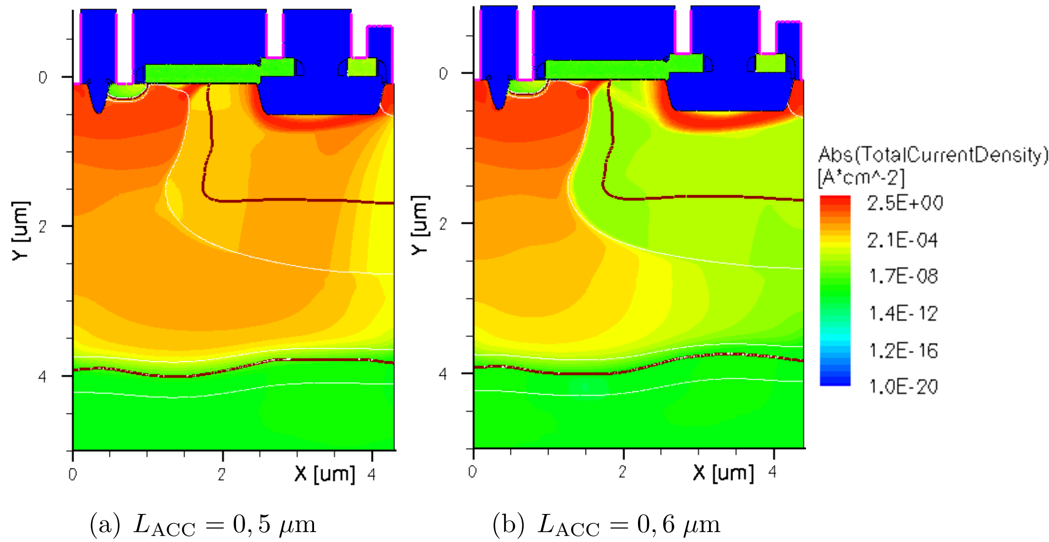


Fig. 5.22: Simulation and measured data of BV_{DSS} dependence on L_{ACC} distance

Simulated values of breakdown voltage correspond to the measured data for length of L_{ACC} in range from 0,2 μm to 0,4 μm, for higher values we can observe discrepancy between

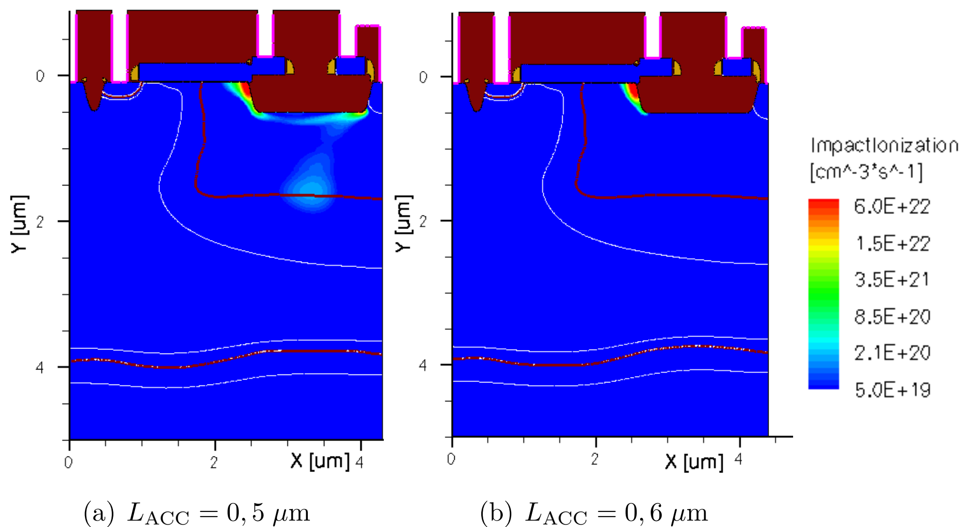
simulation and measurement. Fig. 5.23 shows total current density under breakdown condition for $L_{\mathrm{ACC}} = 0,5\ \mu$m and $L_{\mathrm{ACC}} = 0,6\ \mu$m.



(a) $L_{\mathrm{ACC}} = 0,5\ \mu$m (b) $L_{\mathrm{ACC}} = 0,6\ \mu$m

Fig. 5.23: Total current density under breakdown condition for different L_{ACC}

In normal conditions the majority of current flows to the Nresurf underneath of Drain contact as shown in fig. 5.5. For length of $L_{\mathrm{ACC}} = 0,5\ \mu$m the most of current flows around STI isolation to the Nwell region and only small part of current flows to the Nresurf. For $L_{\mathrm{ACC}} = 0,6\ \mu$m whole current flows to the Nwell region. Fig. 5.24 shows the distribution of impact ionization under breakdown condition for lengths $L_{\mathrm{ACC}} = 0,5\ \mu$m and $L_{\mathrm{ACC}} = 0,6\ \mu$m.



(a) $L_{\mathrm{ACC}} = 0,5\ \mu$m (b) $L_{\mathrm{ACC}} = 0,6\ \mu$m

Fig. 5.24: Impact ionization under breakdown conditions for different L_{ACC}

Electrical breakdown for lengths of accumulation region 0,5 μm and 0,6 μm occurs at the left corner of STI isolation. In original structure electrical breakdown occurs at the bottom

of Pdrift region underneath of Drain contact. Shift of breakdown from the Pdrift-Nresurf junction to the edge of STI causes lower simulated breakdown voltage in this structure. Relocation of electrical breakdown is caused by change of charge balance which was not seen on the wafer for mentioned evaluation window.
Simulation of R_{DSon} resistance and comparison with measured data is shown in fig. 5.25.

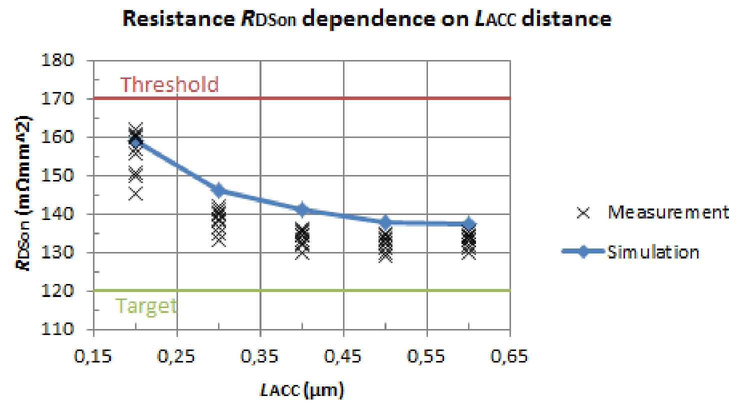


Fig. 5.25: Simulation and measured data of R_{DSon} dependence on L_{ACC} distance

Minimal value of R_{DSon} resistance is 137,3 mΩmm^2 and maximal value is 158,92 mΩmm^2, values of R_{DSon} are within the allowed range. Resistance decreases with lower L_{ACC} because part of the dose is lost in the mask during implantation. For higher value of L_{ACC} the greater part of dose gets into the silicon and thus resistivity decreases. Measured and simulated data have the same shape, maximum difference is 8 mΩmm^2 for distance $L_{\mathrm{ACC}} = 0,4$ μm.

5.6.4 Simulation of L_{EPI} change impact

Original distance between Nwell and Pdrift layer is 0,4 μm and evaluated window in range from 0,2 μm to 0,6 μm. Simulation of breakdown voltage dependence on L_{EPI} distance and comparison with measured data is shown in fig. 5.26.

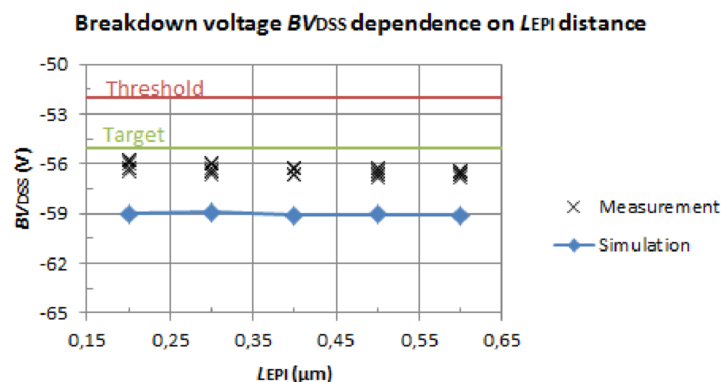


Fig. 5.26: Simulation and measured data of BV_{DSS} dependence on L_{EPI} distance

Minimal simulated value of breakdown voltage is −58,9 V and maximal value is −59,09 V, breakdown voltage is higher than target value. Impact of L_{EPI} change is negligible. The difference between simulated and measured data is approximately 3 V. Simulation of R_{DSon} resistance and comparison with measured data is shown in fig. 5.27.

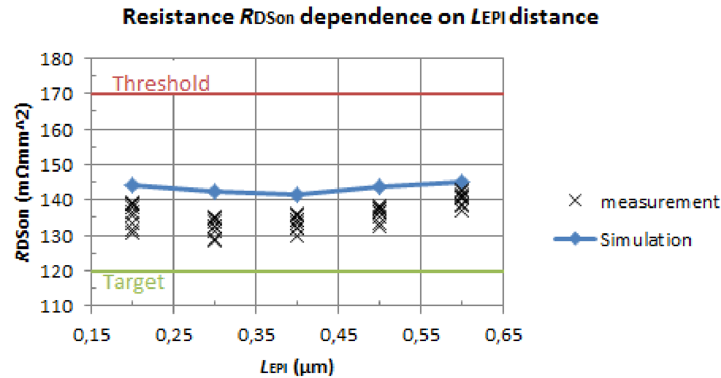


Fig. 5.27: Simulation and measured data of R_{DSon} dependence on L_{EPI} distance

Minimal simulated value of resistance R_{DSon} is 141,3 mΩmm^2 and maximal value is 145,21 mΩmm^2, values of R_{DSon} are within the allowed range. Minimal value of R_{DSon} is for distance 0,4 μm. For lower values compensation impurity between Nwell and Pdrift layers increases what leads to R_{DSon} increase. For higher distance the R_{DSon} is also higher due to increasing of resistivity of the current path flowing through the Pdrift and Nwell regions. The difference between simulated and measured data is about 6 mΩmm^2 in average.

5.7 Electrostatic Discharge Simulation

Electrostatic discharge was simulated by using TLP model and TLP pulse was modeled using a current source whose parameters are shown in tab. 5.1.

Tab. 5.1: The properties of TLP pulse in the simulation

Parameter	Value
T_{RISE}	10 ns
T_{HOLD}	100 ns
T_{FALL}	80 ns
I_{TLP}	$-1,5$ mA

Electrodes Body and Source were connected to ground in this test, Drain electrode was connected to a current source which simulates the TLP pulse and Gate electrode was biased in range from 0 V to $-3,3$ V. If Gate electrode is connected to ground then this

configuration is called ggMOS (grounded gate MOS). Simulated I/V characteristic of PLDMOS transistor for different gate voltages during ESD events is shown in fig. 5.28.

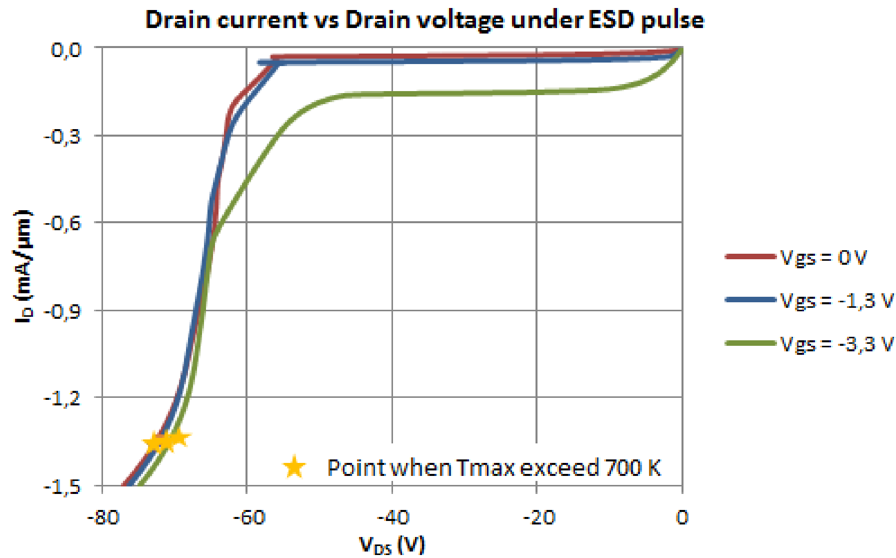


Fig. 5.28: Simualted I/V characteristic of PLDMOS transistor for different gate voltages under ESD pulse

In this figure are shows points of maximal currents before the temperature exceeds 700 K. This temperature determines when the transistor is destroyed. Maximal current of PLDMOS transistor is in range from $-1,32$ mA/μm to $-1,35$ mA/μm and for higher gate voltage this current decreases. Simulated I/V curves doesn't show snapback due to small influence of parasitic bipolar transistor. The gate voltage doesn't affect threshold voltage V_{t1} and is constant about -66 V over gate bias. Despite these shortcomings, transistor is sufficiently robust with maximum current above 1 mA/μm. The time dependence of maximal temperature in the device as function of drain voltage is shown in fig. 5.29.

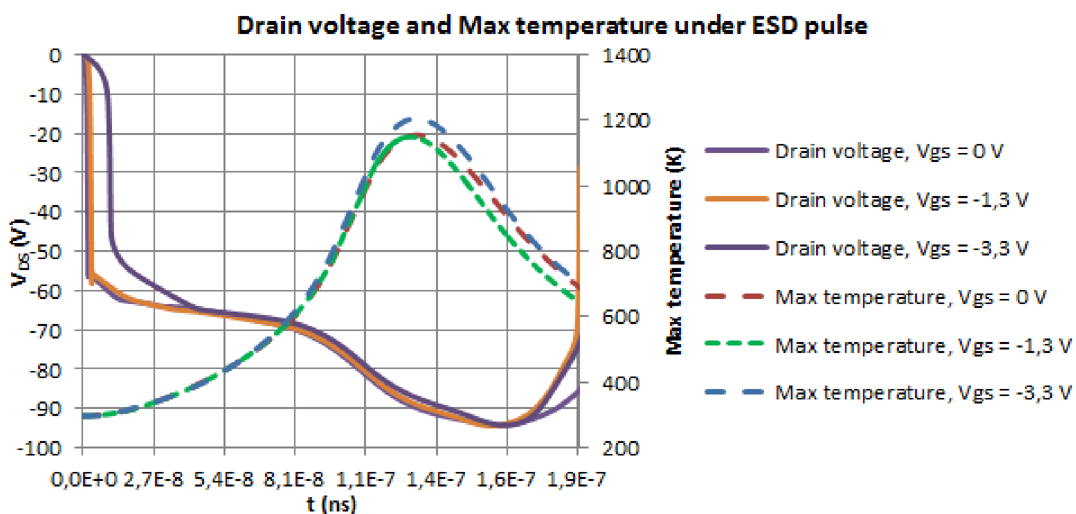


Fig. 5.29: Drain voltage and Max temperature under ESD stress

Maximal drain voltage during ESD stress exceeds value −95 V at time of 175 ns. The temperature in the model rises from an initial value 297 K and reach maximal value about 1200 K at time 135 ns and then decreases to 630 K when the ESD event ends. Gate voltage has no impact on maximal drain voltage, only affects the peak value of maximal temperature in the model. Temperature distribution in PLDMOS transistor after ESD event is shown in fig. 5.30.

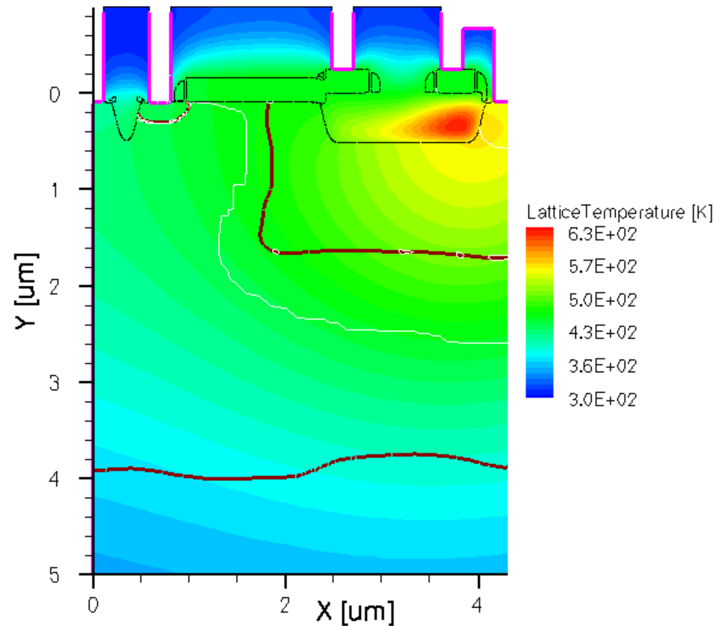


Fig. 5.30: Temperature distribution in PLDMOS after ESD stress for $V_{\mathrm{GS}} = 0$ V

The highest temperature in PLDMOS transistor during ESD event is at Drain electrode. This region is a critical part of the structure where the damage occurs. Simulation of temperature distribution is highly dependent on boundary conditions especially on the size of thermal resistances.

6 CALCULATION OF SAVE OPERATING AREA

For the calculation of Safe Operating Area are used accelerated life tests when the component is stressed by higher voltages than the maximum operating voltage. Test conditions for 45 V PLDMOS transistor are shown in tab. 6.1.

Tab. 6.1: Test condition for calculation of SOA

Parameter	**Values**
Temperature ϑ (°C)	30; 100; 150; 200
Gate voltage V_{GS} (V)	$-3,6$; $-4,2$; $-4,8$; $-5,4$
Drain voltage V_{DS} (V)	-45; -35; 0
Stress time t (s)	100; 133,35; 177,83; 237,14; 316,23; 421,70; 562,34; 749,89; 1000; 1333,52; 1778,28; 2371,37; 3162,28; 4216,97; 5623,41; 7498,94; 10000

For the PLDMOS transistor is a major degenerative mechanism Negative Bias Temperature Instability, therefore to calculate Safe Operating Area of PLDMOS transistor is used model describing NBTI degeneration. The model is used from the standard JEDEC122E as described in chapter 2.3.

$$\Delta V_{\mathrm{t}} = A_0 \mathrm{e}^{\frac{E_{\mathrm{AA}}}{\mathrm{k}T}} \mathrm{e}^{\beta V_{\mathrm{GS}}} \mathrm{e}^{\gamma V_{\mathrm{DS}}} t^n \tag{6.1}$$

The activation energy is calculated from the equation

$$E_{\mathrm{AA}} = \frac{1}{\frac{\mathrm{k}}{q}(\vartheta + 273,15)}, \tag{6.2}$$

where k is the Boltzmann's constant, q is the unit electronic charge and ϑ is the temperature. The degradation rate is the highest for voltage $V_{\mathrm{DS}} = 0$ V (the worst case) so for calculation of SOA is selected this voltage. For this reason, the model is simplificated because the term $\mathrm{e}^{\beta V_{\mathrm{DS}}}$ falls out of the model ($\mathrm{e}^{0 V_{\mathrm{DS}}} = 1$). Degradation model is thus in the form

$$\Delta V_{\mathrm{t}} = A_0 \mathrm{e}^{\frac{E_{\mathrm{AA}}}{\mathrm{k}T}} \mathrm{e}^{\beta V_{\mathrm{GS}}} t^n. \tag{6.3}$$

By logging equation (6.3) we get model into regression format

$$\ln(\Delta V_{\mathrm{T}}) = \ln(A) + \beta V_{\mathrm{G}} + \frac{E_{AA}}{\mathrm{k}T} + n \ln(t), \tag{6.4}$$

where β is the slope due to V_{GS}, E_{AA} the slope due to $\frac{1}{\mathrm{k}T}$, n the slope due to $\ln(t)$, and $\ln(A)$ the intercept. Now it is possible from measured data by using Excel *Analysis ToolPak* extract coefficients in the model. In Excel choice *Data Analysis* and select *Regression*. For Input Y Range select $\ln(\Delta V_{\mathrm{T}})$ data, the X range will be E_{AA}, $\ln(t)$ and V_{GS} data.

The model parameters are in ANOVA table in the column Coefficients. Regression gives $\ln A$ for obtaining the A parameter is used formula

$$A = \mathrm{e}^{\ln A}. \tag{6.5}$$

Extracted parameters of degradation model for 45 V PLDMOS transistor are described in tab. 6.2.

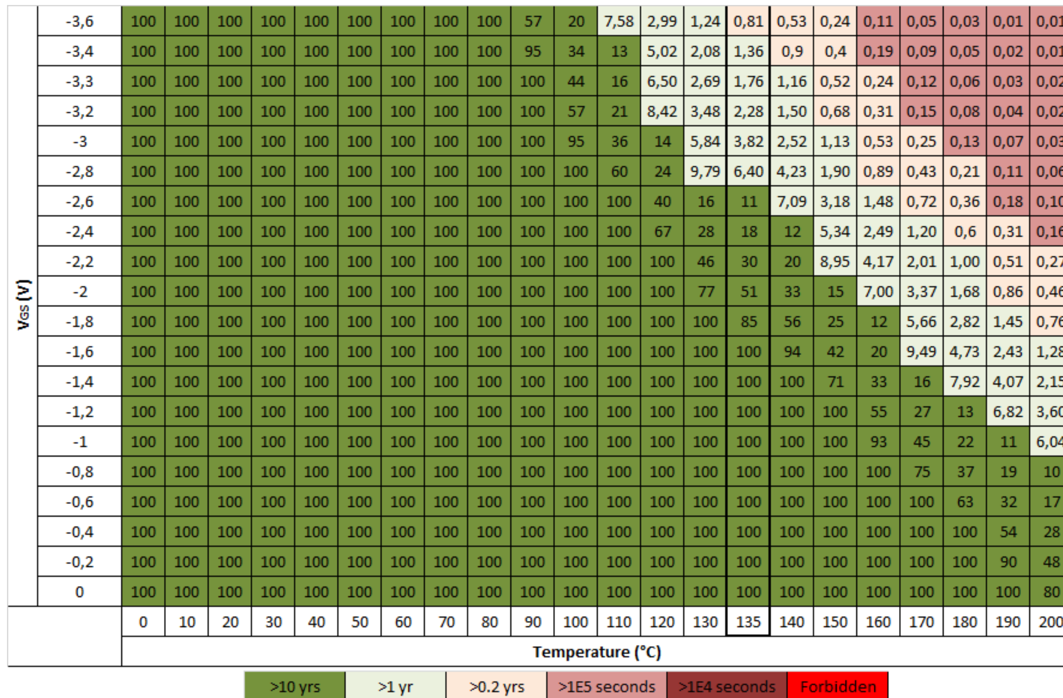
Tab. 6.2: Extracted parameters for 45 V PLDMOS transistor

A	E_{AA}	β	n
0,611819	−0,27423	−0,58497	0,226348

Lifetime of transistor is given by [10]

$$TTF = \left(\frac{\Delta V_{\mathrm{t}}}{A_0 \mathrm{e}^{\frac{E_{\mathrm{AA}}}{\mathrm{k}T}} \mathrm{e}^{\beta V_{\mathrm{GS}}}} \right)^{\frac{1}{n}}. \tag{6.6}$$

For change of threshold voltage about 10 % (max. allowed) and substituting the extracted parameters into the equation 6.6 we can graphically display the lifetime of the transistor for different gate voltages and temperatures as shown in fig. 6.1



VGS (V) \ Temperature (°C)	0	10	20	30	40	50	60	70	80	90	100	110	120	130	135	140	150	160	170	180	190	200
-3,6	100	100	100	100	100	100	100	100	100	57	20	7,58	2,99	1,24	0,81	0,53	0,24	0,11	0,05	0,03	0,01	0,01
-3,4	100	100	100	100	100	100	100	100	100	95	34	13	5,02	2,08	1,36	0,9	0,4	0,19	0,09	0,05	0,02	0,01
-3,3	100	100	100	100	100	100	100	100	100	100	44	16	6,50	2,69	1,76	1,16	0,52	0,24	0,12	0,06	0,03	0,02
-3,2	100	100	100	100	100	100	100	100	100	100	57	21	8,42	3,48	2,28	1,50	0,68	0,31	0,15	0,08	0,04	0,02
-3	100	100	100	100	100	100	100	100	100	100	95	36	14	5,84	3,82	2,52	1,13	0,53	0,25	0,13	0,07	0,03
-2,8	100	100	100	100	100	100	100	100	100	100	100	60	24	9,79	6,40	4,23	1,90	0,89	0,43	0,21	0,11	0,06
-2,6	100	100	100	100	100	100	100	100	100	100	100	100	40	16	11	7,09	3,18	1,48	0,72	0,36	0,18	0,10
-2,4	100	100	100	100	100	100	100	100	100	100	100	100	67	28	18	12	5,34	2,49	1,20	0,6	0,31	0,16
-2,2	100	100	100	100	100	100	100	100	100	100	100	100	100	46	30	20	8,95	4,17	2,01	1,00	0,51	0,27
-2	100	100	100	100	100	100	100	100	100	100	100	100	100	77	51	33	15	7,00	3,37	1,68	0,86	0,46
-1,8	100	100	100	100	100	100	100	100	100	100	100	100	100	100	85	56	25	12	5,66	2,82	1,45	0,76
-1,6	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	94	42	20	9,49	4,73	2,43	1,28
-1,4	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	71	33	16	7,92	4,07	2,15
-1,2	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	55	27	13	6,82	3,60
-1	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	93	45	22	11	6,04
-0,8	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	75	37	19	10
-0,6	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	63	32	17
-0,4	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	54	28
-0,2	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	90	48
0	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	80

Fig. 6.1: Lifetime in years of V_{T}-Extrapolated Parameter for 45 V PLDMOS transistor, $V_{\mathrm{DS}} = 0$ V

Lifetime of 45 V PLDMOS transistor in fig. 6.1 is expressed in years. For industry sector

	%Change Vt (DC use Conditions for Vds=0V)		
	Temperature Profile	Industrial (135°C)	Automotive (See Table)
Vgs	-3,6	17,66%	16,93%
	-3,4	15,71%	15,06%
	-3,3	14,82%	14,21%
	-3,2	13,98%	13,40%
	-3	12,44%	11,92%
	-2,8	11,06%	10,60%
	-2,6	9,84%	9,43%
	-2,4	8,75%	8,39%
	-2,2	7,79%	7,46%
	-2	6,93%	6,64%
	-1,8	6,16%	5,91%
	-1,6	5,48%	5,26%
	-1,4	4,88%	4,67%
	-1,2	4,34%	4,16%
	-1	3,86%	3,70%
	-0,8	3,43%	3,29%
	-0,6	3,05%	2,93%
	-0,4	2,72%	2,60%
	-0,2	2,42%	2,32%
	0	2,15%	2,06%

Fig. 6.2: Percent change over use profiles

($\vartheta = 135°\text{C}$) is guaranteed lifetime 10 years for $V_{\text{GS}} = -2,6$ V or less. Change of threshold voltage for industrial and automotive sector shows fig. 6.2.
For industry sector is shift of V_{T} calculated for temperature 135°C and for expected lifetime 10 years. For automotive sector threshold voltage change is calculated by using the temperature cycles which stress the component at a certain temperature for a defined time. Stress of the components takes place in the temperature range from $-40°\text{C}$ to 200°C, as shown in fig. 6.3. Expected lifetime for automotive sector is calculated as total accelerated time over used profiles, in this case the lifetime is 8,28 years for PLDMOS transistor. Guaranteed change of threshold voltage is less than 10 % for $V_{\text{GS}} = -2,6$ V or less for industry and automotive sector.

Goals	T_J Range (°C)	Cumulative Lifetime
Stretch	175 to 200	100 hrs
Threshold	150 to 175	1000 hrs
Threshold	125 to 150	10000 hrs
Threshold	100 to 125	10000 hrs
Threshold	50 to 100	40000 hrs
Threshold	-40 to 50	40000 hrs

Fig. 6.3: Automotive temperature use profile

7 CONCLUSION

The present work deals with the basic properties of LDMOS transistors. The theoretical part describes the structure of the LDMOS transistor, RESURF principle to increase the breakdown voltage and the effect of the parasitic bipolar transistor. Further is described the Safe Operating Area, hot carrier degradation and Negative Bias Temperature Instability. The last theoretical chapter describes the models used to simulate ESD events.
The practical part deals with the simulation of the basic parameters (threshold voltage, breakdown voltage and R_{DSon}) of NLDMOS and PLDMOS transistors. Simulated data are compared with measured data, values are similar as described in tab. 7.1. The breakdown of the simulated structures occurs at the bottom of the drift region. Next part compares the simulated concentration profiles with measured profiles. Simulated and measured concentration profiles are very similar, except small difference in Nwell+Nresurf layer. Additional calibration was not needed due to small differences in electrical data.

Tab. 7.1: Simulated and measured parameters of 45 V LDMOS devices

	Parameter	Simulation	Measurement
PLDMOS	V_{T} (V)	-0,78	-0,75
	BV_{DSS} (V)	-58,3	-58
	R_{DSon} (mΩ mm^2)	135	132,1
NLDMOS	V_{T} (V)	0,76	0,77
	BV_{DSS} (V)	61	58
	R_{DSon} (mΩ mm^2)	56,9	49

The next section was focused on evaluation of sensitivity of PLDMOS transistor to changes of its geometrical parameters. Simulated values are compared with measured data. Change of L_{G} parameter affects the resistance R_{DSon}, higher value of this distance increases resistance. The breakdown voltage of the transistor is not affected. The optimal value for this parameter is $0,5\ \mu$m, the original size of this distance is $0,6\ \mu$m. This change of L_{G} distance reduces channel resistance and also reduces the threshold voltage of the transistor. Change of L_{STI} distance affects the breakdown voltage and resistance R_{DSon}, these parameters increase with increasing L_{STI} distance. Original distance of $1,7\ \mu$m seems to be optimal with respect to the breakdown voltage and resistance R_{DSon}. L_{EPI} parameter affects only R_{DSon} resistance and optimum size is original value of $0,4\ \mu$m when the value is minimal. Parameters L_{POV} and L_{FP} have no effect on the basic electrical parameters. Thus we keep the initial values of these parameters $L_{\mathrm{POV}} = 0,5\ \mu$m and $L_{\mathrm{FP}} = 0,4\ \mu$m. Last geometrical parameter L_{ACC} affects R_{DSon} resistance and breakdown voltage. R_{DSon} resistance decreases and the breakdown voltage increases with increasing

size of this parameter. For this parameter we observed discrepancy between simulation and measurement due to inaccurate model. Measured values of basic electrical parameters are slightly different from the measured data but the shape of curves is the same. These differences are due to the models used in the simulation and due to the difference between real and simulated concentration profile of PLDMOS transistor. Although, the process team is comfortable with current targets of geometrical parameters in term of process variability, our proposal is summarized in tab. 7.2.

Tab. 7.2: Proposed changes of geometrical parameters

Parameter	Original	Proposed
L_{G} (μm)	0,6	0,5
L_{STI} (μm)	1,7	1,7
L_{EPI} (μm)	0,4	0,4
L_{POV} (μm)	0,5	0,5
L_{FP} (μm)	0,4	0,4
L_{ACC} (μm)	0,4	0,5

The next part deals with the TLP simulation where PLDMOS transistor is used as ESD protection. The maximal current for different gate voltage is in range from $-1,32$ mA/μm to $-1,35$ mA/μm than destruction of the transistor occurs (maximal temperature exceeds 700 K). The maximal current decreases for higher gate voltages. Unfortunately, we didn't get DOE wafers out from the Fab on time, so we can not compare it with the real data. We plan to do it out of this thesis.

Last section describes calculation of Safe Operating Area of PLDMOS transistor. The calculation is based on the standard JEDEC122E and major degenerative mechanism for PMOS transistors is Negative Bias Temperature Instability. Guaranteed change of threshold voltage is less than 10 % for $V_{\mathrm{GS}} = -2,6$ V or less for industry and automotive sector. It was accepted by designers and not additional optimization is required.

Technology is in qualification process and should be released this year.

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LIST OF SYMBOLS, PHYSICAL CONSTANTS AND ABBREVIATIONS

A	material parameter $(-)$
C	capacitance (F)
C_{S}	parasitic capacitance (F)
C_{OX}	gate oxide capacitance per unit area (Fm^{-2})
E	electric field (Vm^{-1})
E_{AA}	activation energy (eV)
E_{C}	critical electric field (Vm^{-1})
g_{m}	transconductance (S)
I_{G}	gate current (A)
I_{D}	drain current (A)
I_{SUB}	substrate current (A)
k	Boltzmann constant (JK^{-1})
L	gate length (μm)
L_{ACC}	length of accumulation (μm)
L_{EPI}	distance between Nwell and Pdrift layer (μm)
L_{G}	gate length (μm)
L_{hp}	distance between center line of a body contact and the center line of the nearest drain contact (μm)
L_{POV}	poly overlap of STI (μm)
L_{S}	Inductance (H)
L_{STI}	Shallow Trench Isolation length (μm)
n	empirically determined exponent $(-)$
N_{epi}	doping concentration of $n-$ layer (cm^{-3})
N_{g}	number of gate poly strips $(-)$

N_{it}	interface-traps density per area (cm^{-2})
N_{ot}	oxide-trapped-charge density per area (cm^{-2})
Q_{n}	net charge of $n-$ layer (cm^{-2})
R_{ACC}	resistance of the overlap area between the drift region and the gate ($\mathrm{m\Omega\,mm^2}$)
R_{B}	resistance of base ($\mathrm{m\Omega\,mm^2}$)
R_{D}	resistance of drain ($\mathrm{m\Omega\,mm^2}$)
R_{DSon}	($\mathrm{m\Omega\,mm^2}$)
R_{DRIFT}	resistance of drift region ($\mathrm{m\Omega\,mm^2}$)
R_{CH}	resistance of channel ($\mathrm{m\Omega\,mm^2}$)
R_{S}	resistance of source ($\mathrm{m\Omega\,mm^2}$)
t	time (s)
T	absolute temperature (T)
t_{epi}	thickness of $n-$epi layer (μm)
V_{D}	drain voltage (V)
V_{BE}	base-emitter voltage (V)
V_{DS}	drain-source voltage (V)
V_{G}	gate voltage (V)
V_{T}	threshold voltage (V)
V_{t1}	threshold voltage of ESD protection (V)
V_{t2}	thermal breakdown voltage (V)
V_{Th}	thermal voltage (V)
W	gate width (μm)
μ_{S}	surface mobility of charge carriers ($\mathrm{cm^2V^{-1}s^{-1}}$)
β	scale factor (V^{-1})
γ	scale factor (V^{-1})
ϑ	temperature (°C)

LIST OF APPENDICES

A Threshold voltage dependence on geometrical parameters **54**

B BV_{DSS} and R_{DSon} dependence on L_{POV} and L_{FP} **56**

A THRESHOLD VOLTAGE DEPENDENCE ON GEOMETRICAL PARAMETERS

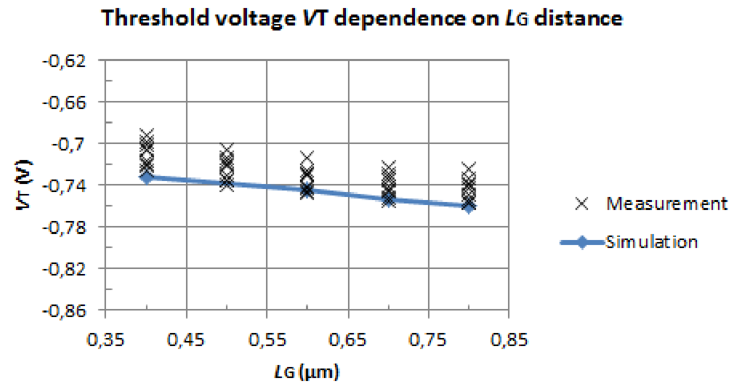

Fig. A.1: Simulation and measured data of V_{T} dependence on L_{G} distance

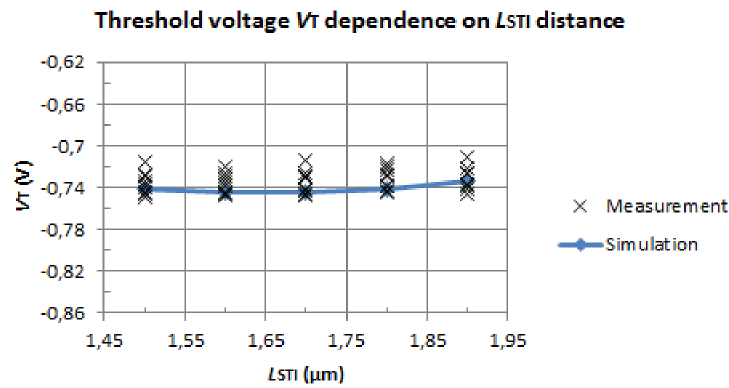

Fig. A.2: Simulation and measured data of V_{T} dependence on L_{STI} distance

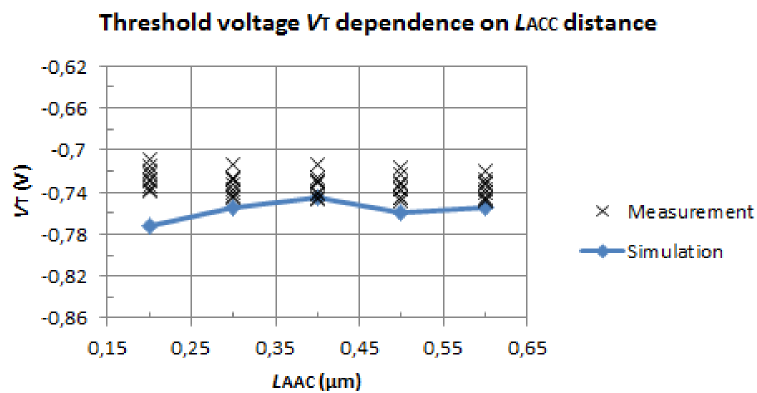

Fig. A.3: Simulation and measured data of V_{T} dependence on L_{ACC} distance

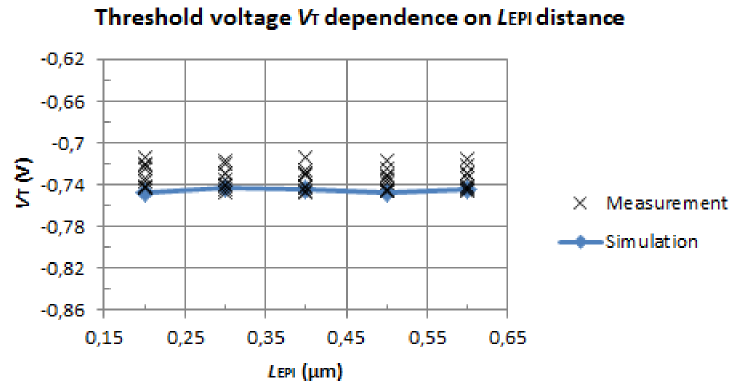

Fig. A.4: Simulation and measured data of V_{T} dependence on L_{EPI} distance

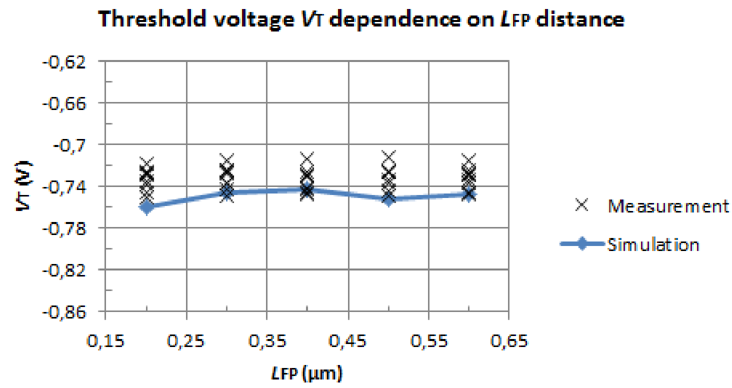

Fig. A.5: Simulation and measured data of V_{T} dependence on L_{FP} distance

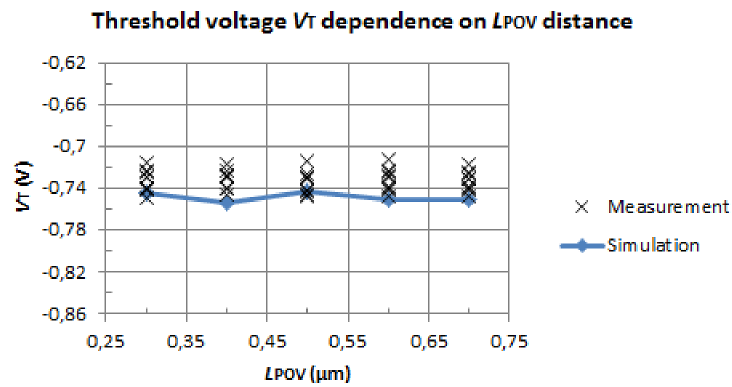

Fig. A.6: Simulation and measured data of V_{T} dependence on L_{POV} distance

B BV_{DSS} AND R_{DSON} DEPENDENCE ON L_{POV} AND L_{FP}

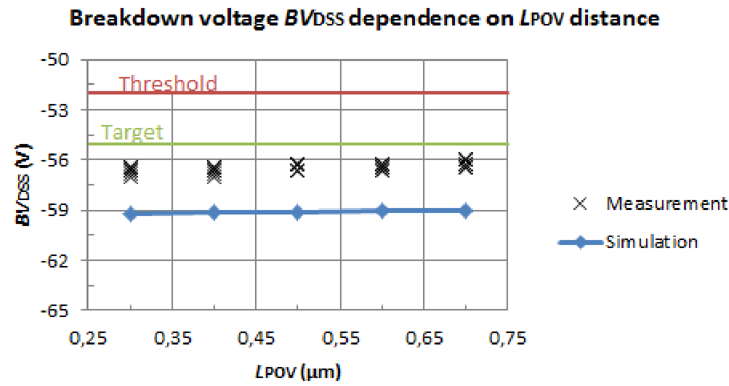

Fig. B.1: Simulation and measured data of BV_{DSS} dependence on L_{POV} distance

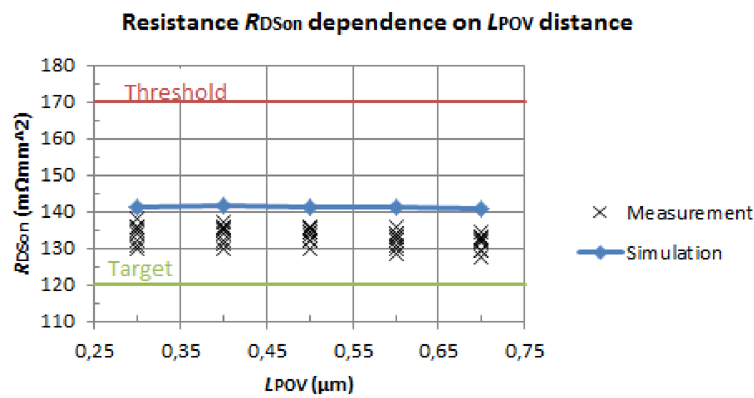

Fig. B.2: Simulation and measured data of R_{DSon} dependence on L_{POV} distance

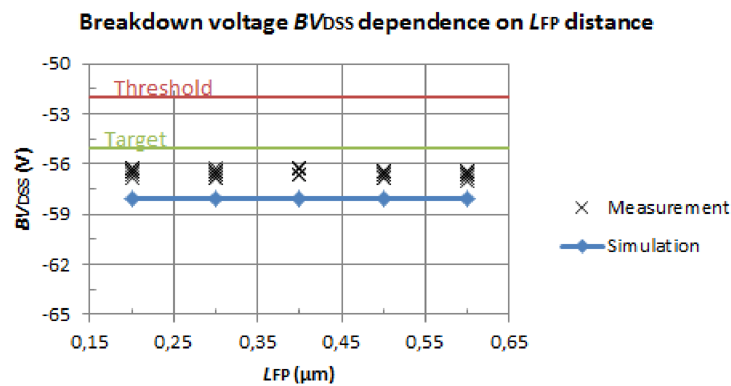

Fig. B.3: Simulation and measured data of BV_{DSS} dependence on L_{FP} distance

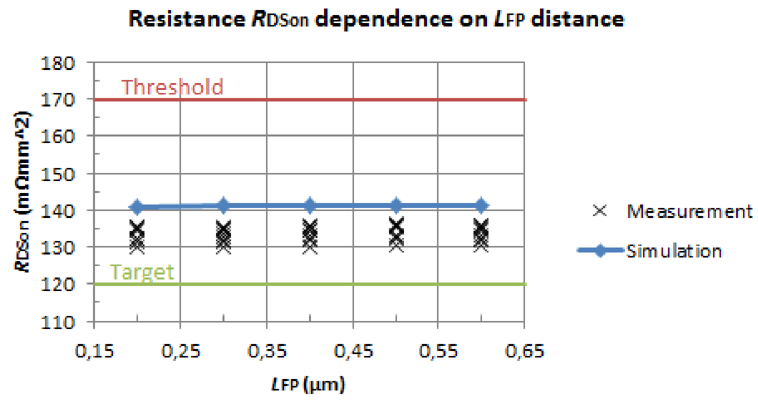

Fig. B.4: Simulation and measured data of R_{DSon} dependence on L_{FP} distance