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Full Length Article

Asynchronous delta-sigma modulator in 28 nm FDSOI technology ☆

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ABSTRACT

A novel solution of the first-order asynchronous delta–sigma modulator (ADSM) is proposed. The circuit is designed for the commercial temperature range (0 °C to 70 °C) in a 28 nm fully depleted silicon on insulator (FD-SOI) technology from STMicroelectronics. This technology allows designing new subcircuit topologies, resulting in an ADSM that offers a 64.2 dB signal-to-noise and distortion ratio (*SNDR*) corresponding to a 10.37-bit resolution in the signal bandwidth of 10 kHz. The ADSM consumes 4.1 μW at a power supply of 1 V, and the obtained power efficiency is 0.15 pJ/conversion. The ADSM occupies an area of only 0.0042 mm^2.

1. Introduction

Delta-sigma modulators are among the most popular data converter circuits. Conventionally, these modulators find wide use in high-resolution, low-speed applications. The circuits have a long history originating in the early development phases of pulse code modulation (PCM) systems, which were formed after the invention of delta modulation in France by E. M. Deloraine, S. Van Mierlo, and B. Derjavitch in 1946 [1,2]. Until the 1980s, when integrated switched-capacitor (SC) circuits began to be implemented as a well-understood technology, modulators were realized using continuous-time (CT) integrators.

Upon the advent of the SC technique, discrete-time (DT) integrators gradually became popular due to their high linearity with an accurate time constant and low sensitivity to process variations. The DT delta-sigma modulator's speed, however, is limited by the settling time, producing a limited sampling frequency [3]. Thus, implementing CT delta-sigma modulators emerged as a favored option again, the loop filter being structured from CT circuits such as transconductors or integrators to reduce the speed requirements of the filters. Principally, CT architectures then show better power efficiency. The CT modulator nevertheless suffers from circuit nonidealities, including the sensitivity to the system clock jitter, process-dependent integrator time constant, and excess loop delay [4,5], all of which render the component's practical advantage inconclusive.

As a matter of fact, another type of the delta-sigma modulator, namely, the asynchronous delta-sigma modulator (ADSM), has gained in popularity in recent years. The architecture, originally introduced by Kikkert [6], can be considered a special variant of the CT delta-sigma modulator. Compared to the standard CT model, ADSMs provide multiple benefits, including a simple circuit design, immunity to clock jitter, and the absence of quantization errors and a clock signal [7].

A large number of state-of-the-art research articles on ADSMs have been published to date, mostly presenting systems with a;very low power consumption, one in the order of tens of nW [8]. This property is achieved by using very low power supply voltages (from 0.25 to 0.3 V) when bulk-driven transistors operating in the subthreshold region are employed. However, the transconductance of a bulk-driven MOSFET is substantially smaller than that of a conventional gate-driven MOSFET [9]. By extension, the bulk is not isolated from the MOSFET channel, such as the gate terminal, which may result in a parasitic bulk current. Importantly, the above-discussed ADSMs are also characterized by a very low bandwidth, one in the range of 20 to 70 Hz; for such a bandwidth, a very high integrator time constant must be designed. The goal is achieved by utilizing very large passive components (R, C), and these are often placed outside the chip.

Besides the above ADSMs, which focused on a markedly low power consumption offering a very low bandwidth, several high-frequency (units of MHz) ADSMs have been presented [10–14]. Generally, the central advantage of such ADSMs rests in the lower value of the integrator time constant; thus, the passive component values are smaller, following from the smaller chip area compared to that of the very low bandwidth ADSMs. However, the high-frequency capability is redeemed by a large power consumption, one in the order of units of mW. Some other ADSMs nevertheless offer a trade-off between the speed, power consumption, and chip area [15,16].

This article proposes an ADSM that embodies an alternative to the DT delta-sigma modulators applied in portable biomedical devices [17] or vibration sensor processing [18]. This ADSM utilizes the 28 nm

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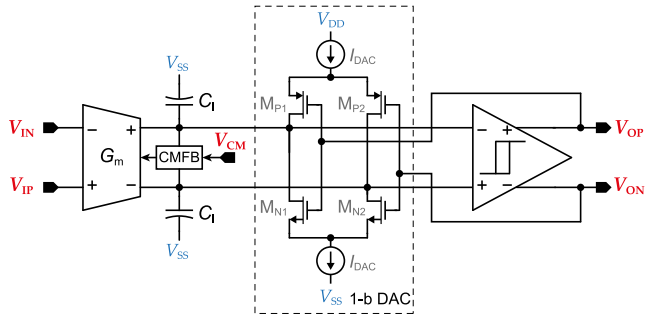

Fig. 1. A block diagram of the proposed fully differential first-order ADSM.

FD-SOI technology, resulting in a modulator with unique parameters; these include an extremely low silicon area, bulk or precisely back-gate driven circuits that do not suffer from parasitic bulk currents, and high signal-to-noise to distortion ratio (*SNDR*). To achieve these properties, new transconductor and hysteresis comparator topologies are designed. The performance of the circuits is analyzed on a circuit model comprising parasitic R and C extracted from a layout where the Cadence Virtuoso with a Spectre simulator is used.

This paper is organized as follows: Section 2 discusses the properties of a first-order ADSM and the determination of its basic parameters. Section 3 proposes a MATLAB Simulink model of the ADSM, including the non-ideal effects that occur in its analog blocks. All necessary parameters of the proposed ADSM are specified in this section. Section 4 introduces novel analog circuits on the transistor level and demonstrates the simulation results; in Section 5, post-layout simulations and ADSM's overall parameters are presented; and Section 6 highlights the major conclusions of the work.

2. Asynchronous delta-sigma modulator

In the above-cited references, the ADSMs are implemented using either first or second-order loop filters. The former option is implemented in this article according to [10], where the authors recommend a first-order modulator due to the easy implementation when using a second-order loop filter may only slightly improve the ADSM's performance. Moreover, the slight performance improvement is achieved at the cost of an increase in the chip area, power consumption, and circuit complexity.

2.1. Limit cycle frequency

A block diagram of the proposed fully differential first-order ADSM is shown in Fig. 1. The circuit comprises a CT Gm–C integrator, a hysteresis comparator, and a feedback 1-b digital-to-analog converter (DAC).

The output V_{OP} (or V_{ON}) 1 is a pulse width modulated square wave of period T with high logic state denoted as T_1 and a low logic state represented as T_2. The state T_1 can be calculated from C_I value, its charge/discharge current I_C, and the comparator's hysteresis width, defined by the threshold levels $\pm V_H$. During the period, the capacitor C_I is discharged by I_C; as a result, the voltage on C_I decreases from $+V_H$ to $-V_H$. This is mathematically expressed as

$$T_1 = \frac{2V_H C_I}{I_C} = \frac{2V_H C_I}{I_{Gm} - I_{DAC}} = \frac{2V_H C_I}{V_{IN} G_m - I_{DAC}}, \tag{1}$$

where I_{Gm} is transconductor's output current, I_{DAC} is the current from the DAC, and V_{IN} (or alternatively V_{IP}, where $V_{IN} = |V_{IP}|$) is voltage on the inverting input of the transconductor.

Period T_2 can be derived in the same way; thus,

$$T_2 = \frac{2V_H C_I}{I_C} = \frac{2V_H C_I}{I_{Gm} + I_{DAC}} = \frac{2V_H C_I}{V_{IN} G_m + I_{DAC}}. \tag{2}$$

When a zero-input signal is applied, namely, $V_{IP} = V_{IN} = 0\,V$, the output of the ADSM is a square wave signal with a duty cycle of 50%. In this state, the maximum possible frequency occurs and is denoted as the center frequency or limit cycle frequency, f_C. By defining $T_C = 1/f_C$ as the period of the output signal, it can be calculated as

$$T_C = T_1 + T_2 = \frac{4V_H C_I}{I_{DAC}}. \tag{3}$$

The limit cycle frequency of ADSMs determines the carrier-to-bandwidth ratio (*CBR*) and is equivalent to the oversampling ratio (*OSR*) in synchronous delta-sigma modulators [12]. This is mathematically expressed as

$$CBR = \frac{f_C}{2f_{BW}}, \tag{4}$$

where f_{BW} is the input signal bandwidth.

As can be derived from (1) and (2), the parameter *CBR* is not constant such as *OSR*. If the input signal is nonzero ($V_{IN} \neq 0\,V$), the output carrier frequency does not remain equal to f_C but decreases; therefore, the term output instantaneous frequency (f_I) is introduced to describe the frequency of the output carrier frequency for an arbitrary instantaneous magnitude of the input signal. Its maximum value equals f_C when $V_{IN} = 0\,V$. We have

$$f_I = f_C\left(1 - v_n^2\right), \tag{5}$$

where $|v_n| < 1$ is a normalized input signal amplitude representing the depth of the modulation, which is defined as the ratio between the amplitude of the actual input signal and the maximum input signal applicable to the ADSM's input. Mathematically, this reads

$$v_n = \frac{V_{IN}}{V_{IN(max)}} = \frac{G_m V_{IN}}{I_{DAC}}. \tag{6}$$

The normalized input signal amplitude v_n can also be expressed in terms of T_1 and T_2 as

$$v_n = \frac{T_1 - T_2}{T_1 + T_2}. \tag{7}$$

The limit cycle frequency required for a specific conversion accuracy must be carefully determined. For a zero input signal, the output frequency spectrum contains a single tone at the limit cycle frequency ($f_I = f_C$). When the sinusoidal input signal is applied, the output is modulated, and the Bessel components appear around the output instantaneous frequency. The worst condition arises when $v_n \to 1$ because low-frequency components appear in the output spectrum; thus, the limit cycle frequency should be set far away from the baseband to avoid the appearance of Bessel components in the selected frequency baseband [10].

It should be noted that the limit cycle frequency can be negligibly affected by the comparators' propagation delay, which increases the effective value of the hysteresis, meaning that the impact of the comparator delay, τ_C, on the limit cycle frequency of the proposed ADSM should be considered. Then, Eq. (3) can be rewritten as

$$T_C = \frac{4V_H C_I}{I_{DAC}} + \tau_C. \tag{8}$$

Eq. (8) shows that the limit cycle frequency, $f_C = 1/T_C$, decreases for a higher comparator propagation delay value.

2.2. Signal-to-noise ratio (SNR)

The output bitstream can be recovered by applying an ideal low-pass filter with a cut-off frequency at the signal bandwidth (f_{BW}). When the ADSM is used in an analog-to-digital (A/D) data conversion, a decoding circuit is required. The input signal can be recovered by the measuring periods T_1 and T_2. This step is achievable with time-to-digital converters (TDC); the simplest method nevertheless lies in utilizing the sample and holding the circuit, as illustrated in Fig. 2.

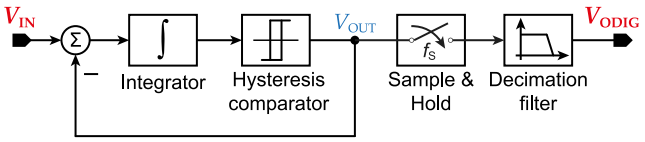

Fig. 2. A general ADSM block diagram including asynchronous signal processing.

To calculate signal-to-noise ratio (*SNR*), the total demodulated noise power (P_N) must be determined first. In [19] the author proposes certain simplifying assumptions to express P_N within a bandwidth f_{BW} amounts to

$$P_N = \frac{8}{3}\frac{f_I f_{BW}}{f_S^2}, \tag{9}$$

where f_S is sampling frequency.

Several authors have derived a mathematical formula for determining the *SNR* in ADSMs. In [19], the procedure exploits (9), and the *SNR* is defined as

$$SNR = \frac{P_S}{P_N} = \frac{3f_S^2}{4f_{BW}f_I}, \tag{10}$$

where P_S is the signal power of a harmonic signal with an amplitude at the overload level, that is, $v_n = 1$ and $P_S = \frac{1}{2}$.

Eq. (10) shows that the *SNR* can be increased by changing just the sampling frequency f_S. However, a very high sampling frequency f_S or, more precisely, limit cycle frequency oversampling ($f_S/(2f_C)$) is required to achieve a high *SNR* with a first-order ADSM. This is due to the absence of noise shaping.

The modified formula for determining the *SNR* include various v_n is [8,20]

$$SNR = \frac{3}{4}\frac{f_S^2}{f_{BW}f_I}v_n^2. \tag{11}$$

Slightly different formulas are also proposed in [6,7]. In terms of completeness, it should be noted that these formulas consider only the "digital" noise produced during the sampling of the asynchronous output signal of the ADSM; the noise generated in the ADSM analog circuits is not included.

3. System level design

Besides the mathematical relations mentioned above, an ADSM model is created in MATLAB Simulink using the Simscape extension to verify the calculated values and to analyze other nonideal effects on the overall ADSM parameters. The model is shown in Fig. 3.

3.1. Determination of limit cycle frequency

First, it is necessary to determine the limit cycle frequency (f_C) and the assumed sampling frequency (f_S) at which the output analog bitstream will be sampled. These parameters result from Eq. (11) when the input parameters are the known bandwidth of the processed signal, f_{BW} = 10 kHz, and an *ENOB* (effective number of bits) of not less than 10 (*SNR* ≥ 62 dB); the modulation depth is v_n = 0.8. However, f_S and f_I are two unknown values in (11), where f_I is related to f_C according to Eq. (5). The dependence of the *SNR* on the sampling frequency f_S is shown in Fig. 4. Theoretically, it is possible to achieve any resolution by just modifying f_S. However, its maximum value will be limited by the noise of the analog parts and the maximum sampling rate given by the technology. Based on the experimental results from the ADSM model in MATLAB, a target value of *SNR* = 65 dB is chosen.

As shown in Fig. 4, *SNR* = 65 dB can be achieved using f_C = 100 kHz (*CBR* = 5) and a high sampling frequency, f_S = 100 MHz, to capture the edges of the asynchronous signal accurately. Another option is to use a higher f_C, such as 1 MHz (*CBR* = 50), with f_S = 30 MHz. A higher value of *CBR* (and also f_C) has the advantage of the low-frequency components being set far away from the baseband in the output spectrum. On the other hand, the lower f_C offers the benefit that the requirements on the analog circuits are markedly more relaxed. Thus, for example, the comparator's transient nonidealities, such as the propagation delay or its different values for the outputs, have a lower impact on the ADSM's parameters. Based on these findings and the observations from the ADSM model in MATLAB, f_C = 100 kHz is selected.

3.2. Determining the basic analog circuit parameters

The values of the limit cycle frequency f_C and the modulation depth v_n were determined in Section 3.1. Now, the circuit parameters that directly set the f_C and v_n values can be calculated according to Eqs. (3) and (6). The limit cycle frequency f_C is settable using V_H, C_I, and I_{DAC}, as shown in Eq. (3). An appropriate tradeoff must be found among the values of these parameters.

The comparator hysteresis V_H directly sets the voltage swing on the outputs of the capacitors and transconductors. The circuit's input/output range requirements are more relaxed when a lower value of V_H is used. A lower value allows designing circuits with simpler input/output stages when the rail-to-rail structures are unnecessary. Regarding the capacitors, their value must be carefully determined with respect to the chip area, mutual matching in a fully differential configuration, and current leakage; for instance, the area of the capacitor impacts the current leakage, which grows with the area and applied voltage (defined by V_H) on the capacitors. Furthermore, matching errors result in higher harmonics tones in the output spectrum and degrade the resulting *SNR*. The parameters calculated according to Eqs. (3) and (6) are V_H = 100 mV, C_I = 3.125 pF, G_m = 200 nA/V, and I_{DAC} = 125 nA for f_C = 100 kHz and v_n = 0.8. The impact of global and local variations of the parameters will be shown in Section 4.

A timing diagram of the voltages at the capacitor and the output node (V_{OP}) for the calculated values is shown in Fig. 5. The corresponding frequency spectrum of the output signal is shown in Fig. 6. It is noticeable that the output instantaneous frequency (f_I) will decrease as the V_{IP} increases. The high-frequency components shift to the low-frequency region, and the tails at the adjacent harmonics of f_C are mixed.

4. Circuit design on the transistor level

The proposed ADSM has been designed on the transistor level using a standard threshold voltage (V_{TH}) and low V_{TH} transistors where necessary in the 28 nm FD-SOI technology. This technology enables a very wide V_{TH} tuning range of ~250 mV for the FD-SOI versus 10 mV for the bulk CMOS, in addition to very good analog intrinsic performances, high-performance energy-efficient solutions, and reduced parasitic capacitances [21]. The circuit was designed for V_{DD} = 1 V with rail-to-rail input signal range ($V_{IN(max)} = V_{CM} \pm 0.5$ V) in the signal bandwidth (f_{BW}) of 10 kHz. All of the parameters have been verified on a post-layout model with a Spectre simulator.

4.1. Transconductor

The transistor-level schematic of the proposed transconductor is shown in Fig. 7. The single-stage, fully differential transconductor consists of an input differential pair, current mirrors including current shunts to increase the transconductance (g_m) of the differential pair, a class A output stage, and a CMFB circuit. All transistors in the circuit are designed to operate in the center of moderate inversion, namely, where the inversion coefficient (*IC*) equals 1. In this region, the g_m/I_D ratio almost approaches its maximum, thus being an optimal design variant.

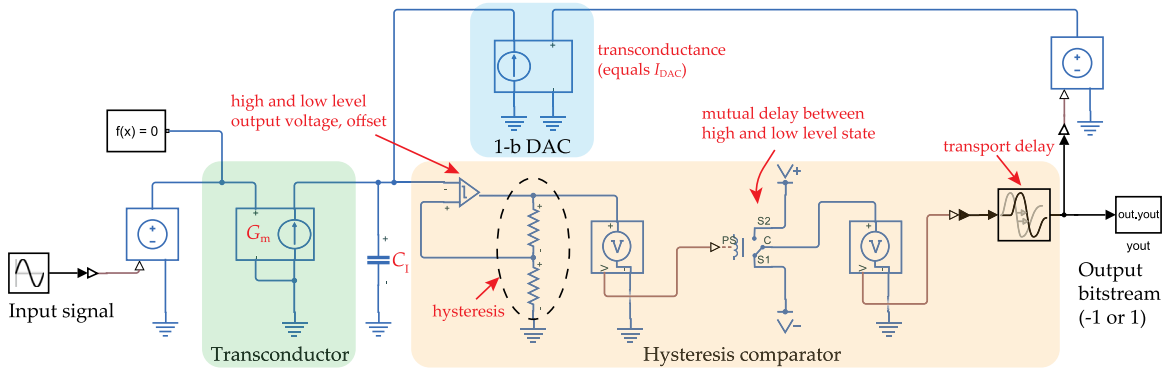

Fig. 3. A block diagram of the MATLAB Simulink model of the first-order ADSM.

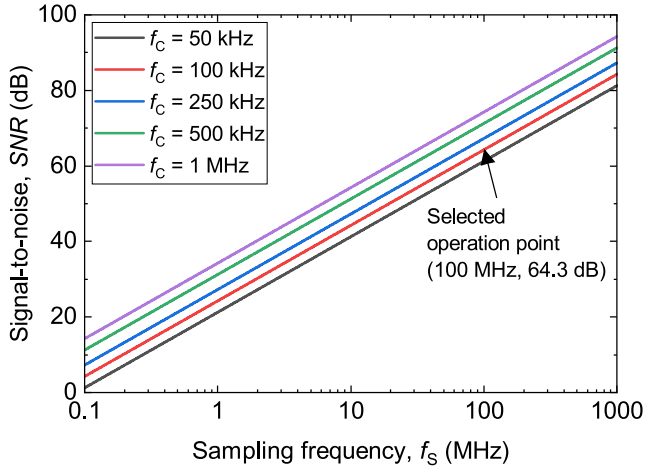

Fig. 4. An estimation for the achieved *SNR* versus oversampling rate in a different limit cycle frequency, f_C (f_{BW} = 10 kHz, v_n = 0.8).

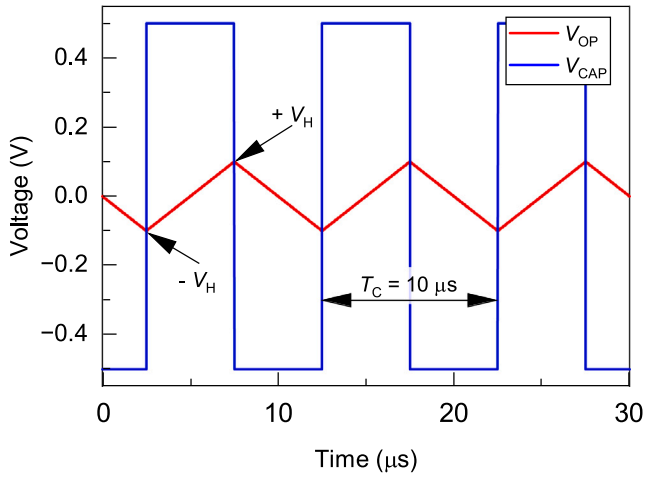

Fig. 5. The timing diagram of the MATLAB model of the ADSM ($V_{IP} = V_{IN}$ = 0 V).

The input differential pair consists of four transistors M_1-M_4 implemented with low V_{TH} NMOS transistors. The transistor M1 is driven from both gates, the front (V_{GS1}) and the back ones (V_{BS1}). Due to the requirement for rail-to-rail operation, the front gate of M_1 is driven through M_3 to eliminate the minimum input voltage limitation arising from M_1's V_{TH}. The front gate of M3 is connected to V_{DD}, and the back gate is linked to the input, where the input signal changes the threshold voltage (V_{TH3}) of M_3 and, consequently, the front gate voltage (V_{GS1})

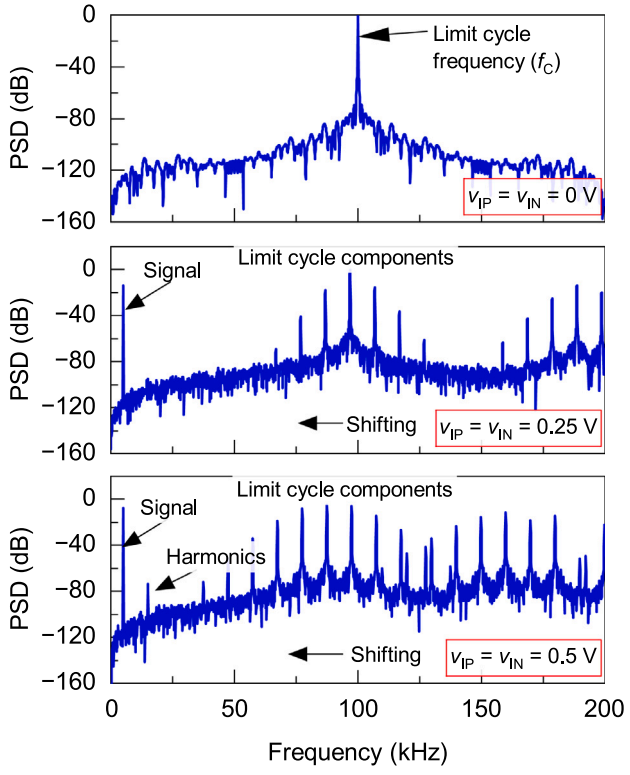

Fig. 6. The frequency spectrum of the ADSM with a different input signal amplitude.

of M_1. Then, the overall input differential pair transconductance g_{dp} can be mathematically described as

$$g_{dp} = g_{G,B1} + \frac{-\Delta V_{GS3}}{\Delta V_{G,B3}} g_{m1}, \tag{12}$$

where $g_{G,B1}$ is M_1's back gate transconductance.

As the front and the back interface of an FD-SOI MOSFET can be in accumulation, depletion, or inversion, there are nine possible modes of operation, depending on V_{GS} and V_{BS}. In this case, the front interface of all back-gate driven MOSFETs (M_1-M_4) lies in the inversion mode and the back one in the depletion; a channel is formed at the front gate side. Then, the threshold voltage (V_{TH3}) variation with respect to V_{BS3} can be mathematically expressed as [22]

$$\begin{aligned} \frac{dV_{TH3}}{dV_{G,B3}} &= -\frac{t_{ox1}/\varepsilon_{ox} + t_{DSf}/\varepsilon_{Si}}{\left(t_{Si} - t_{DSf} + t_{dep}\right)/\varepsilon_{Si} + t_{ox2}/\varepsilon_{ox}} \\ &\cong -\frac{C_{ox1}}{C_{Si} + C_{ox2}} \cong -\alpha, \end{aligned} \tag{13}$$

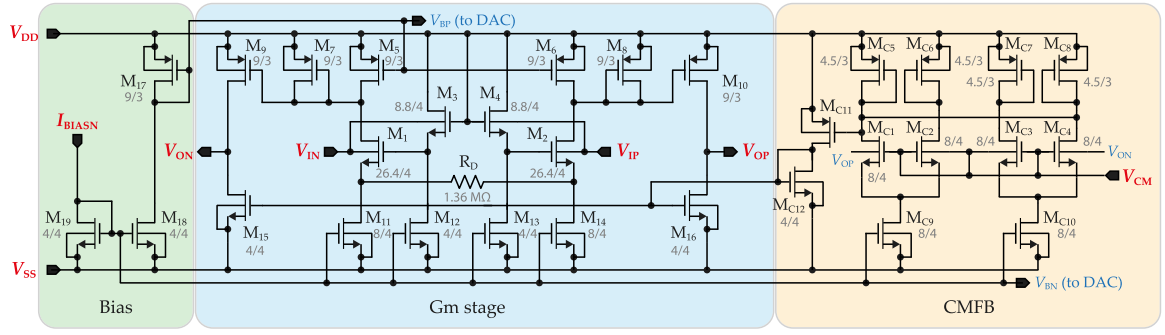

Fig. 7. A schematic of the proposed rail-to-rail transconductor; all dimensions of MOSFETs are in units of μm, i.e. 8/4 = 8 μm/4 μm.

where t_{ox1} is front-gate oxide thickness, t_{ox2} is back-gate or buried oxide thickness, ϵ_{ox} denotes the permittivity of SiO_2, ϵ_{Si} is the permittivity of silicon, t_{Si} represents the silicon channel thickness, t_{dep} stands for the depletion width, and t_{DSf} is the dark space close to the front interface of the channel.

In most cases, the following approximation can be made [23]:

$$\alpha \cong -\frac{t_{ox1}}{t_{ox2}}. \tag{14}$$

The thickness ratio (α) of the front and the back gate oxides is approximately 0.25 in the employed technology.

The dependence of V_{GS} on $V_{G,B}$ should be ideally the same as the dependence of V_{TH} defined in Eq. (13). Yet V_{GS} is affected by some nonidealities, entailing its dependency on additional parameters. Consequently, the variation of V_{GS} on $V_{G,B}$ differs from the variation of V_{TH} on $V_{G,B}$. Mathematically, V_{GS} is expressed as

$$\frac{\Delta V_{GS3}}{\Delta V_{G,B3}} = 2nV_T \ln(e^{\sqrt{IC}} - 1) + \frac{\Delta V_{TH3}}{\Delta V_{G,B3}}, \tag{15}$$

where n is the subthreshold slope, V_T denotes the thermal voltage, and IC stands for the inversion coefficient, defined as

$$IC_3 = \frac{I_{D3}}{\left(k_n' \frac{W}{L}\right)_3 (2nV_T)^2}. \tag{16}$$

The current I_{DS3} is generated by M_{12}, whose finite output resistance causes the dependency of I_{DS12} on V_{DS12}. Thus, IC_3 is affected by the variation of V_{TH3}, and $\Delta V_{GS}/\Delta V_{G,B}$ will be slightly different than $\Delta V_{TH}/\Delta V_{G,B}$.

A source degeneration resistor, R_D, is added between the sources of M_1 and M_2 to improve the transconductor's linearity. A higher linearity can be achieved when $R_D \gg 1/g_m$. The disadvantage of employing R_D is that a large resistor value is needed to maintain a wider linear input range. Using a passive resistor costs more chip area than a source degeneration resistor implemented with MOSFETs; however, the linearity of the MOSFET resistor is limited and may significantly degenerate the ADSM's overall *SNDR*.

The differential pair output current, i_{D1}, is related to the input voltage by the equation

$$i_{D1} = G_{mR} v_{id}, \tag{17}$$

where $v_{id} = V_{IP} - V_{IN}$, and G_{mR} is the transconductance of the differential pair including the degeneration resistor R_D.

The transconductance G_{mR} can be mathematically described as

$$G_{mR} \approx \frac{g_{dp}}{1 + g_{dp} R_D}. \tag{18}$$

Then, the transcondustor's output current is

$$I_{ON} = \frac{W_9 L_7}{W_7 L_9} \left(G_{mR} v_{id} - I_{D5}\right) - I_{D15}, \tag{19}$$

where I_{ON} flows from the negative output; current from the positive output is given as $I_{OP} = -I_{ON}$. Parameters G_{mR} and I_{ON} can be calculated using Eqs. (12), (15) and (16).

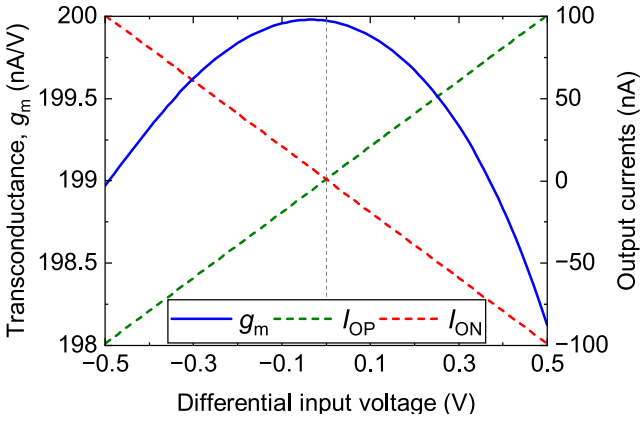

Fig. 8. The transconductance, G_m, as a function of the differential input voltage.

A CMFB circuit using two differential pairs with back-gate-driven MOSFETs is included, Fig. 7. Due to process limitations, the back gate-driven low V_{TH} PMOS cannot be used without triple-well isolations, which increase the transconductor's area and worsen the mismatch. Thus, the input differential pairs are implemented with NMOS transistors. Consequently, the CMFB bias output must be converted from a PMOS bias to an NMOS one via M_{C11} and M_{C12}. This circuit has a rail-to-rail input voltage range, satisfying the requirements over PVT corners.

The simulated input voltage dependence of the transconductor's G_m is shown in Fig. 8. All of the simulated parameters across the PVT corners are summarized in Table 1.

4.2. Hysteresis comparator

As mentioned earlier, the comparator's hysteresis and propagation delay significantly affect the limit cycle frequency and, thus, the overall parameters of the ADSM. Another critical parameter affecting the modulator's *SNDR* is the mutual delay between the differential output signals (V_{OP} vs V_{ON}); this delay may be caused by, for example, the different slew rate of the rising and falling edge of the input stage's output signal. As a consequence of the mutual asymmetry of the outputs, the DA converter's fully differential outputs do not switch synchronously; the state of the first output changes earlier than that of the second one or vice versa. This phenomenon results in an increase of the higher harmonic components in the output spectrum and, thus, a decreasing *SNDR*.

Based on the above requirements, an improved self-biased comparator is proposed and shown in Fig. 9. Its differential pair is designed as single-ended, and differential outputs are derived from it. This solution has the advantage of a simple structure that does not need to incorporate the CMFB circuit.

Table 1
Simulated parameters of the transconductor.

Parameter	Unit	Min	Typ	Max
Transconductace, G_m	nA/V	166	200	244
Voltage gain, A_U	dB	41.1	45.6	49.3
Power consumption, P_d	µW	3.2	3.7	4.1
PSRR	dB	40	49	58
CMRR	dB	53.2	59.3	60.4
THD (V_{IP} = 1 V_{pp}/1 kHz)	%	0.022	0.047	0.077
THD (V_{IP} = 1 V_{pp}/10 kHz)	%	0.28	0.3	0.31
Input referred noise @ 100 Hz	µV/$\sqrt{\text{Hz}}$		5.2	
Input referred integrated noise (100 Hz – 10 kHz)	µVrms		256	
Input referred offset (1 σ)	mV		5.2	
Area	mm^2		0.0024	

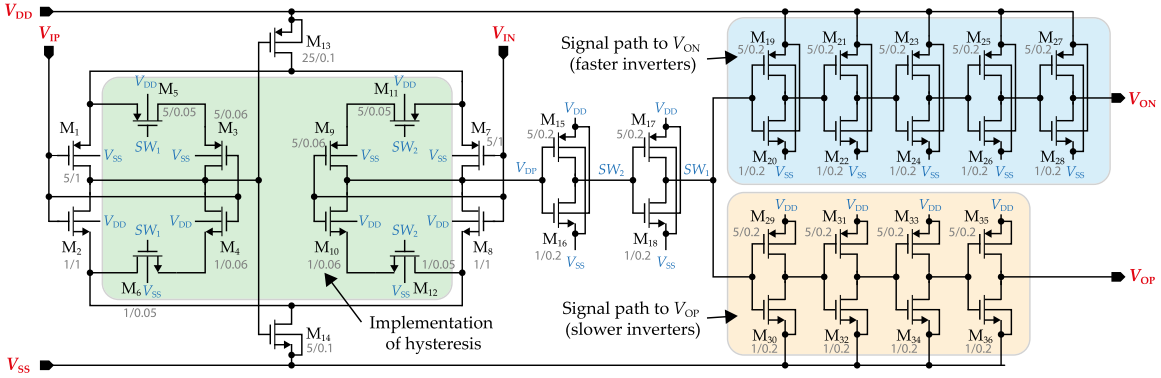

Fig. 9. A schematic of the proposed hysteresis comparator; all dimensions of MOSFETs are in units of µm, i.e. 5/0.2 = 5 µm/0.2 µm.

The differential pair consists of two inverters (M_1, M_2 and M_7, M_8) and two tail current switches, M_{13} and M_{14}, which are adaptively turned ON/OFF based on the input signal voltages. The threshold voltage of $M_1 - M_4$ and $M_7 - M_{10}$ is reduced by adjusting the back-gate voltage. When the positive input voltage (V_{IP}), increases, the drains of M_1 and M_2 fall and turn on M_{13} to a large current, which is sourced to the output node (V_{DP}) through M_7. During this condition, M_{14} is off. When the voltage, V_{IP}, decreases, M_{14} turns on and a large current is sunk through the output (node V_{DP}) via M_8. Hence, this circuit is capable of sourcing and sinking large currents without a large quiescent current.

The hysteresis is introduced into the circuit by using two additional transistor pairs, M_3, M_4 and M_9, M_{10}. The transistors M_5, M_6 and M_{11}, M_{12} then operate as switches that connect/disconnect the PMOS (M_3, M_9) or NMOS (M_4, M_{10}) transistor to the primary inverter, thus changing its threshold voltage. When the positive input voltage, V_{IP}, is above the threshold level (assume that V_{IN} is below), the transistors M_2 and M_7 are on, and therefore V_{DP} is in the high state, SW_2 in the low state, and SW_1 in the high state. The transistor M_6 is turned on, and M_4 is connected in parallel with M_2. The same situation occurs in the case of the switch M_{11}, which coupled M_7 and M_9. As a result, the circuit behaves analogously, as the input inverters have a higher W/L ratio in the transistors M_2, M_7 than M_1, M_8. This leads to a higher threshold level in the V_{IP}'s input inverter (M_1, M_2), and to a lower threshold level in the V_{IN}'s inverter (M_7, M_8). A similar situation can be described with opposite input signals when M_5, M_6, M_{10} and M_{12} are employed.

The comparator's threshold voltage without the hysteresis circuit is generally given by

$$V_{TH,X} = \frac{V_{DD} - \left|V_{THp}\right| + V_{THn}\sqrt{\frac{\beta_{n,X}}{\beta_{p,X}}}}{1 + \sqrt{\frac{\beta_{n,X}}{\beta_{p,X}}}}, \tag{20}$$

where X denotes the input part A (M_1 and M_2) or B (M_7 and M_8).

The parameter β is given by

$$\beta_{n,X} = k'_n \frac{W_n}{L_n} \; or \; \beta_{p,X} = k'_p \frac{W_p}{L_p}. \tag{21}$$

When the hysteresis circuit composed of M_3-M_6 and M_9-M_{12} is considered, the comparator's positive hysteresis voltage, denoted as V_{Hp}, can be obtained from Eq. (20) by modifying the β from Eq. (21), which can be rewritten as

$$\beta_{n,A} = k'_n \left(\frac{W_2}{L_2} + \frac{W_4}{L_4}\right), \tag{22}$$

for the input part A and

$$\beta_{n,B} = k'_p \left(\frac{W_7}{L_7} + \frac{W_9}{L_9}\right), \tag{23}$$

for the input part B.

The parameters β_n and β_p for the negative hysteresis voltage can be derived similarly. Nevertheless, the proposed comparator uses symmetrical hysteresis; hence, β_n and β_p will have the same values as indicated in Eqs. (22) and (23), respectively.

The SW_1 output node is followed by two signal paths to create a fully differential output. This, however, requires an extra inverter in the path to V_{ON}, introducing the V_{ON} and V_{OP} mutual timing asymmetry into the circuit if all of the inverters have identical delays. To eliminate the nonidentical time delay from SW_1 to V_{OP} and from SW_1 to V_{ON}, tuning the transistors' back gate electrode voltage of the invertors in the path SW_1 to V_{ON} is used to achieve a lower inverter's delay. As a result, an identical time delay of both paths is achieved with a minimum impact of the PVT variations.

The simulated propagation time delay and the DC transfer characteristics of the comparator are shown in Figs. 10 and 11. All the simulated parameters across the PVT corners are then summarized in Table 2.

The load capacitance, C_L, mentioned in Table 2 consists of the gate capacitance of an input MOSFETs in the DAC circuit and the assumed input capacitance of the following circuit that will be connected to the ADSM's output.

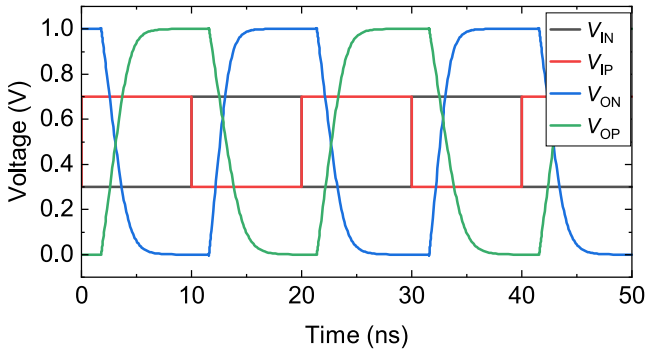

Fig. 10. The timing diagram of the comparator.

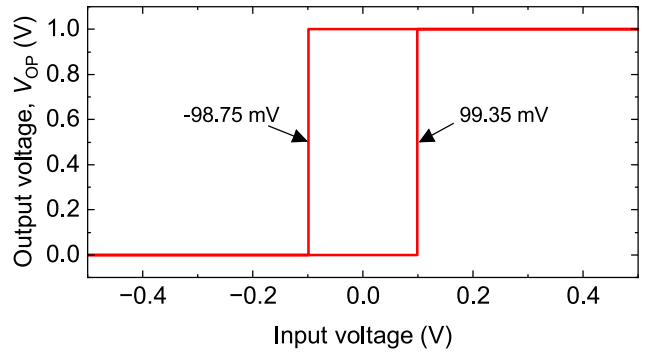

Fig. 11. The simulated DC transfer characteristic of the comparator.

Table 2
Simulated parameters of the comparator.

Parameter	Unit/Condition	Min	Typ	Max
Hysteresis	mV			
L to H		83.75	99.35	121.6
H to L		83.35	98.75	121.1
Slew rate	V/µs			
$V_{OP}(rising)$	200 mV input	259	309	361
$V_{OP}(falling)$	step with 100 mV	221	261	289
$V_{ON}(rising)$	overdrive	332	397	459
$V_{ON}(falling)$	C_L = 1 pF	264	313	357
Time delay	ns			
$V_{OP}(rising)$	200 mV input	2.91	3.13	3.59
$V_{OP}(falling)$	step with 100 mV	2.89	3.15	3.55
$V_{ON}(rising)$	overdrive	2.43	2.59	2.81
$V_{ON}(falling)$	C_L = 1 pF	2.88	3.07	3.49
Power cons.	nW at 100 kHz	111	172	428
Input offset	mV (1 σ)		8.76	
Area	mm^2		0.000528	

4.3. Digital-to-analog converter (DAC)

The 1-bit DAC used in the proposed ADSM is shown in Fig. 12.

The circuit's core comprises six transistors, of which four are switches (M_1 – M_4) and two are current sources (M_6 and M_7). The current sources are common for both of the DAC's outputs. Thanks to this solution, the effect of the matching error affecting the duty cycle of the generated signal is minimized. Consequently, a significantly lower leakage current through the off state switch is achieved (14.5 fA vs 600 fA in typical conditions) due to its V_{GS} (or V_{SG}) being negative.

The circuit of the DAC contains digital trimming of the I_{DAC}. This feature is implemented into the circuit to compensate for the of the transconductor's G_m variation, which mostly depends on the absolute value of the resistance R_D. In addition, G_m is affected by the manufacturing process and mismatch errors of the other components in

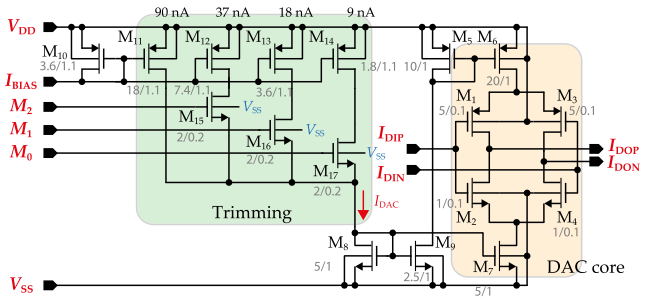

Fig. 12. A schematic of the DAC circuit; all dimensions of MOSFETs are in units of µm, i.e. 5/0.1 = 5 µm/0.1 µm.

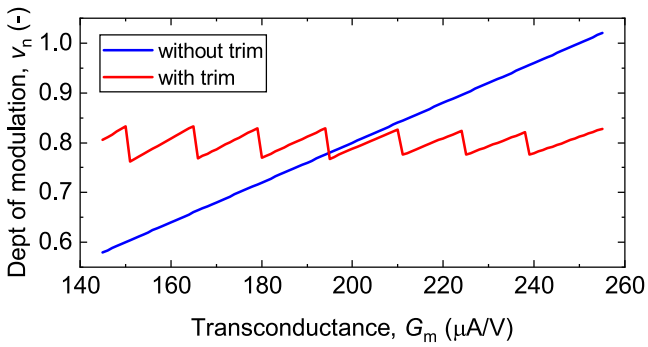

Fig. 13. The dependence of the modulation depth (v_n) on the transconductor's G_m: with and without trimming.

the transconductor when the G_m's overall variance can be up to approx. ±20%. Together with the I_{DAC} errors, the depth of the modulation (v_n) error can reach up to ±26% for the standard deviation of 3 σ. A large positive deviation of v_n can cause premature overload in the ADSM, resulting in a significant *SNDR* drop. A negative deviation of v_n does not cause a large drop in the *SNDR* as in the previous case; however, the ADSM's dynamic range is reduced. In order to compensate for v_n across the process corners and mismatch errors, the required I_{DAC} range was experimentally determined from analyses to be ≈90 – 160 nA, when the I_{DAC} of 125 nA is valid for the typical process parameters (see Section 3.2). The DAC's bias circuit consists of four current sources (M_{11} - M_{14}); the current source M_{11} (90 nA) is permanently connected to the circuit. The three remaining sources compose binary-weighted current sources provided an additional 64 nA that can be connected to the DAC, with the minimum step amounting to 9 nA (*LSB*). The bias current corresponding to the typical process parameters is slightly different than mentioned before (127 nA instead of 125 nA) due to *LSB* of DAC. This current should be set by pull-up and pull-down components when no trimming is employed. As is obvious from Fig. 13, the error of the trimmed v_n decreases as G_m increases because the *LSB* has a larger percentage ratio at lower values of G_m than at higher ones. It is also important to note that the G_m error shown on the X-axis incorporates the I_{DAC} error.

As presented in Fig. 13, the maximum error before trimming is v_n ±0.22, and after trimming 0.035. The Total area of the DAC is 0.000140 mm^2.

Parameters of the DAC are summarized in Table 3.

5. Post-layout simulations

The proposed ADSM was designed and simulated in the STMicroelectronics 28 nm FDSOI technology with a 1 V supply voltage. Based on the ADSM's layout shown in Fig. 14, Calibre PEX was used to generate an equivalent ADSM schematic (post-layout model) containing the parasitic capacitance and resistance. Based on the post-layout

Table 3
Simulated parameters of the DAC.

Parameter	Unit	Min	Typ	Max
Output current range	nA	90	127	385
Output current error	%			3
LSB	nA		9	
Power consumption	nW	243		403
Area	mm^2		0.00014	

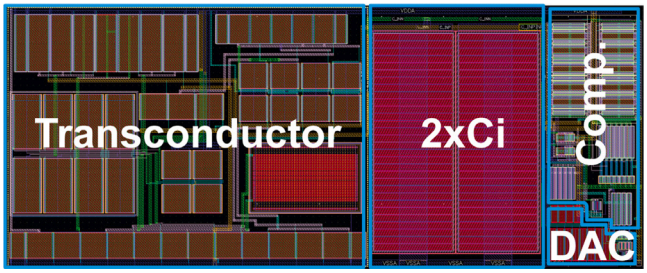

Fig. 14. The layout of the designed ADSM with the dimensions of 101.8 µm × 41.5 µm.

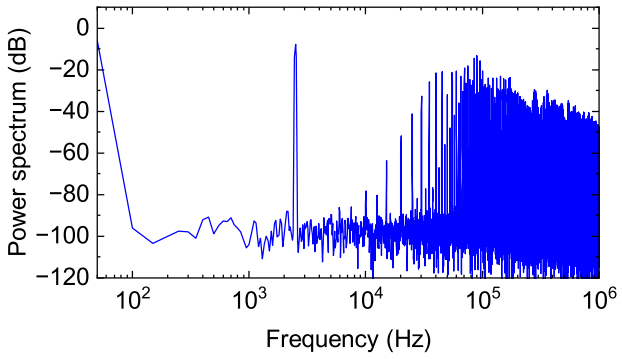

Fig. 15. The simulated output spectrum of an 2.5 kHz sinusoidal input with a 0.5 V amplitude.

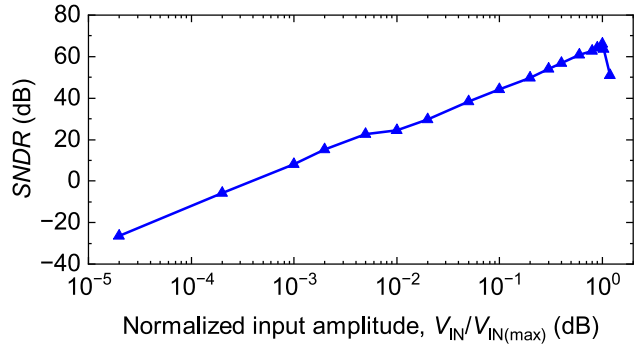

Fig. 16. The simulated *SNDR* vs. the normalized input amplitude.

model, the circuit was characterized over the process corners and the commercial temperature range of 0 °C to 70 °C. The current I_{DAC} is set to 127 µA by default, except for cases where premature overload and a significant *SNDR* reduction occur.

In Fig. 15, the simulated spectrum of the ADSM for the maximum possible input signal amplitude of 500 mV is exposed. The applied input signal frequency of 2.5 kHz is used; then, the potential third harmonic component of the input signal enters the 10 kHz bandwidth and may degrade the *SNDR*. The simulated peak *SNDR* and spurious-free dynamic range (*SFDR*) are 66.2 dB and 76.6 dB, respectively; this corresponds to a resolution of 10.7-bit. The simulated *SNDR* value is very close to that calculated according to Eq. (11), which is 65.5 dB.

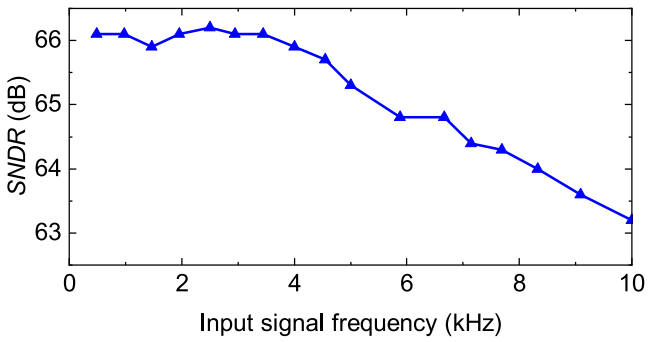

Fig. 17. Simulated *SNDR* vs. input signal frequency.

Table 4
The simulated main parameters over PVT variations.

Temperature	°C	0	27	70
SNDR	dB	65.7	66.2	63.02
Limit cycle freq., f_C	kHz	83.75	99.35	121.6
Depth of modulation, v_n	–	0.81	0.8	0.77
Magnitude at frequency f_{in}	dB	−13.82	−13.98	−14.27
SFDR	dB	80.01	76.66	66.37
Power supply	V	0.9	1	1.1
SNDR	dB	64.78	66.2	65.77
Limit cycle freq., f_C	kHz	100.4	99.35	81.55
Depth of modulation, v_n	–	0.8	0.8	0.8
Magnitude at frequency f_{in}	dB	−14.24	−13.98	−13.18
SFDR	dB	71.65	76.66	73.41
Process corner		$C_{min}R_{min}$	$C_{min}R_{min}$ [a]	$C_{min}R_{max}$
SNDR	dB	39	62.54	63.9
Limit cycle freq., f_C	kHz	103.4	119.85	103.4
Depth of modulation, v_n	–	0.95	0.82	0.7
Magnitude at frequency f_{in}	dB	−12.52	−13.81	−15.26
SFDR	dB	39.64	67.27	73.72
Process corner		$C_{max}R_{min}$	$C_{max}R_{min}$ [a]	$C_{max}R_{max}$
SNDR	dB	32.07	63.65	63.7
Limit cycle freq., f_C	kHz	88.8	102.95	88.8
Depth of modulation, v_n	–	0.95	0.82	0.7
Magnitude at frequency f_{in}	dB	−12.52	−13.8	−15.26
SFDR	dB	32.6	70	75.42

[a] Trimming applied ($I_{DAC} = 90nA + 37nA + 18nA$).

In Fig. 16, the resulting *SNDR* versus the normalized input signal $V_{IN}/V_{IN(max)}$ is visualized. The simulated dynamic range and the peak *SNDR* are 87 dB and 66.2 dB, respectively.

The graph in Fig. 17 shows the *SNDR* versus the input signal frequency when the maximum input signal amplitude is used. Apparently, the *SNDR* decreases with increasing frequency; this phenomenon is more evident in the first-order ADSMs than in the second-order ones, as presented in [24].

To expose the circuit robustness against PVT variations, we show the results of the corner analysis in Table 4. As can be seen, the transconductor's G_m deviation, caused mainly by the R_D deviation, has the most significant impact on the *SNDR*. While the Rmax corner results in a minimal reduction of the *SNDR*, the Rmin one produces a premature overload and a significant reduction of the *SNDR*. In this second case, I_{DAC} trimming is applied.

Let us now view the results in greater detail. For the temperature and supply voltage variations, the f_C registers some fluctuation; the variation of v_n, however, is insignificant. In the case of a minimum temperature (0 °C), v_n increases by 0.01 only. A substantial increase in v_n occurs at the process corner with the minimum value of R_D (R_{min}). Here, the G_m of the transconductor reaches its maximum value, leading to an increase of v_n to 0.95; the ADSM overloads; and the *SNDR* is reduced to values below 40 dB. As is obvious from (6), v_n can be

Table 5
Comparing the performance with previously published ADSMs.

Parameter	This work	[25] 2020	[24] 2017	[20] 2019	[26] 2015	[14] 2016
Technology	28 nm FDSOI	180 nm	130 nm	180 nm	130 nm	130 nm
Supply voltage, V_{DD}	1 V	1 V	0.25 V	0.3 V	0.25 V	3.3 V
Order	1	2	2	1	1	1
Modulator frequency, f_C	100 kHz	848 kHz	1.73 kHz	2.64 kHz	630 Hz	–
Bandwidth, f_{BW}	10 kHz	10 kHz	70.2 Hz	62 Hz	30 Hz	2 MHz
$SNDR$	66.2 dB	92 dB	67.3 dB	53.3 dB	58 dB	47 dB
$SFDR$	76.66 dB	–	68.12 dB	–	–	54 dB
Dynamic range, DR	87 dB	112 dB	67.31 dB	53.8 dB	58 dB	–
Power dissipation, P_{diss}	4.1 µW	290 µW	30 nW	37 nW	28 nW	495 µW
FoM_1	159	187	161	146	148	–
FoM_2	0.16 pJ/step	0.45 pJ/step	0.11 pJ/step	0.79 pJ/step	0.8 pJ/step	0.67 pJ/step
Area	0.0042 mm^2	0.054 mm^2	–	0.141 mm^2	0.141 mm^2[a]	0.00099 mm^2
Obtained results	Post-layout	Post-layout	Simulated	Measured	Measured	Measured

[a] External passive components required.

reduced by increasing the I_{DAC}. Thus, the I_{DAC} is increased via digital trimming to become 145 µA instead of 127 µA. This step reduces v_n to the default value ($v_n = 0.8$); simultaneously, f_C increases, producing a negligible increase in the power consumption.

Table 5 presents a comparison of the proposed ADSM with other published ADSMs, with two commonly used figures of merit (FoM) defined as

$$FoM_1 = DR + 10\log\left(\frac{f_{BW}}{P_{diss}}\right), \tag{24}$$

and

$$FoM_2 = \frac{P_{diss}}{2^{ENOB} 2 f_{BW}}, \tag{25}$$

better performance is indicated in the ADSMs by larger FoM_1 and lower FoM_2 values.

The presented ADSM is compared with three ultra low-voltage (ULV) ADSMs, one being a fast ADSM with the signal bandwidth of 2 MHz and the other a second-order ADSM with a corresponding 10 kHz bandwidth. The latter exhibits good parameters; however, it suffers from high power consumption and a high silicon area. The modulator also employs a 1 V power supply with a rail-to-rail input signal range. Nevertheless, this is achieved using a conventional RC integrator with an operational amplifier whose input is kept at virtual ground. The approach results in the input signal source being loaded by the resistors in the integrator, and, in the case of applications such as biomedical signal processing, an input voltage buffer is required. All these disadvantages are not inherent in the proposed ADSM. As can be seen in Table 5, the presented ADSM offers very good performance across the entire spectrum of monitored parameters, featuring a very low silicon area, high $SNDR$, high FoM_1, and low FoM_2. Besides the monitored parameters, the limit cycle frequency (modulator frequency) is designed to be only ten times higher than f_{BW}. This results in the lowest CBR (see Eq. (4)).

6. Conclusion

In this article, a novel first-order ADSM designed in the 28 nm FD-SOI technology has been presented. The design on the transistor level was preceded by mathematical calculations and advanced circuit modeling in MATLAB. The approach allows setting the requirements for the analog blocks and determining the effective value of the limit cycle frequency; this results in a CBR of only 5. Employing the FD-SOI technology enables designers to produce improved rail-to-rail transconductor and hysteresis comparator structures. Consequently, the resolution of 10.7 bits was achieved at the power consumption of 4.1 µW. The results were verified across the PVT corners via a post-layout analysis. The total circuit area is only 0.0042 mm^2. The ADSM can be used in not only biomedical signal acquisition applications covering the entire spectrum of biosignals but also, for example, vibration sensor signal postprocessing.

CRediT authorship contribution statement

Vilem Kledrowetz: Writing – review & editing, Writing – original draft, Validation, Methodology, Investigation, Formal analysis, Conceptualization. **Lukas Fujcik:** Writing – review & editing, Project administration, Investigation. **Roman Prokop:** Writing – review & editing, Validation, Software. **Jiri Haze:** Writing – review & editing, Validation.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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