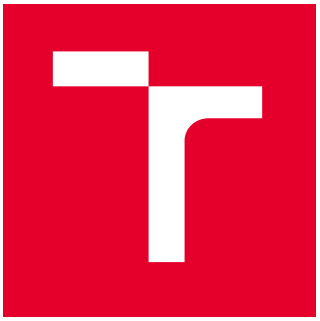

BRNO UNIVERSITY OF TECHNOLOGY

VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ

FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION

FAKULTA ELEKTROTECHNIKY
A KOMUNIKAČNÍCH TECHNOLOGIÍ

DEPARTMENT OF MICROELECTRONICS

ÚSTAV MIKROELEKTRONIKY

FUNCTION GENERATOR WITH VOLTAGE AND CURRENT OUTPUT MODE

FUNKČNÍ GENERÁTOR S NAPĚŤOVÝM A PROUDOVÝM VÝSTUPEM

BACHELOR'S THESIS
BAKALÁŘSKÁ PRÁCE

AUTHOR — **Filip Pavlovič**
AUTOR PRÁCE

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VEDOUCÍ PRÁCE

BRNO 2025

VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ
FAKULTA ELEKTROTECHNIKY A KOMUNIKAČNÍCH TECHNOLOGIÍ

Bakalářská práce

bakalářský studijní program **Mikroelektronika a technologie**

Ústav mikroelektroniky

Student: Filip Pavlovič ***ID:*** 247056

Ročník: 3 ***Akademický rok:*** 2024/25

NÁZEV TÉMATU:

Funkční generátor s napěťovým a proudovým výstupem

POKYNY PRO VYPRACOVÁNÍ:

Navrhněte funkční generátor, který bude schopen pracovat jako proudový či napěťový zdroj. Požadované minimální parametry generátoru jsou 15 V amplituda výstupního napětí, 500 mA výstupní proud a 1 MHz šířka pásma. Generátor by měl být ve formátu zásuvné karty do rack systému a výstup generátoru je nutné galvanicky oddělit od zbytku systému. Zařízení navrhněte, realizujte a změřte jeho klíčové parametry.

DOPORUČENÁ LITERATURA:

According to recommendations of the sipervisor.

Termín zadání: 10.2.2025 ***Termín odevzdání:*** 5.6.2025

Vedoucí práce: Ing. Pavel Tomíček

doc. Ing. Pavel Šteffan, Ph.D.
předseda rady studijního programu

BRNO UNIVERSITY OF TECHNOLOGY
FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION

Bachelor's Thesis

Bachelor's study program **Microelectronics and Technology**

Department of Microelectronics

Student: Filip Pavlovič ***ID:*** 247056

Year of study: 3 ***Academic year:*** 2024/25

TITLE OF THESIS:

Function generator with voltage and current output mode

INSTRUCTION:

Design function generator, that will be able to to work as a voltage source or a current source. Required minimum parameters of the generator are 15 V output voltage amplitude, 500 mA output current and 1 MHz bandwidth. Generator should have a form factor of a plug-in card in a rack system. The output of the generator needs to be galvanically isolated from the rest of the rack. Design the device, realize it and measure its key parameters.

RECOMMENDED LITERATURE:

According to recommendations of the sipervisor.

Date of project specification: 10.2.2025 ***Deadline for submission:*** 5.6.2025

Supervisor: Ing. Pavel Tomíček

doc. Ing. Pavel Šteffan, Ph.D.
Chair of study program board

Abstract

The goal of this thesis is to design an arbitrary function generator with both voltage and current output mode. The generator is capable of functioning as a voltage or current source with enough power capability to be used as a power supply. The physical form is based on the Eurocard standard, with modifications that suit the needs of the project. The output signal is galvanically isolated from the rack system's ground, allowing the user to either offset the voltage/current or generate a signal independent of the target circuit's grounding potential. The device communicates via the RS485 protocol embedded in the card's connector with other devices connected to the rack and is controlled and configured using SCPI commands.

The thesis describes the theory of generating arbitrary signals, as well as the practical implementations of the selected method. Block diagrams will be presented for different modules of the device, as well as their schematics. Finally, all the necessary measurements are performed and documented.

Keywords

Waveform generation, AWG, arbitrary waveform generator, DDS, direct digital synthesis, lab equipment, card system, mixed signal.

Abstrakt

Cieľom tejto práce je navrhnúť generátor ľubovoľných funkcií s napäťovým alebo prúdovým výstupom. Generátor je schopný pracovať ako zdroj napätia alebo prúdu s dostatočným výkonom, aby umožňoval jeho použitie ako zdroj napájania. Fyzická forma je založená na štandarde Eurocard s úpravami, ktoré vyhovujú potrebám projektu. Výstupný signál je galvanicky oddelený od zeme rackového systému, čo umožňuje používateľovi generovať signál nezávislý od potenciálu uzemnenia cieľového obvodu. Zariadenie komunikuje prostredníctvom protokolu RS485, zabudovaného v konektore karty s ostatnými zariadeniami pripojenými k racku a je ovládané a konfigurované pomocou príkazov SCPI.

Táto práca popisuje teóriu generovania ľubovoľných signálov, ako aj praktické implementácie zvolenej metódy. Budú predstavené blokové schémy pre rôzne moduly zariadenia, ako aj ich schémy zapojenia. Nakoniec sú vykonané a zdokumentované všetky potrebné merania.

Rozšírený abstrakt

Testovanie elektronických obvodov a súčiastok sa často vykonáva pomocou generátorov frekvencií. Generátory ľubovoľného tvaru signálu (AWG) sú schopné produkovať nielen digitálne, ale aj analógové signály, ako sú sínusové, trojuholníkové, pílovité atď. s konfigurovateľnou frekvenciou a amplitúdou. Komerčne dostupné prístroje však nemajú dostatočný výstupný výkon a výstupy sú často obmedzené na ±10 V so slabou prúdovou kapacitou. Dôvodom je, že sú určené na použitie iba ako zdroje riadiacich signálov, ktoré z generátora odoberajú veľmi málo energie.

Cieľom tejto práce je navrhnúť AWG s galvanicky izolovaným výstupom schopným fungovať v napäťovom aj prúdovom režime, ktorý dokáže riadiť nielen odporové, ale aj kapacitné alebo indukčné záťaže bez rizika poškodenia zariadenia alebo zníženia kvality signálu. Jeho jedinečná schopnosť vytvárať prúdový signál je nevyhnutná pre riadenie citlivých polovodičových súčiastok, ako sú laserové diódy. Izolovaný výstup umožňuje používateľovi vložiť signál do ľubovoľného bodu cieľového obvodu a zabraňuje skratovaniu izolovaných zemných spojení alebo vytváraniu uzemňovacích slučiek v testovacom zapojení.

Hlavné parametre zariadenia sú:

1. Maximálna amplitúda napätia: 15 V.
2. Maximálny trvalý prúd: 0,5 A.
3. Maximálny špičkový prúd: 1 A.
4. Maximálna výstupná frekvencia: 1 MHz.
5. Komunikačný protokol: SCPI.

Bakalárska práca sa zameriava na teóriu metód generovania signálov, praktický návrh rôznych častí zariadenia a po finálnej montáži na jeho testovanie, ktoré bude slúžiť ako dôkaz jeho skutočných parametrov. Zariadenie je najprv navrhnuté pomocou blokovej schémy a potrebné bloky sú následne nahradené príslušným obvodom.

Klíčová slova

Generovanie priebehu, AWG, generátor ľubovoľných priebehov, DDS, priama digitálna syntéza, laboratórne vybavenie, kartový systém, zmiešaný signál.

Bibliographic citation

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Author’s Declaration

Author:	*Filip Pavlovič*
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Paper type:	*Bachelor’s Thesis*
Academic year:	*2024/25*
Topic:	*Function generator with voltage and current output mode*

I declare that I have written this paper independently, under the guidance of the advisor and using exclusively the technical references and other sources of information cited in the project and listed in the comprehensive bibliography at the end of the project.

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Brno, June 2 ----------

author’s signature

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Brno, November 2, 2024 ----------

Author’s signature

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INTRODUCTION

Testing of electronic circuits and components is often performed with the help of frequency or waveform generators. Arbitrary waveform generators (AWGs) are capable of producing not only digital, but also analog signals such as sine, triangle, sawtooth etc. with configurable frequencies and amplitudes. However, commercially available instruments lack output power capabilities. Their outputs are often limited to ±10 V with a poor current capability. The reason for that is because they're meant to be used as control signal sources, which draw very little power from the generator.

The goal of this thesis is to design AWG with galvanically isolated high-power voltage or current output mode, capable of driving not only resistive, but also capacitive or inductive loads without the risk of damaging the AWG or decreasing signal quality. Its unique ability to output current signal is essential for driving sensitive semiconductor components such as laser diodes. Isolated output acts as differential and allows user to inject signal into any point of the target circuit and prevents from shorting isolated grounds or creating ground loops in his test setup. In this bachelor thesis, signal generation methods are described and based on the theory the design of the custom waveform generator is presented.

The main parameters of the device are:

1. Maximum voltage amplitude: 15 V
2. Maximum continuous current: 0.5 A
3. Maximum peak current: 1 A
4. Maximum output frequency: 1 MHz
5. Communication protocol: SCPI

The bachelor thesis will focus on the theory of signal generation methods, practical design of different parts of the device, and after the final assembly, its testing, which will act as proof of its real parameters.

1. THEORY OF SIGNAL GENERATION

The chapter will focus on the theory of signal generation and their conversion from digital to analog values. Multiple methods will be presented, and in the end the most suitable one will be selected.

1.1 Programmable clock generators and conditioners

The important component of any signal generator is a clock generator. It is either responsible for controlling the output frequency of the device or providing a precise and stable timing reference for other modules of signal generator.

The following chapters will discuss the common types of programmable clock generators and conditioners as well as their advantages and disadvantages. It is assumed that all clock generator types are already equipped with a fixed frequency oscillator.

1.1.1 Programmable frequency divider

As one of the simplest methods of digitally controlled clock generation is the programmable frequency divider. As shown in Figure 1.1, it is composed of a binary counter with either a multiplexer, that routes the appropriate bit of the counter to the device's output or a comparator, which resets the counter when its value matches the divider control input.

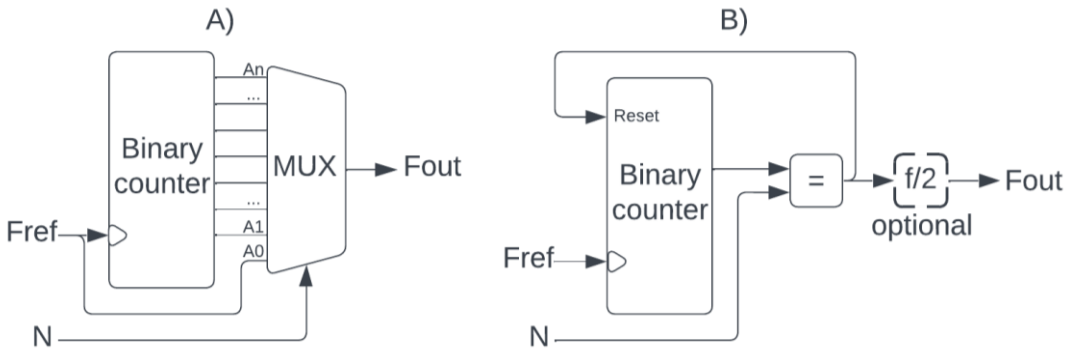

Figure 1.1: A) divide by 2^N counter B) divide by N counter

The first version of divider (type A) is simpler to implement. No matter what the input duty cycle is, its output signal is exactly 50%, except when N is 0, where the output is tied directly to the input, then the duty cycle is the same as on the input. The main downside is the poor divider value resolution, dividing the input frequency by only multiples of 2.

Version B) fixes this limitation by introducing a digital comparator. When the value of the counter matches the divider value N, it outputs a logic 1, resetting the counter. This means that the setup generates short pulses with the desired frequency, where the pulse

width depends on the propagation delay from the comparator to reset input of counter and the time it takes to reset the counter. This signal type is commonly referred to as PFM or pulse frequency modulation. This means that the duty cycle will vary with set frequency. This problem can be tackled by an optional divide-by-2 counter placed between the comparator and device's output. Note that this modification will reduce the minimum divider value to 2.

As the name suggests, the programmable frequency dividers can only down-convert the frequency. Because of this limitation, the divider is not used in this project directly, but it serves as a crucial component of the following devices.

1.1.2 Phase locked loop

A Phase locked loop (PLL) is a device capable of generating digital or analog signals, allowing the user to control its frequency. It is a control system that compares the phases of reference input clock and feedback signal and alters its output frequency accordingly. The term "phase lock" refers to the state where both phases match and the PLL outputs signal with desired frequency and phase.

The PLL has become an essential component in modern instruments, used not only for clock multiplication but jitter removal or duty cycle correction. Because PLL has its own oscillator, opposite to frequency divider, it is capable of frequency up-conversion. Generally, it consists of 5 parts: Reference clock, voltage-controlled oscillator (VCO), feedback divider/counter, phase detector (or phase comparator) and low pass filter [1].

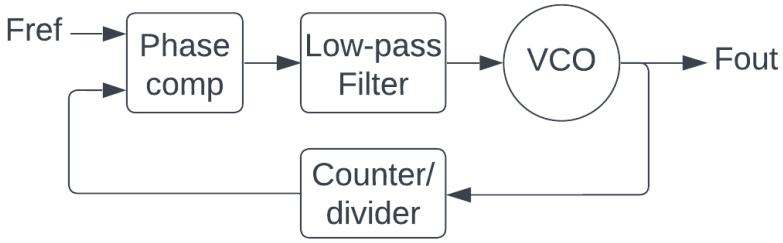

Figure 1.2: Basic PLL block diagram [1]

The phase detector compares phases of reference clock F_{REF} and the output divided by the N counter. It basically works as an error amplifier. Its output is often a charge pump that increases voltage if the phase of the feedback is lacking behind the phase of F_{REF} and decreases otherwise. The low pass filter is used to smooth out this output, which reduces the jitter of the output frequency. The VCO is basically a voltage to frequency converter. The feedback divider/counter is responsible for setting the output frequency, which is given by the following formula.

$$f_{ref} = \frac{f_{out}}{N} \rightarrow f_{out} = f_{ref} \cdot N \quad (1)$$

Where f_{ref} is the frequency of the input reference clock, f_{out} is the output frequency and N is the frequency divider integer value. Because the N is an integer, the minimum output frequency step is f_{ref}. This topology is called Integer-N PLL [18].

If we wanted to improve the output frequency resolution of the Integer-N PLL, we would have to decrease the f_{ref} and increase N to keep the output frequency the same. This modification will improve the resolution, but it will also increase the output phase noise by 20·log(N) dB [18]. This is caused by the transient noise generated by the phase comparator, which will reduce the output frequency and phase stability.

To improve the frequency resolution, the integer divider can be replaced by a fractional divider. The fractional divider component is composed of regular integer divider, but its control value is being constantly switched from N to N+1 by a state machine in such a manner that the effective divider value lies between N and N+1. For example, if the divider value is set to 5, and the time spent in the N+1 state is 80% of the state machine switching period, the effective divider value is then 5.8. This modification of the Integer-N PLL is called a Fractional-N PLL [18].

Compared to Integer-N PLL, the only downside of Fractional-N PLLs is the added logic responsible for the switching of divider values.

1.1.3 Digital phase locked loop

DPLLs were designed to enhance the integration of PLLs into digital circuits. The output of the phase comparator is now exclusively digital and is fed into a digital low-pass filter, either of the FIR or IIR type. The filtered control signal is then converted into analog voltage through a DAC and fed into the VCO.

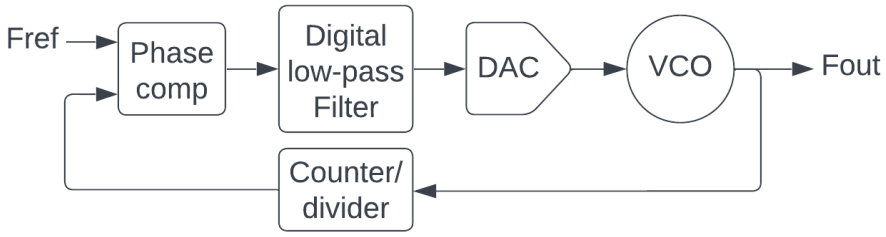

Figure 1.3: DPLL internal block diagram [17]

In Figure 1.3, VCO is the only analog component in this setup and can be attached externally. The DPLL contains less analog circuitry without any major drawbacks if DAC with high resolution is selected.

1.1.4 All-digital phase locked loop

The main downside of standard PLLs and DPLLs is that their structure contains analog components. This prevents their usage in all-digital ASICs, nor can their structure be implemented in an FPGA.

To address these limitations, an ADPLL was developed. While the basic principle of PLL remains, all analog blocks are replaced by their digital counterparts.

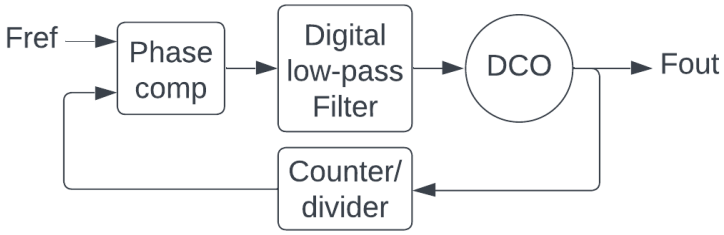

Figure 1.4: ADPLL internal block diagram [17]

Figure 1.4 shows the diagram of an all-digital PLL. When compared to DPLL, the main difference is the replacement of DAC and VCO with a digital controlled oscillator (DCO). Avoiding analog components also ensures superior noise immunity of the device. This architecture is commonly found in FPGAs and SoCs.

1.1.5 Numerically controlled oscillator

Numerically controlled oscillator or NCO is another type of all-digital, digitally controlled clock generator. Similar to the simple frequency dividers, it can only down-convert the input frequency. The NCO's main component is the phase accumulator, composed of a register and an adder (Figure 1.5).

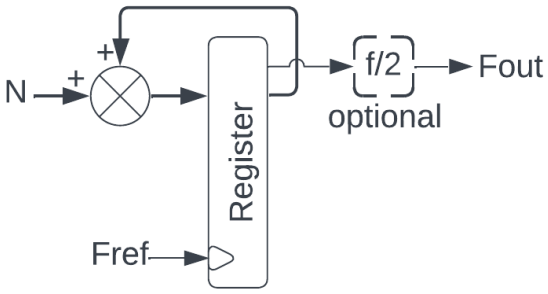

Figure 1.5: NCO block diagram

Unlike regular counters, which increase their output value by one for every clock pulse, a phase accumulator is incremented by the control value N. The width of the register is larger than the width of control value N by 1 bit. This allows the storage of the carry bit in the most significant bit of the register when the sum exceeds the bit width of the control value N and overflows. This carry bit is used as the raw output of the NCO.

Note that this output has a constant pulse width of $1/f_{ref}$, therefore it operates in PFM mode. A fixed 50% duty cycle can be achieved by placing a 1-bit counter between the register and the output.

The overflow period specifies the output frequency and is given by the following formula [19].

$$T_{OF} = \frac{1}{f_{out}} = \frac{2^M}{f_{ref} \cdot N} \rightarrow f_{out} = \frac{N}{2^M} \cdot f_{ref} \quad (2)$$

Where f_{ref} is the frequency of the input reference clock, f_{out} is the output frequency, N is the frequency control value and M is the bit width of the control value. The formula works only for PFM mode, meaning that for the constant duty cycle mode, the output frequency is halved.

Despite the M and N being integers, the NCO can divide the frequency by a fractional number. This is a significant advantage over the frequency dividers. To achieve a finer frequency resolution, the bit width of M can be increased.

1.2 Waveform generators

While chapter 1.1 discussed the clock generation options, this chapter will take use of them and supplement a functional block that will convert the raw clock signal into an analog or digital waveform.

1.2.1 Frequency synthesized analog function generator

The frequency synthesized analog function generator belongs to the simplest waveform shaping devices. It takes the already existing clock signal and transforms it into the 3 most used waveforms: sine, square and triangle.

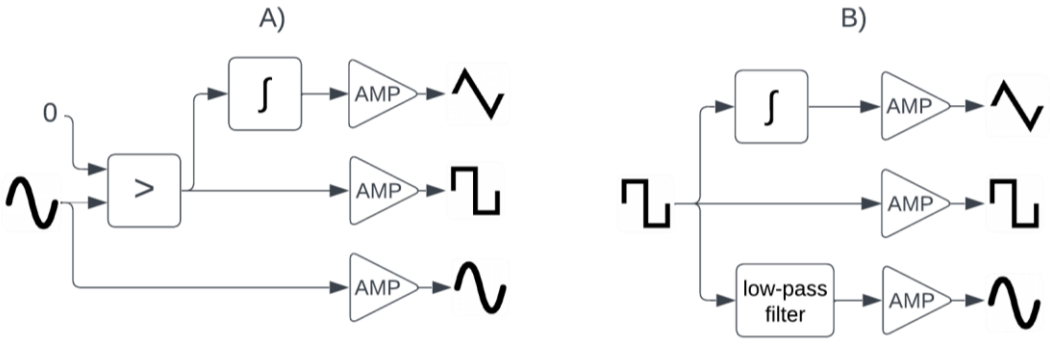

Figure 1.6: Block diagrams of A) sine input and B) square input FSAFG

Figure 1.6 shows the composition of FSAFG with both sine and square clock input. All output waveforms inherit the frequency of the clock.

In case A, where the input is a sine wave, it must first be converted into a square wave. This is achieved by using an analog comparator with a compare threshold of 0 V. Next, the square wave is fed into an analog integrator, which converts it into a triangle wave. Since square waves have constant absolute value with alternating polarity, integration

will result in a linear slope that is rising or falling depending on the square wave's polarity.

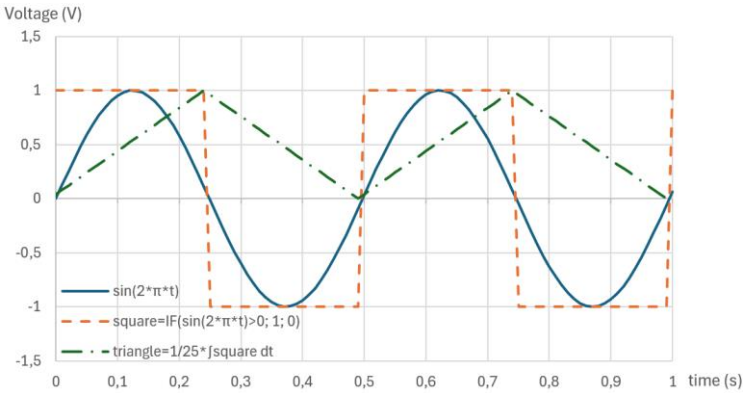

Figure 1.7: Simulation of output shapes for input sine wave

Figure 1.7 shows the simulation of the output shapes. Note that the triangle wave needs amplitude correction. As the frequency of input clock increases, the slope coming from the integrator will have less time to rise and fall, resulting in triangle wave's amplitude decrease.

Case B, where the input is square wave, works in similar fashion. The square is again integrated into a triangle wave. The main difference is that now we need to convert the square wave into a sine wave. This is commonly achieved by filtering the harmonics frequencies of the square wave with low-pass filter.

While case B is more convenient because majority of programmable clock generators output a square wave, its main downside is that a tunable low-pass filter is needed.

It is obvious that the main limitation of FSAFG is poor output waveform selection. This is why it is replaced by systems from the following chapters. However, the main advantage is that this system doesn't need DAC, resulting in low output noise.

1.2.2 Point-per-clock

The PPC is an arbitrary waveform generation method that uses digital circuitry to generate a stream of data representing different points of the waveform in time.

It is made of a binary counter that is being clocked by a reference clock, a memory block containing the waveform samples and a DAC.

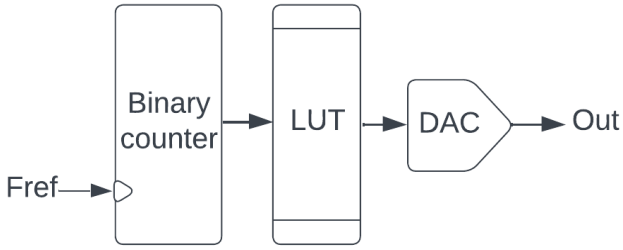

Figure 1.8: Simplified PPC generator block diagram

The memory that stores the samples effectively behaves like a mathematical function: the address input of the memory represents the input variable, in this case discrete time, and the data output corresponds to the amplitude point at that time. is often referred to as a lookup table (LUT).

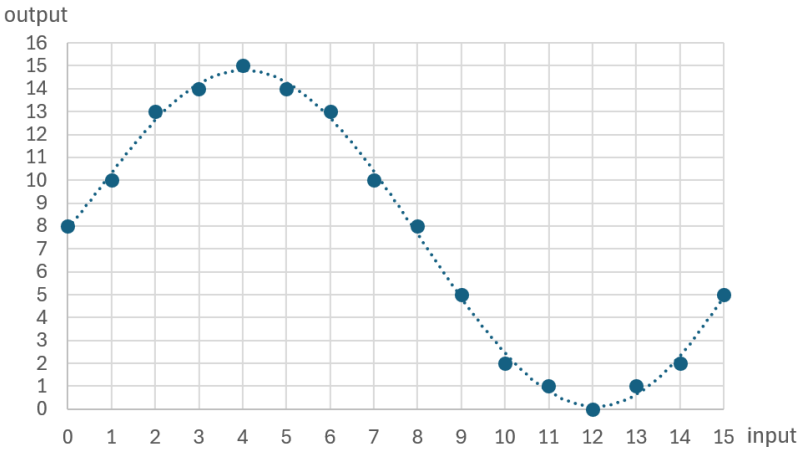

Figure 1.9: 4-bit lookup table example

Figure 1.9 shows a graph of simple sine wave lookup table, where the X axis represents the input values and Y axis the output LUT's output.

For each clock pulse, the counter increments its value by 1 and selects a new sample of the waveform from the LUT memory. It is important that the lookup table contains an integer number of wave periods, because when the counter overflows and wraps back to zero, it will allow the waveform to be seamlessly repeated. The selected sample is then turned into an analog voltage by the DAC. The PPC system's output frequency depends on the counter's overflow period and is given by the following formula [20].

$$T_{OF} = \frac{1}{f_{out}} = \frac{2^M}{f_{ref}} \rightarrow f_{out} = \frac{f_{ref} \cdot P}{2^M} \quad (3)$$

Where f_{ref} is the frequency of the input reference clock, f_{out} is the output frequency and M is the bit width of the counter and LUT memory address. For example, if we have an 8-bit lookup table with 256 sample values of one wave period and the maximum frequency of the circuit is 1 MHz, then the maximum producible output frequency would be 1 MHz / 256 = 3.906 kHz [20].

To further increase the output frequency beyond this limit, the sample count must be sacrificed. Also, the output frequency step size matters purely on the clock sources resolution.

1.2.3 Direct digital synthesis

"Direct digital synthesis (DDS) is a method of producing an analog waveform—usually a sine wave—by generating a time-varying signal in digital form and then performing a digital-to-analog conversion" [5]. The working principle of a direct digital synthesizer shares some similarities with PPC: it also uses a LUT memory to store the waveform data and a DAC to convert them into an analog signal. Chapter 1.2.2 provides more detailed insight into the functionality of a LUT.

The difference lays in how the DDS accesses the LUT memory. While PPC uses simple counter with variable clock, the DDS uses a phase accumulator, clocked by a fixed frequency clock [20].

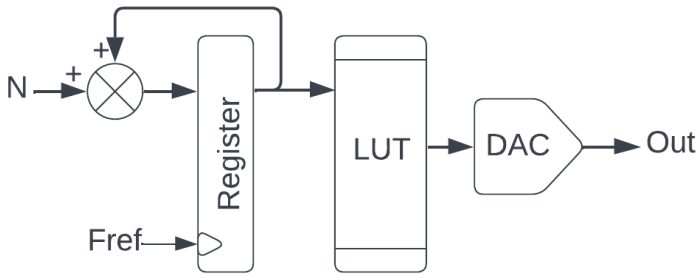

Figure 1.10: DDS block diagram

Figure 1.10 shows the block diagram of a direct digital synthesizer. The lookup table is connected to the output of a phase accumulator, functioning similarly to the NCO described in chapter 1.1.5. However, instead of using only the most significant bit of the register, multiple bits are used to address the table. This means that the output of phase accumulator isn't just a 1-bit clock signal, but a data stream that resembles a sawtooth wave. The frequency of the sawtooth wave, and therefore the output waveform, is the same as the frequency at which the phase accumulator overflows, given by the following formula [5].

$$\mathrm{T_{OF}} = \frac{1}{f_{out}} = \frac{2^M}{f_{ref} \cdot \mathrm{N}} \rightarrow f_{out} = \frac{\mathrm{N}}{2^M} \cdot f_{ref} \tag{4}$$

The same formula applies as for the NCO: f_{ref} is the frequency of the input reference clock, f_{out} is the output frequency, N is the frequency control value and M is the bit width of the control value.

Assuming that the bit width of LUT input is small relative to the size of the phase accumulator register, if the control value N is small and its value is in multiples of 2, the phase accumulator's output and thus the LUT's address will slowly increase by 1 every few clock cycles and no samples will be skipped. However, when a higher output frequency is needed, the value of N increases, and the LUT's address will increment by a larger values than 1, which results in sample skipping.

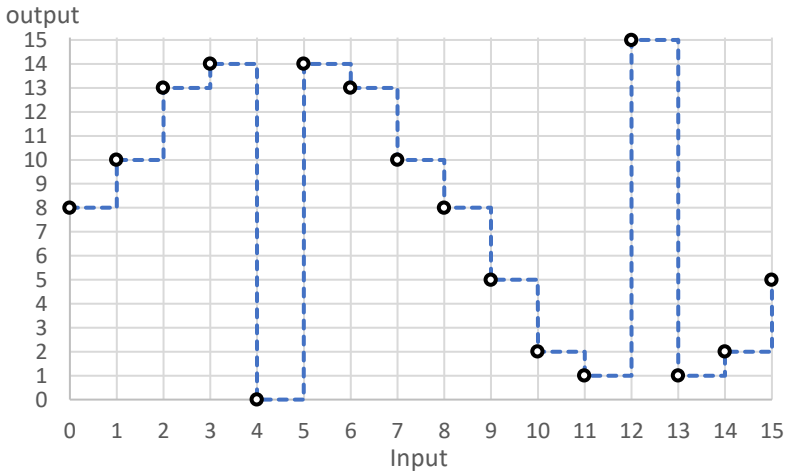

Figure 1.11: Graph of unsuitable waveform for DDS

Figure 1.11 shows the content of LUT loaded with unsuitable signal for DDS in a graph. As an example, a modified sine wave, whose peak values have inverted polarity, is used to demonstrate the impact of sample skipping.

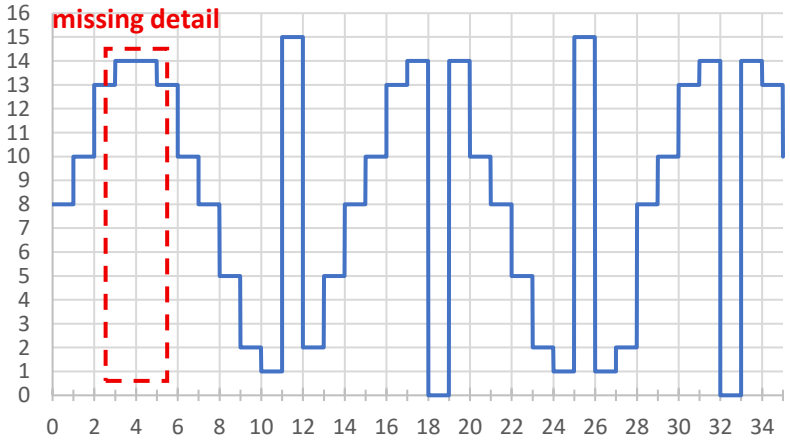

Figure 1.12: DDS output with skipped detail

The DDS is configured with a control value that is not a multiple of 2 and the output is shown in Figure 1.12. Occasionally, a sample of the waveform is skipped, which is harder to notice for a simple sine, resulting in a slightly steeper incline or decline, but with the added one-sample pulse, the change far more is noticeable. At lower frequencies, the pulse will disappear from a few periods, but as the frequency increases, at some point, the pulse will cease to exist.

At this point the output signal will start to distort, and small details of the waveform will disappear from the generator's output. The jitter of the output will also drastically increase.

When compared to PPC, DDS is easier to implement and features better and faster control of the output frequency, making it suitable for frequency and phase modulators, while suffering from increased output jitter, distortions and loss of some details of the waveform [20].

1.3 Digital to analog converters

A crucial part of any digital signal generator is the DAC. The purpose of this device is to convert the input digital signal into an analog value, often current or voltage. This chapter will present some popular DAC architectures as well as their advantages and disadvantages.

1.3.1 String DAC

String DAC or Kelvin divider DAC is a type of voltage output digital to analog converter that is composed of many resistors in series with equal values, referred to as a string, that creates a voltage divider, dividing the reference voltage.

Different taps of the divider correspond to different division ratios. An array of switches selects one of the taps and routes it to the output. Figure 1.13 shows simplified schematic of string DAC.

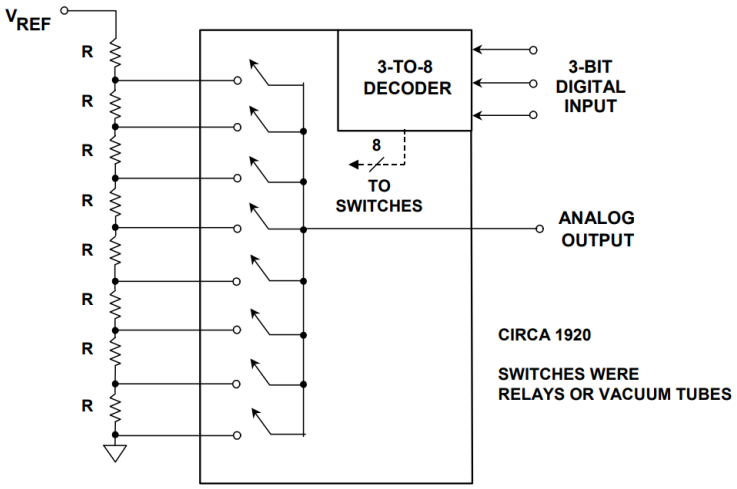

Figure 1.13: String DAC circuit [21]

To create an n-bit string DAC, we would need 2^n resistors and 2^n switches. This becomes an issue for high resolution String DACs. Their maximum resolution is typically 14 to 16 bits [22]. Due to the internal capacitances and the DAC's output resistance whose together form a RC network, they often have poor bandwidth. Also, imperfect resistor matching will create nonlinearities in the output.

1.3.2 Segmented string DAC

This is a modification of the standard string DAC that reduces the number of components needed for an n-bit DAC.

It utilizes two string DACs, where the first one selects a coarse interval of voltage. The second DAC uses the edge voltages of this interval as its reference, narrowing down the interval.

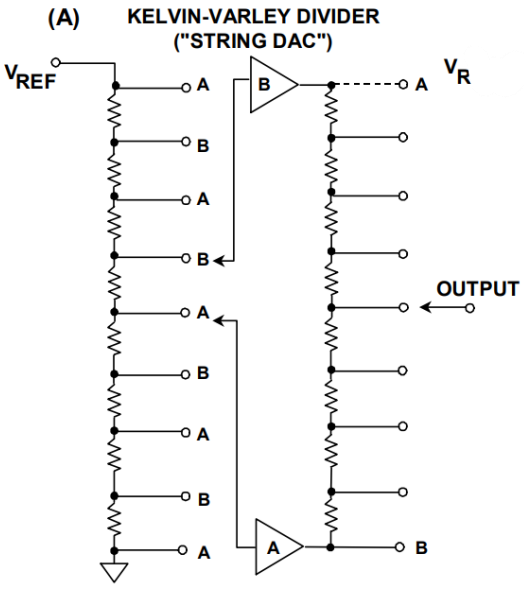

Figure 1.14: Segmented string DAC circuit [21]

Figure 1.14 shows the internal circuit of segmented string DAC type. Sometimes other types of DACs are used as the secondary DAC. While being an optimized version of the design DAC, it suffers from the same issues, such as nonlinearity and low bandwidth.

1.3.3 Thermometer DAC

The thermometer or fully decoded DAC is a current output DAC. While string DAC acts like a programmable voltage divider, this type functions more like a programmable resistor.

A 2^n-1 resistors with switches in series are connected between the reference input and the output. The resistors are often replaced by active current sources. As the input code increases, smaller and smaller resistors are being connected to the output,

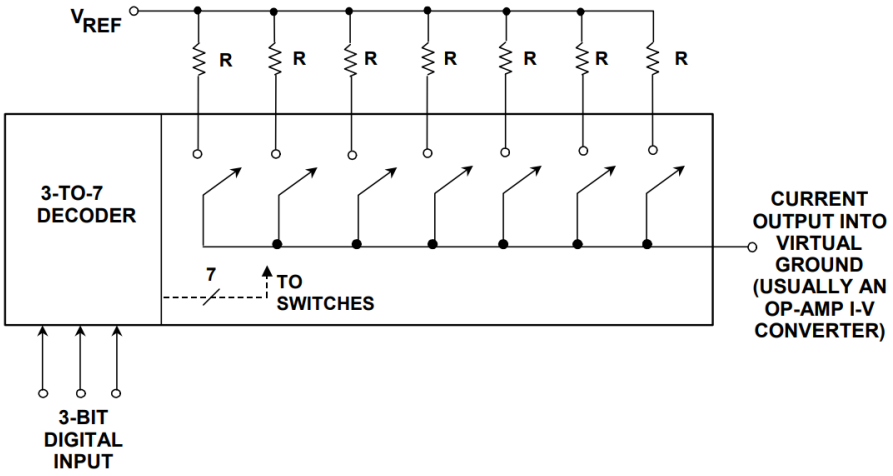

Figure 1.15: Thermometer DAC [21]

An inverting OPAMP configuration is often added to their output to convert the current into a voltage. While containing almost the same number of components, this architecture provides lower settling time than the string DAC.

1.3.4 Voltage mode R2R DAC

The voltage mode or normal mode R2R DAC consists of a R2R ladder. As shown in Figure 1.16, this resistor ladder topology consists of only 2 different values, making it more suitable for factory trimming.

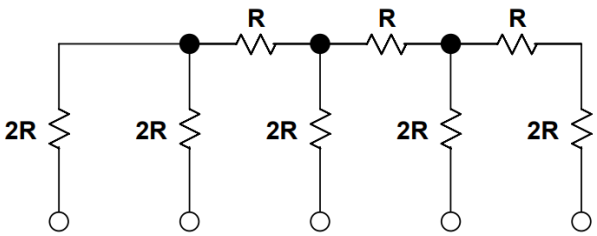

Figure 1.16: Example of a 4-bit R2R ladder [21]

The use of this resistor ladder in DACs leads to lower component count and thus the overall cost of the device.

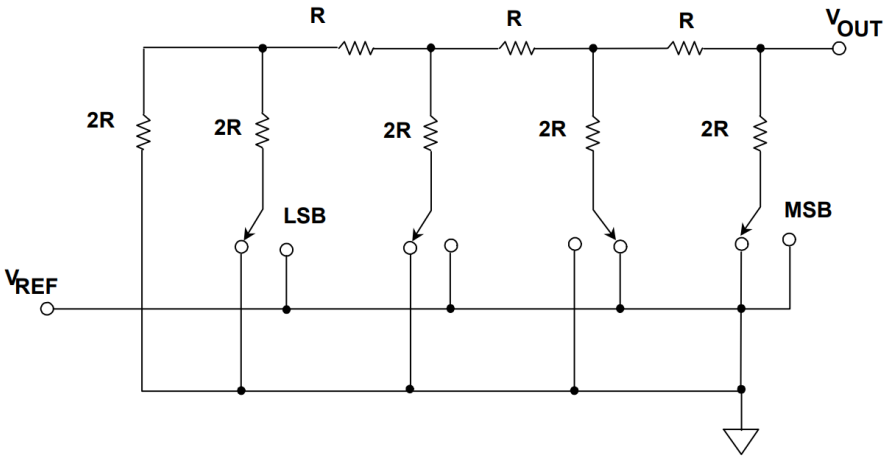

Figure 1.17: Voltage mode R2R DAC circuit [21]

Figure 1.17 shows the now integrated R2R network in a DAC. The small component count also reduces the settling time of the device, making it suitable for high-speed applications [21]. The main issue is that the resistance of the switches adds to the 2R resistors, degrading the DAC's precision.

1.3.5 Current mode R2R DAC

The current mode or inverted R2R DAC takes advantage of the properties of R2R network, but as the name suggests, the DAC topology is reversed. The node used as output in voltage mode is now used as the reference input, whereas the reference inputs are now turned into outputs.

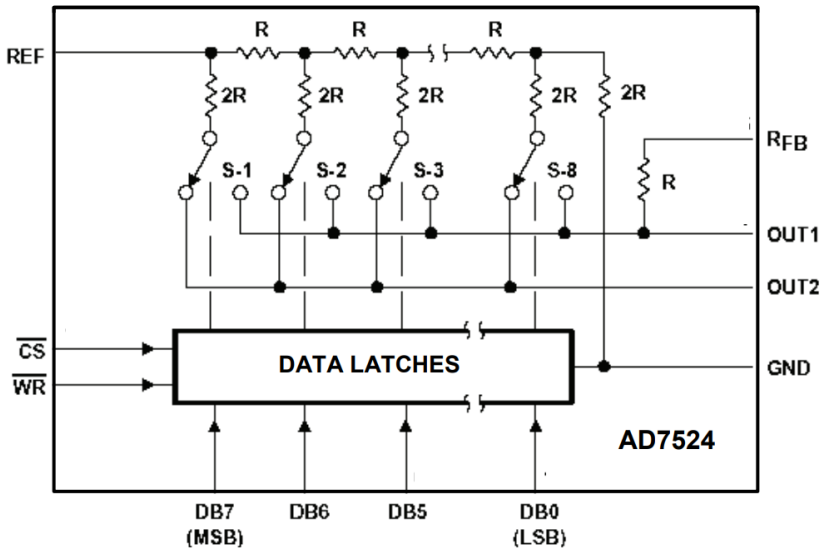

Figure 1.18: Current mode R2R DAC circuit [21]

As shown in Figure 1.18, the DAC has now two current outputs. Because the exact values of the resistors are not important, only their ratio, the manufacturers often add an equally trimmed resistor between the R_{FB} pin and OUT1. This resistor is used as feedback for current-to-voltage conversion by an OPAMP.

The current mode R2R DAC offers better bandwidth than voltage mode R2R converters for the same price, which makes it ideal for a signal generator application.

1.3.6 Sigma-Delta DAC

This DAC architecture favors digital electronics, as it contains the fewest analog components among the types presented.

It is composed of an interpolation filter, which increases the sample rate of the signal, a Sigma-Delta modulator, that converts the parallel data into a 1-bit data stream. A 1-bit DAC is basically a precision digital buffer that is used to assure the voltage precision of high and low state. This conditioned stream is then averaged by an output filter, which is the only analog component in this device. The connection of these blocks is displayed in Figure 1.19.

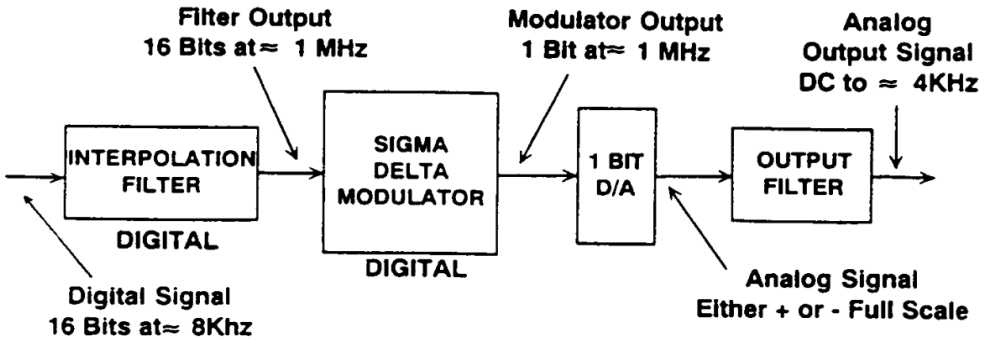

Figure 1.19: Sigma-Delta DAC block diagram [22]

This DAC architecture provides superior resolution (16 – 24 bits) at low cost, but the high oversampling rate required for filtering out the data stream makes it unusable for higher frequencies.

2. HARDWARE DESIGN

This chapter covers the design strategies, component selection and will present both the block diagrams and final circuit diagrams for each functional block of the device. The focus will be exclusively on the electrical aspects of the design.

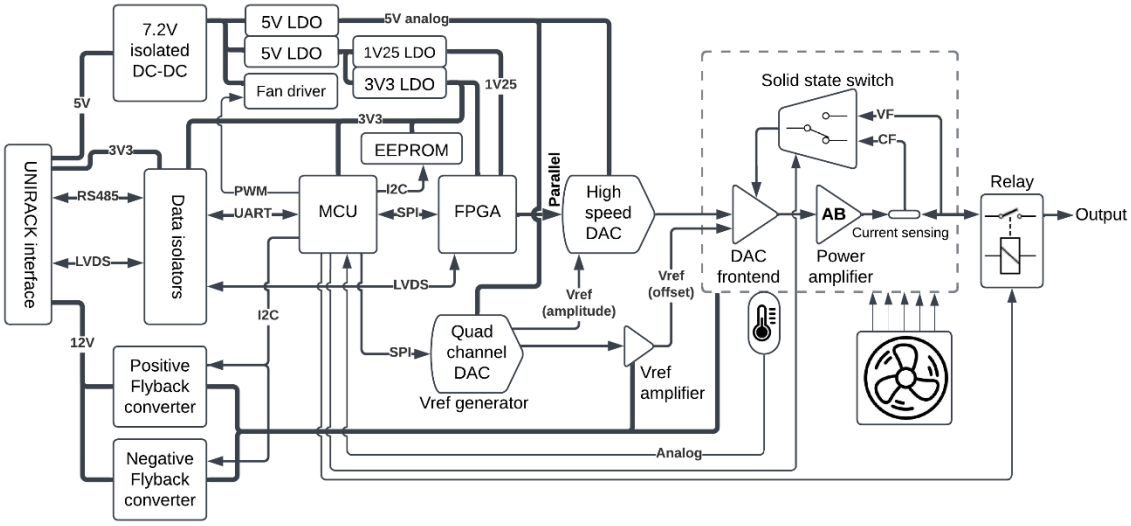

Figure 2.1: AWG complete block diagram

Figure 8 shows a functional block diagram of the device, where the lines with no arrows represent power supply lines, moderately thick ones with arrowheads correspond to an analog signal and thin arrow headed lines are used for control signals.

The left side of the block diagram is dedicated to isolated power converters and data isolators responsible for fulfilling the thesis criteria.

The middle part contains the MCU, which oversees the temperature, controls the programmable power supplies, configures the FPGA and decodes the commands transmitted via RS485. The FPGA is responsible for the signal generation. It contains a DDS core that outputs a stream of digital data corresponding to the samples of the output waveform. The DDS method was selected because of the low clock frequency required to function. This stream is then converted to analog voltage in a high-speed DAC. The quad-channel low-speed DAC is used to set the output amplitude and offset without sacrificing the resolution of high-speed DAC.

Finally, the right part is reserved for amplification of the analog signal. Basically, it functions as a voltage-to-voltage or voltage-to-current converting amplifier, depending on what feedback path is selected for the DAC frontend via the solid-state switch. An AB class power amplifier is used as a final amplification stage to ensure high output power capability.

The next subchapters will describe the internal composition of these blocks in greater detail.

2.1 Programmable voltage reference

This design block is used to set output amplitude and offset. For the DAC reference , which is basically the maximum output amplitude, 2.5V reference will be used because that is the common output voltage of many DACs.

On the other hand, the output power amplifier offset input requires positive or negative reference, depending on the offset polarity. Because most DACs can't produce negative output voltage, an amplifier needs to be used.

DAC8165, a 14bit quad-channel precision DAC with integrated 2.5V reference source was selected. The 2.5V is a common voltage for many mixed signal IC's and it is routed from the DAC to other modules, serving as a primary voltage reference for the whole device.

Although it is expensive, its precision will be necessary for sister modules that can be attached to this device in future.

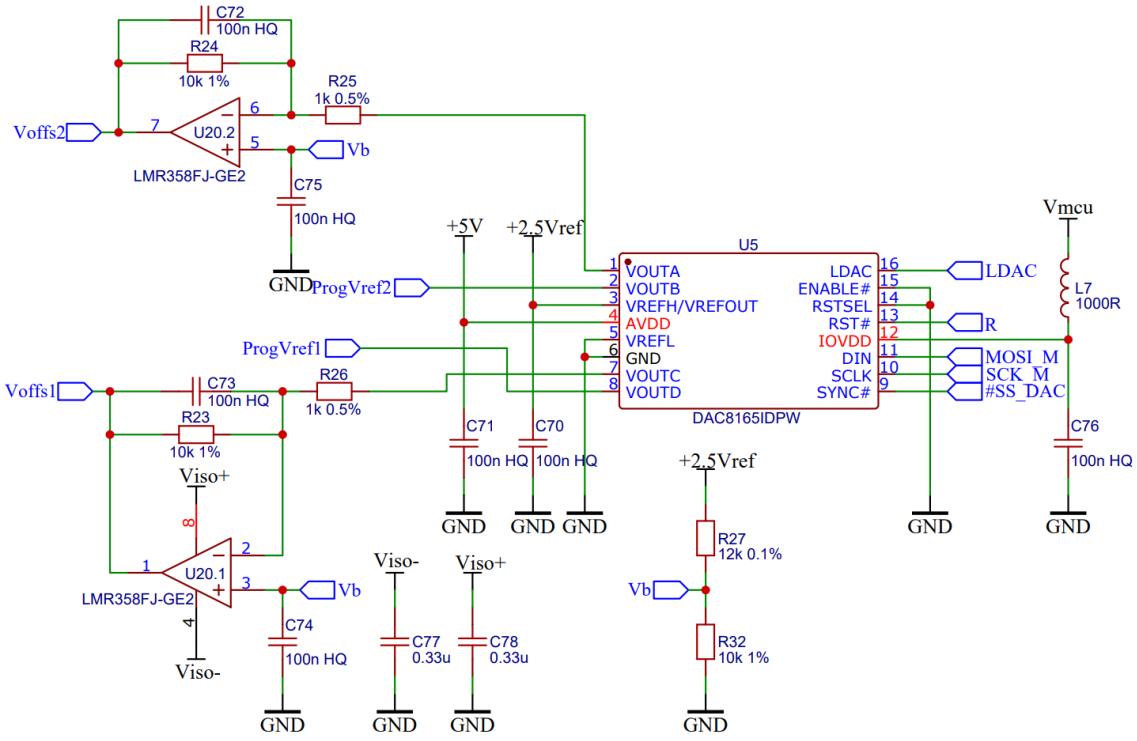

Figure 2.2: Programmable voltage reference circuit

Figure 2.2 shows the circuit of programmable reference block where ProgVref1 is the DAC amplitude reference, Voffs1 is the output offset reference.

As mentioned before, Voffs1 and Voffs2 must be capable of producing positive and negative voltage. This is why OPAMP U20 is configured as an inverting amplifier with offset. A voltage divider composed of resistors R27 and R32 create reference Vb that acts

as virtual ground, allowing the amplifier to output negative voltage when DAC output is higher than Vb. The selected output voltage range was chosen to be ±12.5 V, which means that the amplifiers gain needs to be 10. That's why the selected values are 10 kΩ for R23-R24 and 1 kΩ for R25-R26. The following calculation proofs the amplifier's gain.

$$A = -\frac{R_{24}}{R_{25}} = -\frac{10\ k\Omega}{1\ k\Omega} = -10 \tag{5}$$

The gain matches but is negative. This will be accounted for in the firmware. Now inverting input voltage can be calculated. It must be taken into account that when DAC outputs midscale voltage (half of its maximum), output of U20 must be 0 V. That converts R24 and R25 into simple voltage divider.

$$U_{OPAMP-} = U_{DAC} \cdot \frac{R_{24}}{R_{24} + R_{25}} = 1.25\ V \cdot \frac{10\ k\Omega}{10\ k\Omega + 1\ k\Omega} = 1.136\ V \tag{6}$$

With the OPAMP golden rule applied which says that both input voltages are equal, the last thing that remains is to calculate values of R27 and R32. For R32 a value of 10kΩ was selected again to simplify the bill of materials.

$$U_B = U_{OPAMP-} = U_{ref} \cdot \frac{R_{32}}{R_{27} + R_{32}} \rightarrow$$

$$R_{27} = R_{32} \cdot \frac{U_{ref}}{U_{OPAMP-}} - R_{32} \rightarrow$$

$$R_{27} = 10\ k\Omega \cdot \frac{2.5\ V}{1.136\ V} - 10\ k\Omega = 12\ k\Omega \tag{7}$$

The outputs of the reference generator are used in the following design block.

2.2 High-speed DAC

One of the most important components of arbitrary waveform generators is the digital to analog converter. The 2 main parameters of every DAC are resolution and sampling frequency.

2.2.1 Sampling frequency

To select the sampling frequency, Nyquist theorem needs to be applied. With maximum output frequency being 1 MHz, the sampling frequency needs to be at least 2 MHz.

To ensure that the output waveform is easily distinguished, a factor of 10 was selected, thus, the minimum sampling frequency of the DAC is 20 MS/s.

2.2.2 Resolution

Choosing DAC resolution depends on the maximum output voltage swing and minimum voltage step. The maximum voltage swing is 30 V. The desired voltage step is 5 mV. From these parameters, minimum resolution N can be calculated after modifying formula X:

$$\Delta_{V_{out}} = \frac{V_{ref}}{2^N} \rightarrow 2^N = \frac{V_{ref}}{\Delta_{V_{out}}} \rightarrow N = \log_2 \frac{V_{ref}}{\Delta_{V_{out}}} = 11{,}55 \text{ bit} \quad (8)$$

To satisfy the 5mV output step, final resolution of 12-bit was selected. With these input parameters, AD5445 was the most suitable for this application. It is a 20.4MS/s

12-bit current output DAC with parallel interface.

2.2.3 Current to voltage converting frontend

Because AD5445 has current output, it is necessary to convert it to voltage. It has reverse R2R DAC architecture with no output buffer, so it basically works like a programmable potentiometer.

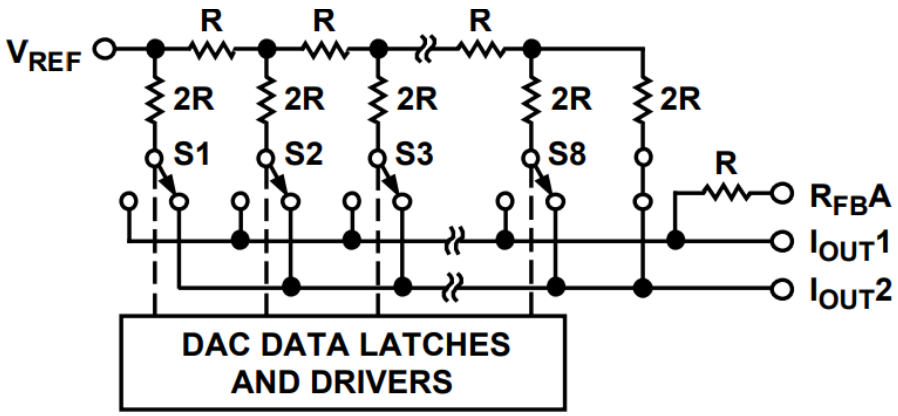

Figure 2.3: AD5445 DAC architecture [6]

The higher the input data, the lower the resistance between V_{REF} and $I_{OUT}1$, and higher resistance between V_{REF} and $I_{OUT}2$ and vice versa.

Fortunately, the manufacturer included a few example circuits for current-to-voltage conversion.

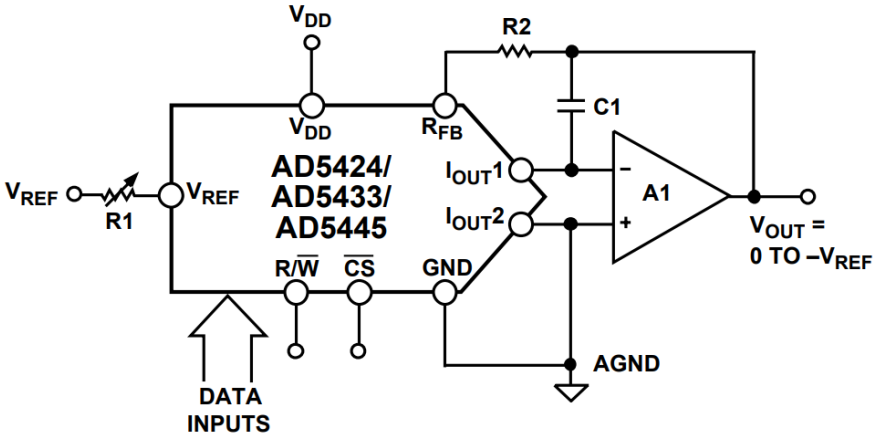

Figure 2.4: AD5445 voltage output datasheet example circuit [6]

It is basically configured as an inverting amplifier with constant input voltage and programmable gain. Since R1 and R2 are used only for gain adjustment, they won't be necessary because gain adjustment will be performed in device firmware.

C1 works as phase compensation, lowering OPAMP's gain at higher frequencies, preventing overshooting and ringing of the output. Its value was chosen from DAC's datasheet.

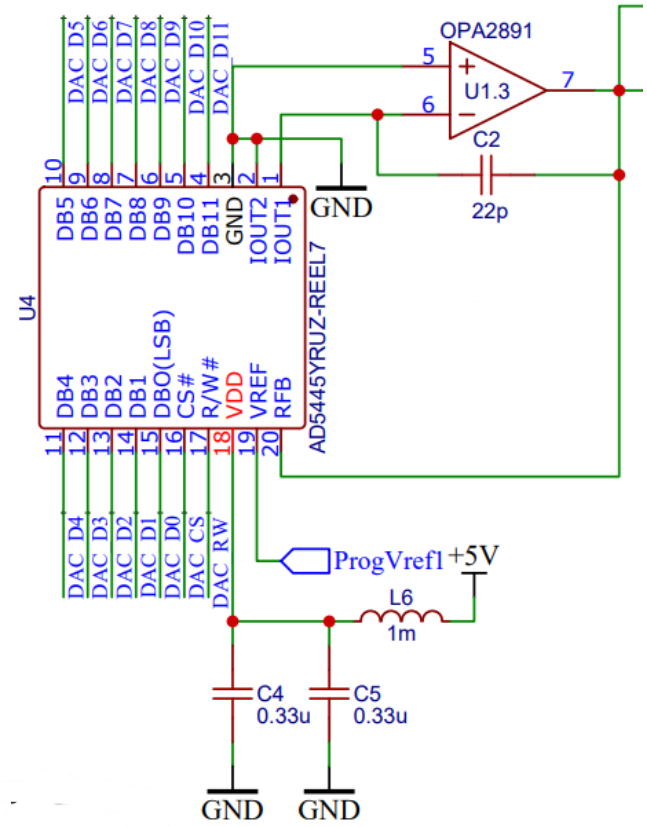

Figure 2.5: AD5445 voltage output circuit

Figure 2.5 shows the final DAC circuit, featuring the DAC itself and its current-to-voltage converting OPAMP. The formula describing the output voltage of this setup is

$$U_{DACOut} = -U_{ProgVref1} \cdot \frac{N}{2^n} \tag{9}$$

Where $U_{ProgVref1}$ is the voltage of programmable voltage reference that sets the maximum amplitude, n is the bit width of the DAC and N is the DAC input data.

Note that the output voltage range is unipolar, 0 V to -V_{REF} only. This will be corrected by the power amplifier.

2.3 Output power frontend

One of the main requirements of the device is its high output current. That is why this chapter focuses on the design process of a power frontend, composed of a power amplifier and feedback regulator. The power frontend is responsible for voltage amplification of the DAC output as well as converting it to current or voltage according to input control signal which selects the output mode.

2.3.1 Power amplifier topology

Because the output current needs to be as high as 1 A with a 15V amplitude, amplifying DAC output is necessary.

The easiest but most expensive solution is to use a single operational amplifier such as PA96CE.

A custom class AB transistor amplifier was chosen as the solution due to its lower cost and high power that can be easily scaled for future purposes. To explain the functionality of class AB, it is necessary to start with its simpler counterpart: class B. Typical class B amplifiers are composed of two common collector bipolar transistor amplifiers, PNP and NPN. The NPN pushes the current into output load and PNP pulls it from load.

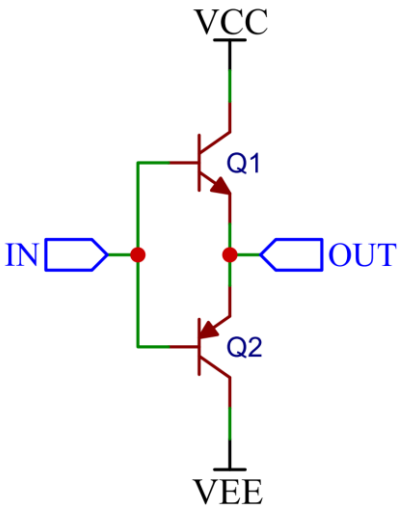

Figure 2.6: Class B amplifier [8]

Figure 2.6 shows the schematic of class B amplifier, which is the simplest form of push-pull amplifier, where VCC is the positive supply voltage and VEE is a negative supply voltage, with both having the same but inverted voltage (VCC = -VEE). Assuming that the output load is terminated to ground (0 V), when the input-output voltage difference is higher than the base-emitter voltage of Q1, current will flow into the base, opening transistor Q1 and supplying current to load and if the output-input voltage difference is lower than output voltage base-emitter voltage of Q2, Q2 will start to conduct and sink current from load towards VEE.

However, when the input voltage doesn't fulfill these conditions, neither of the bases will receive sufficient current to open the corresponding transistor and output will remain at 0 V. This will not only lower the output amplitude by Ube but will also add distortion at zero crossing [8].

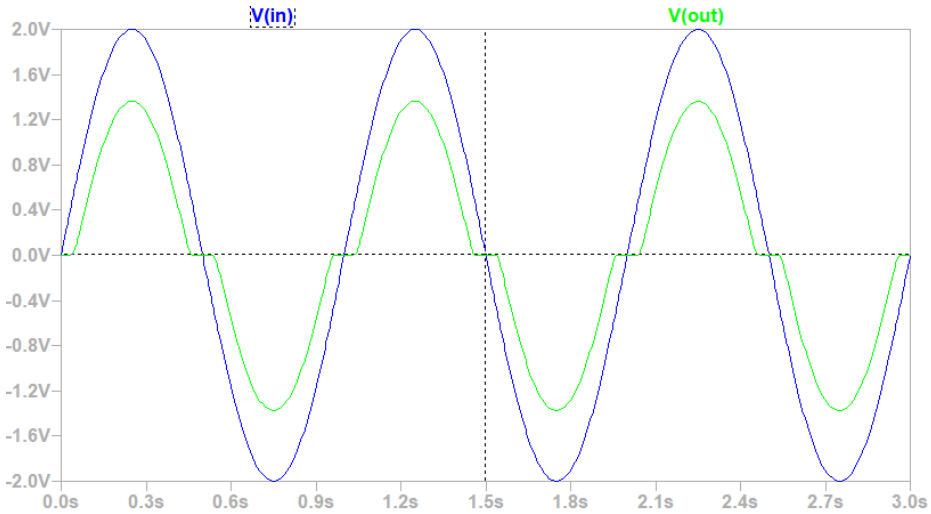

Figure 2.7: Simulation result of class B amplifier with no bias

This can be solved by applying bias voltage to both transistors' bases. Each base receives a bias voltage equal to their Ube. This converts class B amplifier to class AB.

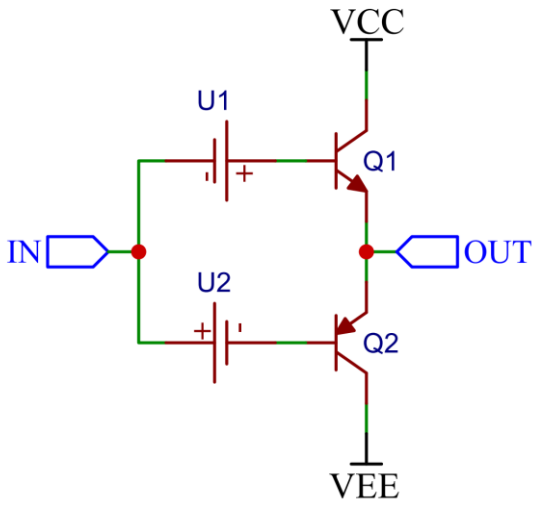

Figure 2.8: Class AB amplifier [8]

If bias voltages U1 and U2 are chosen correctly, meaning both are a bit higher than Ube of their corresponding transistor, Q1 and Q2 will be partially open even if input is 0V.

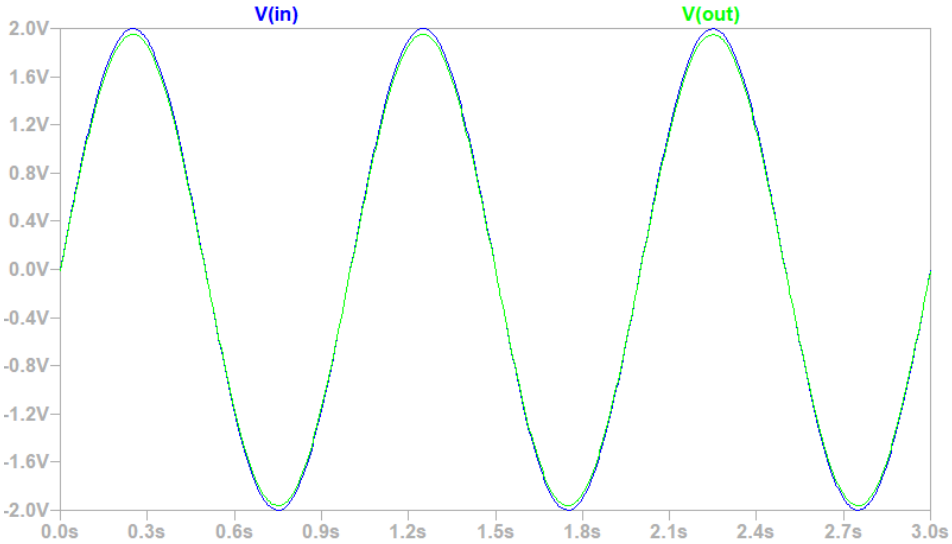

Figure 2.9: Simulation result of class AB amplifier

The biggest downside to this method is that Q1 and Q2 are now both open near zero and current will leak from VCC to VEE, decreasing the overall efficiency. Increasing the bias voltage reduces distortion but it also increases leakage current. Ube also varies with temperature.

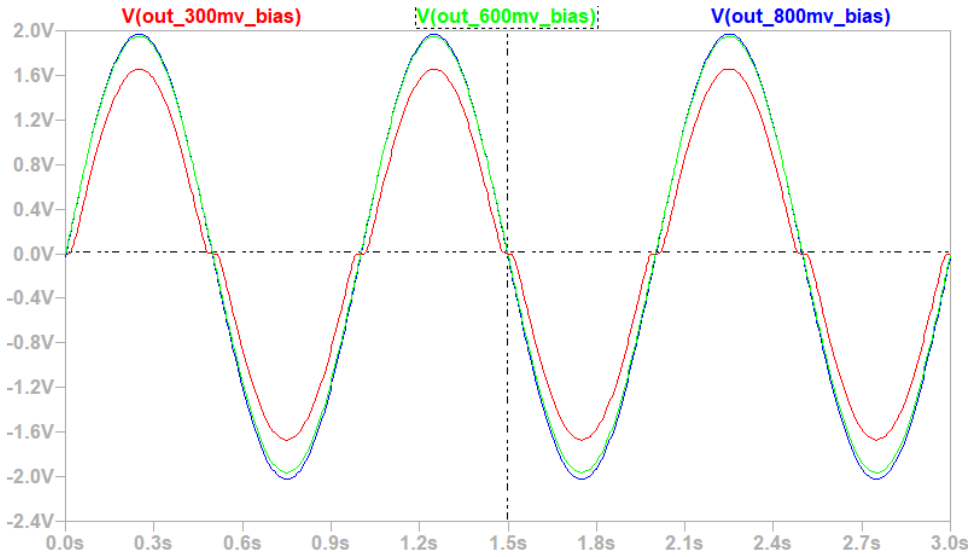

Figure 2.10: Simulation of amplifiers output depending on bias voltage

In this simulation, transistors were chosen so that Ube voltage of both is 600 mV. From figure 17, it is clear that the 300 mV bias is not enough, and zero crossing distortion persists as well as the output voltage drop. With 600 mV bias, the output has no distortion, but a slight voltage drop can be seen in contrast with 800 mV bias, which has no distortion and completely copies the 2 V peaks of input sine wave.

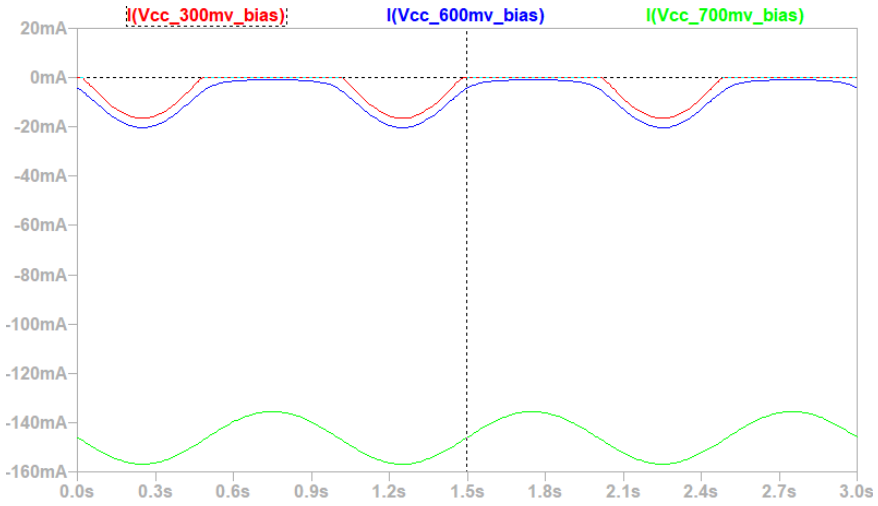

Figure 2.11: Simulation of current consumption depending on the bias voltage

Because the output load is a 100Ω resistor, the maximum current draw from VCC should be 20 mA since the peak voltage is 2 V. The 300mV bias variant doesn't reach the desired 2V output amplitude (as seen in Figure 2.10), but its current consumption is the lowest. The 600mV bias variant's peak current consumption is precisely 20 mA. Because of the large bias of 700 mV, both transistors are partially open and draw around 145 mA from VCC to VEE, which equals to 4.35W of total power loss.

This means that there is a sweet spot between output distortion and current consumption, and it is slightly higher than the Ube voltage.

2.3.2 Class AB amplifier biasing

Note that the bias voltage is referenced to input signal and not ground. To achieve this, some designs use voltage divider biasing.

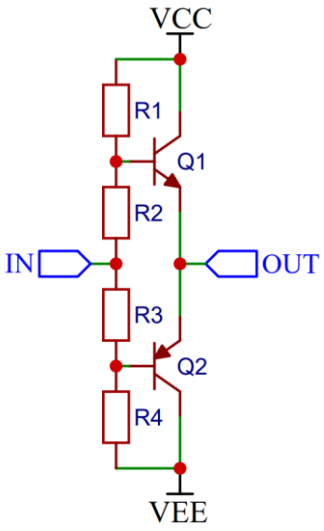

Figure 2.12: Class AB amplifier voltage divider biasing

This method allows designers to easily set bias by adjusting ratio of R1 and R2. When the temperature of the circuit increases, Ube decreases but bias voltage remains almost unchanged due to the good temperature stability of resistors. This will lead to an increase in base current of both transistors, increasing the total power consumption. Also, the solution works best only if the VCC and VEE are constant, which they are not due to better efficiency at lower output amplitudes.

R2 and R3 can be replaced by diodes with forward voltage almost equal to transistors Ube which will improve temperature stability because of similar diode forward voltage/temperature dependence, but it might be challenging to match diode voltage with transistor.

That’s why the chosen solution is the replacement of R1 and R4 with current sources.

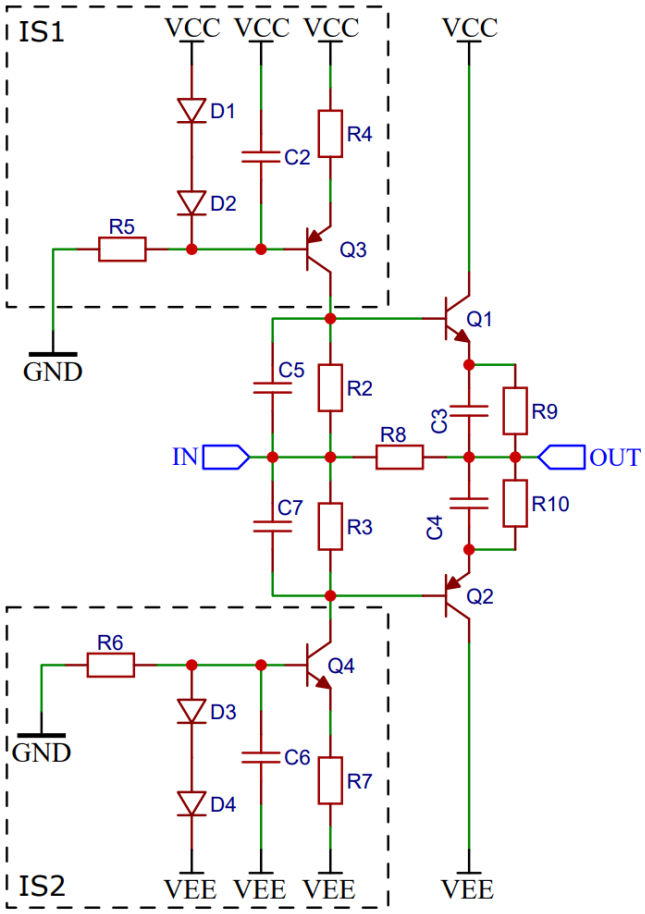

Figure 2.13: Current source resistor voltage drop biasing

C3, C4, C5 and C7 were added to bypass resistors, increasing the amplifier's bandwidth. R9 and R10 act as negative feedback for Q1 and Q2. If for example the bias voltage of Q1 gets too high, emitter current will increase as well as voltage drop on R9, lowering the base-emitter voltage of Q1 and thus bias voltage. Voltage difference between input and transistors base is dependent on resistance of R2-R3 and output current of current source IS1-IS2.

$$U_{Q1bias} = U_{Q1be} + U_{R9} = R2 \cdot I_{IS1} + R2 \cdot I_{Q1E} \tag{10}$$

2.3.3 Current sources

Current source IS1 is sourcing current from VCC and IS2 sinks towards VEE.

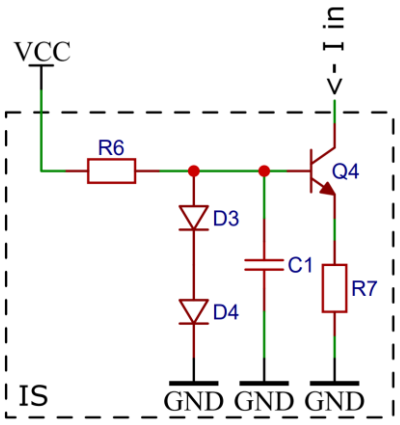

Figure 2.14: Current sink IS2 circuit

For simplicity VCC offset was added to the circuit, converting VEE to GND and GND to VCC. R6 with D3 and D4 functions as voltage source. Base voltage on Q4 will be given by the following simplified formula:

$$U_{Q4B} = U_{DF3} + U_{DF4} = 2 \cdot U_{DF} \tag{11}$$

This formula assumes that both diodes have the same parameters, and their drop doesn't change with VCC level. Q4 acts as BJT common collector voltage follower with output at R7.

$$U_{R_7} = U_{Q4B} - U_{Q4BE} = 2 \cdot U_{DF} - U_{Q4BE} \tag{12}$$

By selecting Q4 with Ube close to the diode's U_{DF} the formula can be then simplified:

$$U_{R_7} = 2 \cdot U_{DF} - U_{Q4BE} = 2 \cdot U_{DF} - U_{DF} = U_{DF} \tag{13}$$

Meaning that voltage on R7 will be almost same as diode forward voltage. The current flowing out of Q4 emitter is:

$$I_{Q4E} = \frac{U_{R_7}}{R_7} = \frac{U_{DF}}{R_7} \tag{14}$$

Now the collector current can be calculated:

$$I_{Q4E} = \beta_{Q4} \cdot I_{Q4B} \rightarrow I_{Q4B} = \frac{I_{Q4E}}{\beta_{Q4}} \rightarrow$$

$$I_{Q4C} = I_{Q4E} - I_{Q4B} = I_{Q4E} - \frac{I_{Q4E}}{\beta_{Q4}} = I_{Q4E} \cdot \left(1 - \frac{1}{\beta_{Q4}}\right) \approx I_{Q4E} \quad (15)$$

Where β_{Q4}, also known as h_{FE} is DC current gain of Q4. Because most small signal BJT transistors have β in order of hundreds, impact of base current can be neglected. The final current is given by this formula:

$$\mathrm{I_{IS2}} = \frac{\mathrm{U_{DF}}}{\mathrm{R_7}} \quad (16)$$

Collector current is the current source output. The same formula applies to the current source IS1. With current source formula, bias voltage can be calculated:

$$U_{Q1bias} = U_{Q2bias} = \frac{R_2}{R_4} \cdot U_{DF} = \frac{R_3}{R_7} \cdot U_{DF} \quad (17)$$

2.3.4 Power transistors

PHPT61003 (NPN) and PHPT60603PYX (PNP) were selected as power transistors with max collector-emitter voltage of 80 V and max current of 3 A. Both transistors have very similar parameters in terms of maximum ratings, although their Ube is slightly different: 0.67 V typical and 0.85 V maximum for NPN and 0.83 V typical to 0.9 V maximum for PNP. Real life experiments showed that bias voltage value of 0.85 V was the ideal setpoint.

For current source voltage reference diodes BAV99-A7 were selected, which is composed of two Schottky diodes in series packed in a single package with forward voltage U_{DF} drop typically 0.7 V.

BC857 and BC846 (Q4 and Q3) were picked based on their similar Ube with BAV99-A7 forward voltage, 0.66 V typically for both. Values of R2 and R3 cannot be too high, as the base current of Q1 and Q2 would decrease the set bias. Conversely, they cannot be too low, as this would cause overheating of the current source transistors Q3 and Q4, altering the set current and, consequently, the bias point. Additionally, low values of R2 and R3 would reduce the amplifier's input impedance. First, the value of 120Ω was picked for the R2 resistor, which enabled the calculation of R4.

$$U_{Q4BE} = \frac{R_2}{R_4} \cdot U_{DF} \rightarrow R_4 = \frac{R_2}{U_{Q4BE}} \cdot U_{DF} = \frac{120}{0.85} \cdot 0.7 = 98.82\Omega \approx 100\Omega \quad (18)$$

Previously it was assumed that diode has constant forward voltage. However, real diodes forward voltage depends on the amount of current that flows through it, as well as temperature. Table 2 shows the relation of BAV99-A7 forward voltage to the forward current. The values were obtained from the datasheet and then the volt-ampere characteristics was approximated in simulation.

Table 2.1: BAV99-A7 forward voltage to current relation

I_{DF} [mA]	U_{DF} [V]
1	0,715
10	0,855
50	1
100	1,25

The goal is to achieve U_{DF} stability over a wide range of supply voltage. At sub mA currents, the U_{DF} will be changing in relation to current, altering the previous set bias. According to simulation in LTspice, 0.35 mA was the lowest current at which the diode forward voltage was above 0.665 V or about 95% of the desired value. R5-R6 value can now be calculated:

$$I_{DF} \approx \frac{VCC - 2 \cdot U_{DF}}{R_5} \rightarrow R_5 = \frac{VCC_{Min} - 2 \cdot U_{DF}}{I_{DF_{Min}}}$$
$$= \frac{5\,V - 2 \cdot 0.665\,V}{0.35\,mA} = 10500\Omega \approx 10\,k\Omega \quad (19)$$

The maximum current is given by following formula:

$$I_{DF_{Max}} \approx \frac{VCC_{Max} - 2 \cdot U_{DF}}{R_5} = \frac{15V - 2 \cdot 0.665\,V}{10\,k\Omega} = 1.4\,mA \quad (20)$$

Note that the formula only approximates currents because the base current of Q3 is neglected. Values of feedback resistors R9 and R10 were chosen so that at maximum current of 1 A, the voltage drop will be less than 0.25 V. Two 200mΩ 1W thick film resistors were chosen, which means that the maximum voltage drop will be 0.2 V.

2.3.5 Output current sense

This circuit senses the output current and converts it into voltage that is fed to feedback loop, creating a voltage-to-current converter. It consists of a shunt resistor connected between output of AB amplifier and device output. This way the output current will create a voltage drop across it. The bigger the shunt resistor value, the larger voltage drop will be created which will allow smaller currents to be sensed.

However, a large resistance will limit the maximum output voltage swing at high currents.

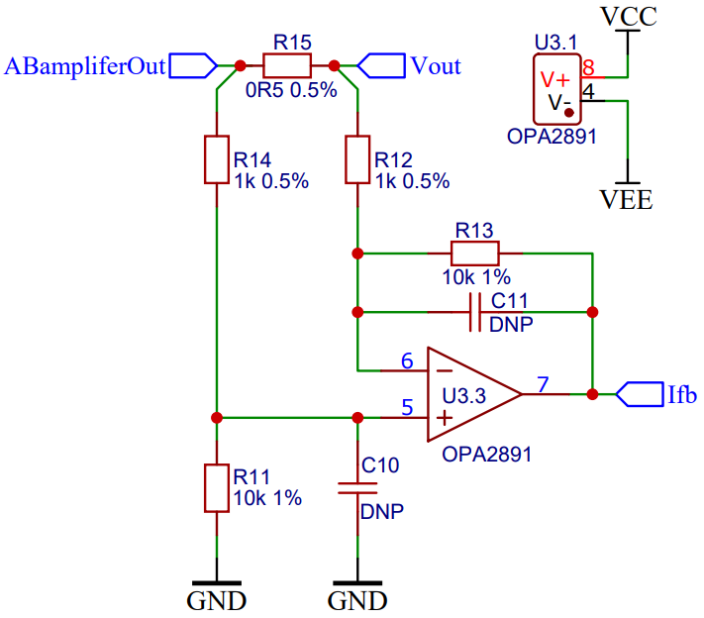

Figure 2.15: Output current sense circuit

One way around this is to choose small resistor value that will produce smaller voltage drop that can be amplified. Since the shunt resistor R15 is not connected to ground, a differential amplifier needs to be used. Shunt value of 0.5 Ω was selected with maximum voltage drop of 0.5 V and power dissipation of 0.5 W. This differential voltage is amplified by U3.3. the amplifier output formula is [9]:

$$U_{Ifb} = \frac{R_{13}}{R_{12}} \cdot U_{R15} = \frac{R_{13}}{R_{12}} \cdot \left(U_{ABampliferOut} - U_{out}\right) \tag{21}$$

This formula is in simplified form because R12 = R14 and R11 = R13 [9]. With the maximum differential voltage of 0.5V and minimum VCC to GND voltage of 5V, maximum gain of 10 can be used because selected OPA2891 has Rail-to-Rail output. For R13(R11) the value of 10kΩ was selected because it is already present in circuit. Now R12 can be calculated:

$$U_{Ifb_{Max}} = \frac{R_{13}}{R_{12}} \cdot \Delta U_{Max} \rightarrow R_{12} = R_{13} \cdot \frac{\Delta U_{Max}}{U_{Ifb_{Max}}}$$
$$= 10\ k\Omega \cdot \frac{0.5\ V}{5\ V} = 1\ k\Omega \tag{22}$$

The output voltage in relation to output current can be now derived in the next formula:

$$U_{Ifb} = \frac{R_{13}}{R_{12}} \cdot U_{R15} = \frac{R_{13}}{R_{12}} \cdot R_{15} \cdot I_{OUT} \quad (23)$$

2.3.6 Output voltage sense

Output voltage is sensed after the current shunt resistor to compensate for its voltage drop. This circuit acts as impedance isolation, so feedback doesn't draw current from beyond the shunt resistor which would decrease the output current sense precision.

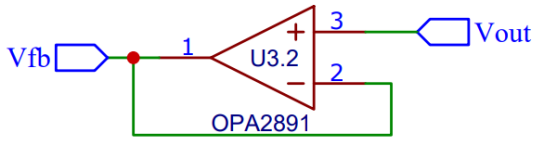

Figure 2.16: Output voltage feedback impedance isolation

The second channel of U3 OPAMP is used for this purpose.

2.3.7 Output mode selection

The voltage or current output depends solely on the chosen feedback source. For that purpose, an analog 2-to-1 multiplexer is utilized.

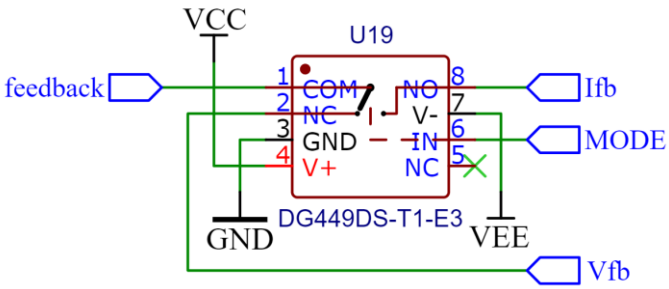

Figure 2.17: Feedback selecting 2-to-1 analog multiplexer

Because of its wide operating voltage of 5 V to 40 V, low on resistance flatness and digital input ground reference, DG449 is used. When digital signal MODE is low, NC(voltage feedback) is connected to COM(feedback node) and the device operates in Voltage output mode. Applying logic 1 to MODE pin connects NO(current feedback) to COM(feedback node) switching the device into Current output mode.

2.3.8 Main feedback regulator

The “beating hearth” of the power amplifier frontend is the feedback regulator. It corrects the AB amplifiers distortion, offset and gain error. Basically, it is a summation inverting OPAMP topology.

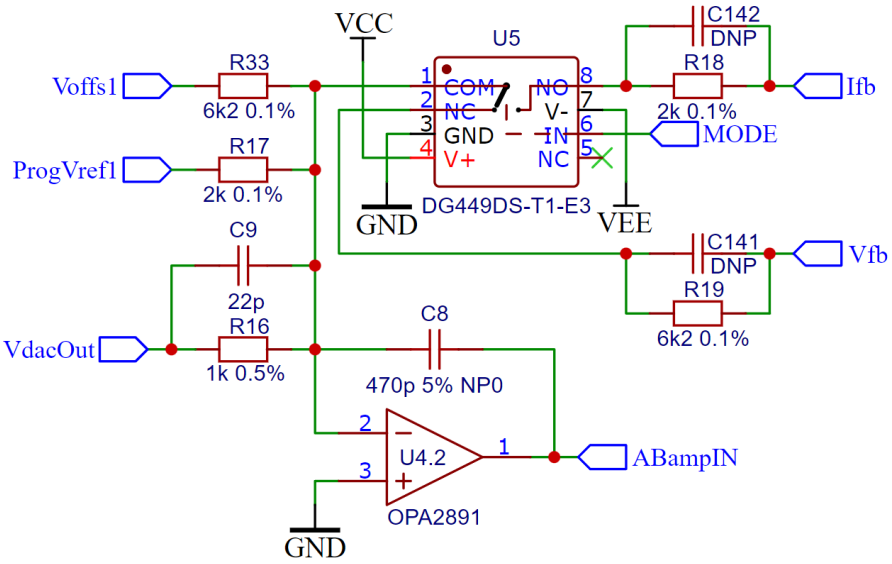

Figure 2.18: Main feedback regulator circuit

OPA2891 is a high-speed low offset Rail-to-Rail output operation amplifier. With this topology, it is possible to add output offset with input Voffs1. Because it is generated by the reference DAC, output with small amplitude but large offset can be generated with high-speed DAC full resolution.

The regulator OPAMP U4.2 tries to keep its inverting input at 0 V. as mentioned in high-speed DAC chapter, VdacOut has voltage range from 0 V to minus ProgVref1. The value of resistor R16 was chosen to be 1k because of its previous usage. DAC output is unipolar, but the output must be bipolar.

To achieve that, R17 with value of 2 kΩ was added between ProgVref1 and inverting input of U4.2, injecting half of the maximum current that can flow from VdacOut to the regulation node. This way when the DAC is set to midscale, the voltage on the inverting pin will be 0 V. The following formula for summation inverting amplifier was taken from Analog devices MT-214 manual [10].

$$U_{Vfb} = -R_{19} \cdot \left(\frac{U_{DACOut}}{R_{16}} + \frac{U_{ProgVref1}}{R_{17}} + \frac{U_{offs1}}{R_{33}} \right) \tag{24}$$

$$U_{Ifb} = -R_{18} \cdot \left(\frac{U_{DACOut}}{R_{16}} + \frac{U_{ProgVref1}}{R_{17}} + \frac{U_{offs1}}{R_{33}} \right) \tag{25}$$

Formula 24 applies if MODE is set to 0 and the voltage feedback is selected. In other case, formula 25 is used. We will be focusing on formula where voltage mode is selected. To calculate R17, ProgVref1 will be set to 2 V, VdacOut is going to be midscale, which is -1 V, Voffs to 0 V and desired output voltage will be 0 V. The formula can be simplified to this form:

$$0 = -R_{19} \cdot \left(\frac{U_{DACOut}}{R_{16}} + \frac{U_{ProgVref1}}{R_{17}}\right) \rightarrow -\frac{U_{ProgVref1}}{R_{17}} = \frac{U_{DACOut}}{R_{16}} \rightarrow$$
$$-R_{16} \cdot \frac{U_{ProgVref1}}{U_{DACOut}} = R_{17} = -1\ k\Omega \cdot \frac{2}{-1} = 2\ k\Omega \quad (26)$$

R18 and R19 will set the final gain and will be adjusted in real life experiments. Now that all the necessary block of the power amplifier frontend designed and their formulas derived, the final formula that will convert the DAC input data into the output current or voltage, depending on the selected mode.

First, the main regulator formulas 24 and 25 are combined with formulas describing the voltage and current sense circuit and the DAC output voltage is derived.

$$U_{Vfb} = U_{\mathrm{OUT}} = -R_{19} \cdot \left(\frac{U_{DACOut}}{R_{16}} + \frac{U_{ProgVref1}}{R_{17}} + \frac{U_{offs1}}{R_{33}}\right) \rightarrow$$
$$U_{DACOut} = -R_{16} \cdot \left(\frac{U_{\mathrm{OUT}}}{R_{19}} - \frac{U_{ProgVref1}}{R_{17}} - \frac{U_{offs1}}{R_{33}}\right) \quad (27)$$

Formula 27 applies for voltage mode and is used to calculate the voltage on DAC frontend. Now, U_{DACOut} is substituted by the DAC formula 9:

$$U_{DACOut} = -U_{ProgVref1} \cdot \frac{N}{2^n} = -R_{16} \cdot \left(\frac{U_{\mathrm{OUT}}}{R_{19}} - \frac{U_{ProgVref1}}{R_{17}} - \frac{U_{offs1}}{R_{33}}\right) \rightarrow$$
$$N = \frac{R_{16} \cdot 2^n}{U_{ProgVref1}} \cdot \left(\frac{U_{\mathrm{OUT}}}{R_{19}} - \frac{U_{ProgVref1}}{R_{17}} - \frac{U_{offs1}}{R_{33}}\right) \quad (28)$$

Formula 28 is used by the MCU to calculate the n-bit DAC's input code N for the given output voltage U_{OUT}, reference voltage $U_{ProgVref1}$ and offset U_{offs1}.

When the device is in current mode, the same process is used to derive the formula:

$$U_{Ifb} = \frac{\mathrm{R}_{13}}{\mathrm{R}_{12}} \cdot \mathrm{R}_{15} \cdot \mathrm{I}_{\mathrm{OUT}} = -R_{18} \cdot \left(\frac{U_{DACOut}}{R_{16}} + \frac{U_{ProgVref1}}{R_{17}} + \frac{U_{offs1}}{R_{33}}\right) \rightarrow$$

$$U_{DACOut} = -R_{16} \cdot \left(\frac{\mathrm{R_{13}}}{\mathrm{R_{12}}} \cdot \frac{\mathrm{R_{15}}}{R_{18}} \cdot \mathrm{I_{OUT}} - \frac{U_{ProgVref1}}{R_{17}} - \frac{U_{offs1}}{R_{33}}\right) \rightarrow$$

$$-U_{ProgVref1} \cdot \frac{N}{2^n} = -R_{16} \cdot \left(\frac{\mathrm{R_{13}}}{\mathrm{R_{12}}} \cdot \frac{\mathrm{R_{15}}}{R_{18}} \cdot \mathrm{I_{OUT}} - \frac{U_{ProgVref1}}{R_{17}} - \frac{U_{offs1}}{R_{33}}\right) \rightarrow$$

$$N = \frac{R_{16} \cdot 2^n}{U_{ProgVref1}} \cdot \left(\frac{\mathrm{R_{13}}}{\mathrm{R_{12}}} \cdot \frac{\mathrm{R_{15}}}{R_{18}} \cdot \mathrm{I_{OUT}} - \frac{U_{ProgVref1}}{R_{17}} - \frac{U_{offs1}}{R_{33}}\right) \quad (29)$$

Formula 29 is used in current output mode and it converts the desired output current into the DAC input code.

2.3.9 Overtemperature protection

Because the output stage consists of 2 transistors operating in linear mode, sourcing or sinking of high currents will result in large power losses on the transistors. For example, if the output power amplifier's voltage is ±15 V, output voltage is 1 V and the load is 2 Ω to ground, the equivalent circuit is shown in Figure 2.19.

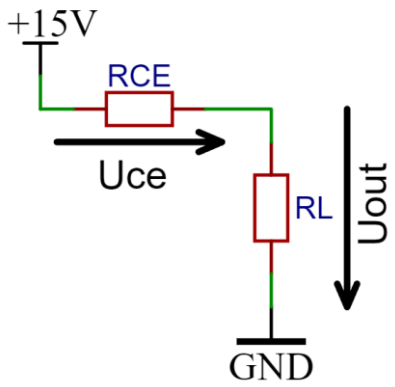

Figure 2.19: Equivalent circuit used for modeling output stage power loss

Power loss of the power amplifier can be calculated by the following formulas:

$$I_{ce} = I_L = \frac{U_L}{R_L} = \frac{1\,V}{2\,\Omega} = 0.5\,A \quad (30)$$

$$U_{ce} = U_{cc} - U_L = 15\,V - 1\,V = 14\,V \quad (31)$$

$$P_{loss} = U_{ce} \cdot I_{ce} = 14\,V \cdot 0.5\,A = 7\,W \quad (32)$$

Where I_L is the load current, I_{ce} is the collector-emitter current passing through high-side transistor, R_L is the load resistance, U_{ce} is voltage drop across transistor and U_{cc} is the supply voltage.

Static thermal simulation in SolidWorks revealed that with passive cooling the transistor will heat up to approximately 145 °C. Simulation results are shown in the chapter 3.2. Note that at this temperature the transistor's maximum power dissipation derates more than 80% and it could result in damaging or destruction of the amplifier output stage. That's why it's necessary to monitor temperature and control blower fan or even disable generator's output via relay.

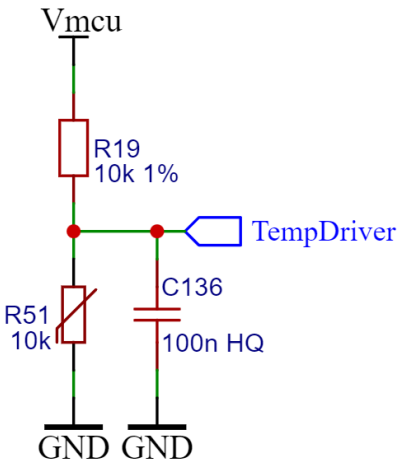

Figure 2.20: NTC temperature sensor circuit

Figure 2.20 shows the circuit used for measurement of amplifiers temperature. A voltage divider configuration is used to convert resistance of the NTC thermistor R51 into voltage that MCU can measure. C136 acts as lowpass filter, lowering the output noise. General formula for voltage divider is:

$$U_{out} = U_{in} \cdot \frac{R_{NTC}}{R_{NTC} + R_{Pullup}} = U_{MCU} \cdot \frac{R_{51}}{R_{51} + R_{19}} \tag{33}$$

The formula for resistance of NTC thermistor is:

$$R_{NTC} = R_{25°C} \cdot e^{\beta \cdot \left(\frac{1}{T_{NTC}} - \frac{1}{T_{25°C}}\right)} \tag{34}$$

By combining these two formulas we can derive the conversion from temperature to voltage:

$$U_{out} = U_{MCU} \cdot \frac{R_{51}}{R_{51} + R_{19}} \rightarrow \frac{U_{MCU}}{U_{out}} = \frac{R_{51} + R_{19}}{R_{51}} = 1 + \frac{R_{19}}{R_{51}} \rightarrow$$

$$\frac{R_{19}}{\frac{U_{MCU}}{U_{out}}-1}=R_{25°C}\cdot e^{\beta\cdot\left(\frac{1}{T_{NTC}}-\frac{1}{T_{25°C}}\right)}\rightarrow\frac{1}{\beta}\cdot ln\left(\frac{\frac{R_{19}}{R_{25°C}}}{\frac{U_{MCU}}{U_{out}}-1}\right)=\frac{1}{T_{NTC}}-\frac{1}{T_{25°C}}\rightarrow$$

$$T_{NTC}[°C]=\frac{1}{\frac{1}{\beta}\cdot ln\left(\frac{R_{19}}{R_{25°C}}\cdot\frac{1}{\frac{U_{MCU}}{U_{out}}-1}\right)+\frac{1}{298.15\,°C}}-273.15\,°C \qquad (35)$$

Where R_{19} is resistance of the pullup resistor, $R_{25°C}$ is the nominal resistance of NTC at 25 °C and β is NTC coefficient. Note that in the last step of equation, 273.15 is subtracted to convert resulting temperature from Kelvins to degrees Celsius.

2.4 FPGA

Although many on chip solutions for DDS exist (even including DAC) that are inexpensive, FPGA based DDS generator was chosen for this task because of its versatility and option of adding logic analyzer and oscilloscope into the card as an external stack up PCB.

My previous experience with products from the company Xilinx (now AMD) as well as ownership of multiple development kits and a programmer for their FPGAs made me choose one of their integrated circuits, especially from Spartan 3A family.

XC3S200A is the final pick, even though it is near obsolescence, I chose it because of its leaded VQFP-100 package which will be easy to solder, inspect and debug.

2.4.1 Clock source

Because the FPGA hosts the DDS core responsible for the signal generation, it is important to equip it with a precise clock. The parameters of the clock will directly influence the DDS frequency accuracy.

The FPGA has two options: it can either use the onboard 10 MHz active oscillator or an external clock reference provided by the rack system. The use of external reference is useful if more of the AWG cards are used in a single rack, synchronizing their outputs.

This thesis will use the onboard crystal oscillator. In the end a 10MHz 25ppm clock was selected. The next figure shows the oscillator's circuit.

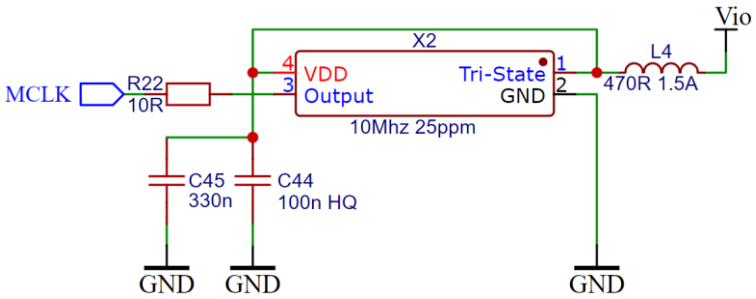

Figure 2.21: FPGA onboard oscillator circuit

A 10Ω resistor was placed between the oscillator's output and FPGA input to lower the capacitive loading of oscillator, which reduces the noise injected into power supply Vio.

2.4.2 Configuration Flash

Two external configuration flashes are used so that the user can select different architectures or functionalities. Configuration flashes U7 and U24 are connected to FPGA through SPI directly. XC3S200 has an inbuild SPI bootloader which supports only one config flash.

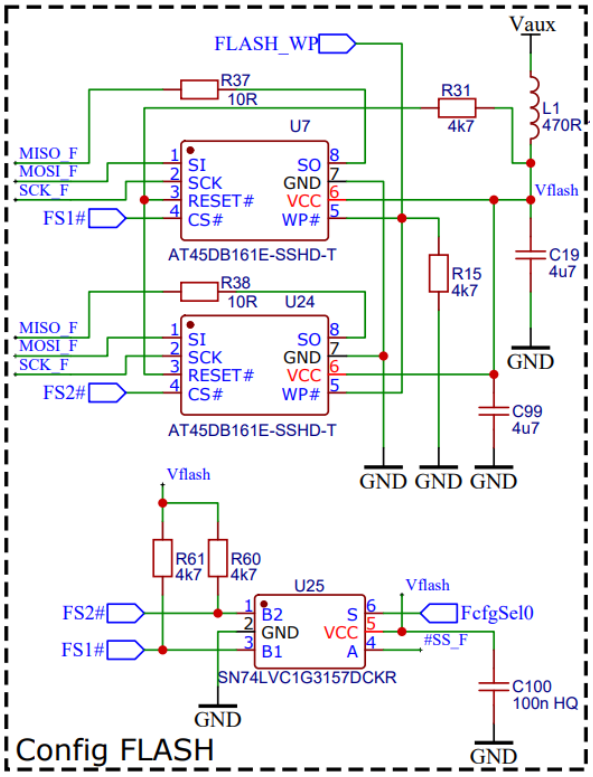

Figure 2.22: Multiple configuration flash schematic

That's why the slave select signal #SS_F is routed thru a solid state SPDT switch U25. This way the MCU can control which of these flash ICs is used via FcfgSel0 signal.

Also, the MCU can lock both flashes via FLASH_WP signal, preventing users from reprograming them.

2.4.3 Configuration modes

Spartan 3 has multiple ways of configuration: JTAG, serial, parallel and SPI. On powerup or after reset, the FPGA samples mode pins M0, M1 and M2 and launches bootloader accordingly.

Table 2.2: SPARTAN 3 self-configuration modes [7]

	M0	M1	M2
Master serial	0	0	0
SPI (Serial Flash)	1	0	0
Internal Master SPI	1	1	0
BPI (Parallel flash)	0	1	0
JTAG	1	0	1
Slave Serial	1	1	1
Slave Parallel	0	1	1

Only SPI Serial Flash and JTAG modes will be used, Serial Flash as a Non-volatile memory intended for normal operation and internal volatile memory loaded from JTAG for faster programming and debugging.

2.4.4 Flash version selection

To select Flash paging, version select pins VS0, VS1 and VS2 are used according to the following table.

Table 2.3: Flash version select pins [7]

VS[2:0] Pins			Read Command	Hexadecimal Command Code	Address Bits	Dummy Bits
VS2	VS1	VS0				
1	1	1	Fast Read	0x0B	24 bits, all zeros	8 bits, all zeros
1	0	1	Read	0x03		None
1	1	0	Read Array	0xE8		32 bits, all zeros
Others			Reserved			

Since VS pins have an internal pullup, 0Ω pulldown resistors are used to select the correct version.

2.5 MCU

A microcontroller is used to ease the user interface, communicate with other cards in rack, configure FPGA and supervise whole board.

Like FPGA manufacturer selection, I choose STMicroelectronics because of my previous experience. STM32F103C6T6 (U6) was my final pick because of its popularity and large RAM and FLASH sizes compared to its price.

2.5.1 EEPROM

To store device settings, external EEPROM was added. This way the user can store his preset in nonvolatile memory rather than RAM which will be erased on reset or power cycle.

M24C64, a 64-kb I2C EEPROM (U17) was selected due to its availability, low price and compatible pinout with EEPROMS from other manufacturers.

2.5.2 Clock sources

Because the device uses RS485, which is an asynchronous communication protocol, ceramic resonator (X1) is used for generating MCU system clock. The stability of ceramic resonators is far greater than the internal RC oscillator of the MCU. The resonators frequency is 8 MHz, which is then multiplied by the internal PLL of the MCU to 72 MHz.

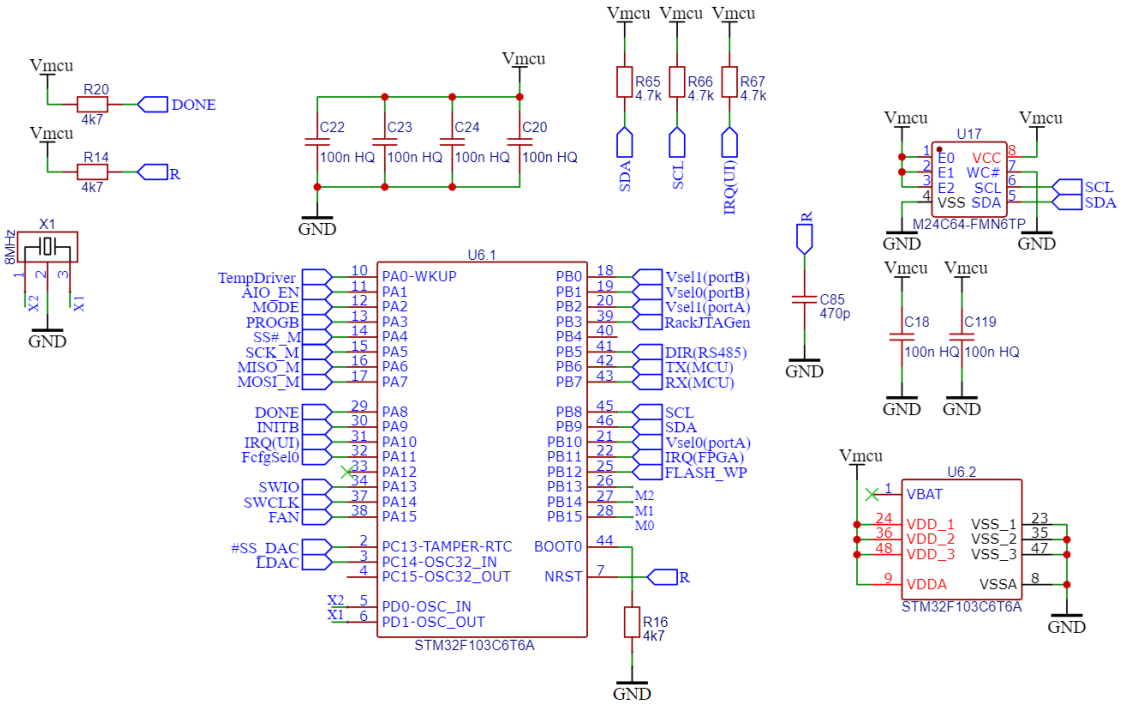

Figure 2.23: Schematic of the MCU

A pulldown resistor is connected to boot pin, setting the bootloader option to boot from internal flash memory, which is the most common way of configuration.

2.6 Power supply

Since one of the main features of this device is its isolated output, an isolated DC-DC converter needs to be used. There will be 2 types of isolated DC-DC converters: Programmable high-power used for output amplifier and fixed low-power used for digital and analog circuitry.

2.6.1 Power supply for digital part and analog

A voltage of 5 V will be needed for the DAC, digital level shifters and active cooling, a 3.3 V for FPGA and MCU and a 1.25 V for FPGA core. An isolated DC-DC power module AM2DS-0507SJZ is used for this purpose. It is a 7.2V output variant with the maximum output current of 278 mA. A higher voltage than the required 5 V was selected because the output voltage varies with output current, as shown in the figure below.

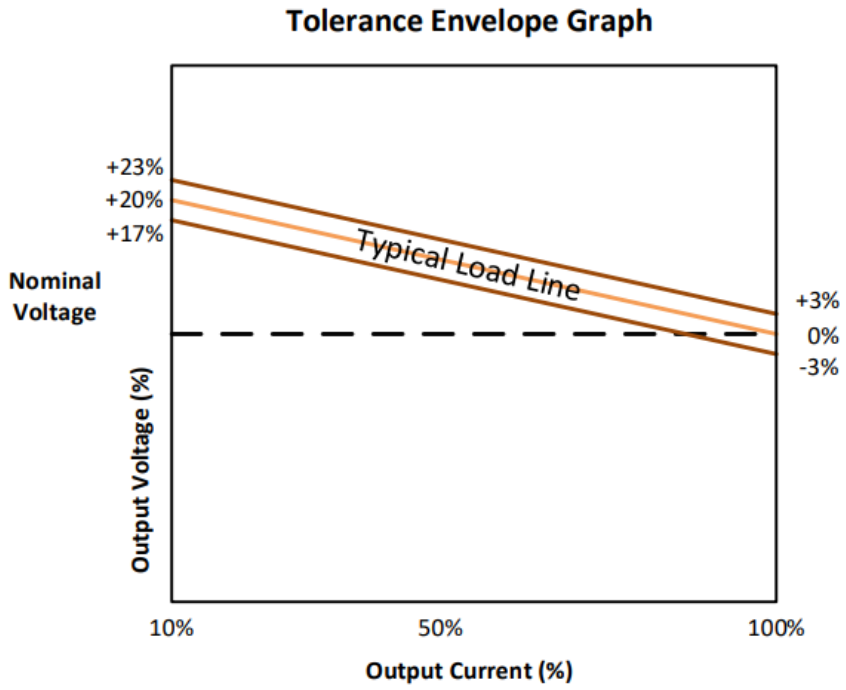

Figure 2.24: AM2DS-0507SJZ load characteristics [12]

From Figure 2.24 it can be seen that when the DC-DC converter is unloaded, the output voltage can be higher by up to 23% than its nominal voltage. If the 5V output variant was connected directly to the DAC and level shifters, with no load, the output voltage would be 6.4 V, almost 1 V higher above maximum operating area. This could be fixed by lowering the voltage through an LDO, but it would require a voltage headroom of at least 0.4 V at the maximum current. That's why a 7.2V variant is used. It is connected directly to the cooling fan and its voltage is lowered via series of LDOs.

For the 5V digital and DAC supply, 2 LDOs with 5V output are used, one for DAC and one for level shifters to decrease the power supply noise for DAC.

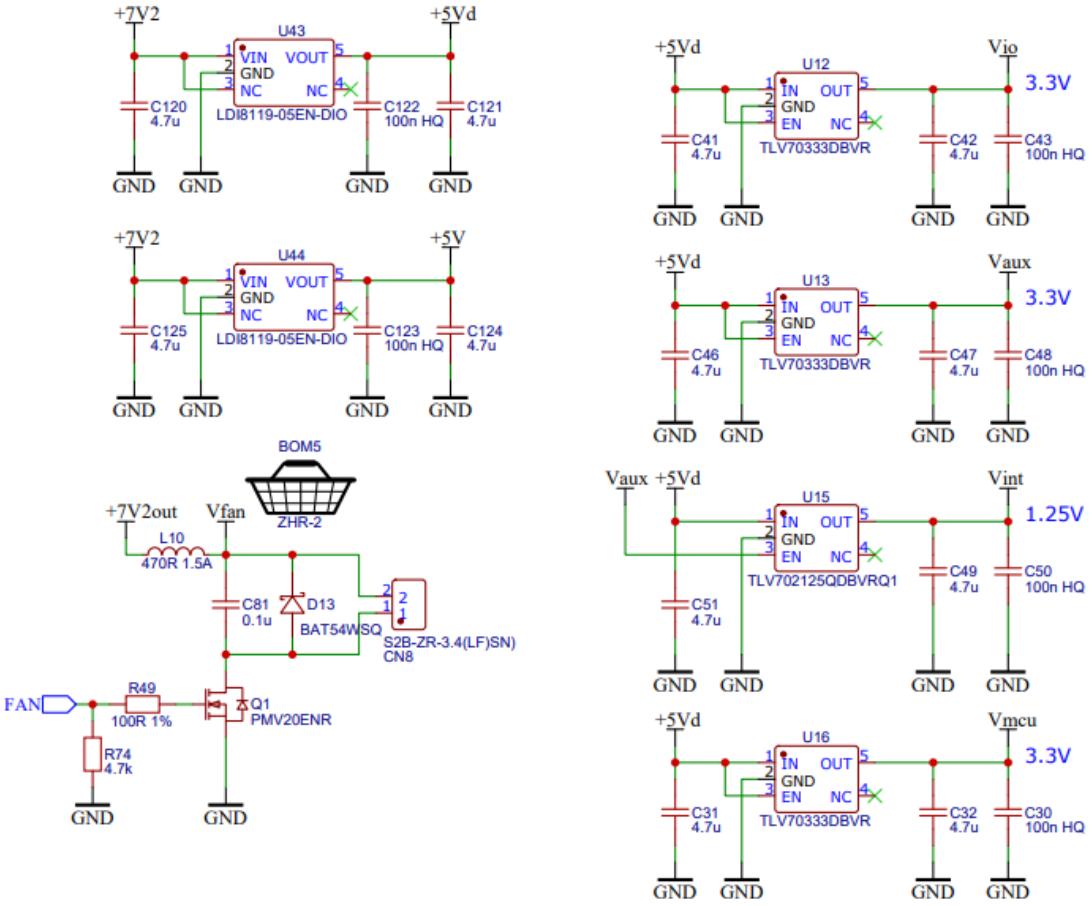

Figure 2.25: Digital and DAC power supply circuit with fan driving circuit

After the 5V conversion, another set of LDOs will convert it to 3.3 V. A separate LDO U16 is used for powering the 3.3 V MCU and 3 LDOs for the FPGA. As recommended by the manufacturer [15], LDO U12 powers the I/O banks, LDO U13 powers the auxiliary circuits such as JTAG core and bootloader and U15 powers the FPGA's core.

The design guide also stated that for lower power consumption, Vint (FPGA core) needs to be the last to receive power. By connecting the enable signal of U15 to auxiliary power it is assured that it will be turned on only after the Vaux and Vio.

2.6.2 Power supply for output amplifier

As described in previous chapters, it is highly inefficient to have a fixed power supply when outputting low voltage signals into low impedance loads. It is caused by the large voltage drop across amplifier's transistors. With programmable power supply this drop can be mitigated. The requirements for this module are:

1. Input voltage independence: the output voltage shall remain constant even when the input voltage changes.

2. Programmable output voltage: the output voltage shall be controlled via microcontroller.
3. The power supply shall have 2 channels, one for positive and one for negative voltage.
4. Both channels must be independently programmed.
5. Input voltage range: 10 V to 25 V.
6. Output voltage range: 5 V to 20 V and -5 V to -20 V.
7. Output current: >500 mA.

The power supply was created by modifying LTC3803 recommended circuit. It is a constant frequency 200kHz current mode flyback regulator. The main advantage of this integrated circuit is its ability to operate at large input voltage span. The IC doesn't feature internal MOSFET as some converter ICs do, which will lead to increased size of the converter on the circuit board, but allows easy replacement and upgrade of the MOSFET, potentially increasing PSU's power capability.

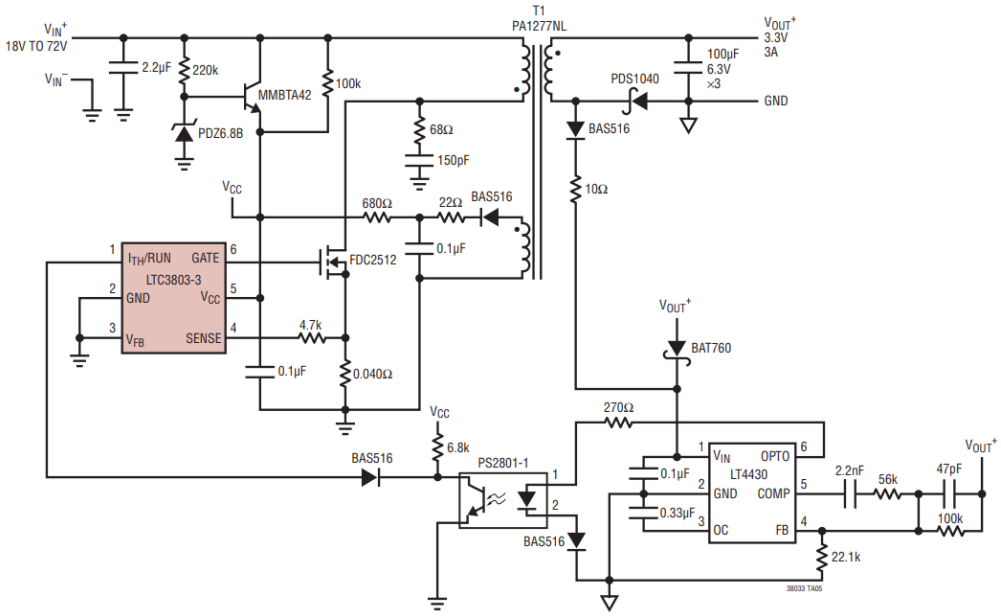

Figure 2.26: Typical application of LTC3803 as isolated Flyback DC-DC converter [24]

Figure 2.26 shows a schematic that is recommended by the manufacturer. In this case, the feedback pin of the LTC3803 is tied to ground meaning that the PWM output (pin GATE) will switch at full duty cycle. The only way to limit the duty cycle and decrease the output voltage is through I_{TH}/RUN pin.

Optocoupler PS2801 acts as current sink controlled by voltage on isolated side provided by LT4430, an optocoupler driver with integrated reference. This is the component that is responsible for regulation of the isolated voltage. The figure below shows the schematic of the modified positive programmable DC-DC.

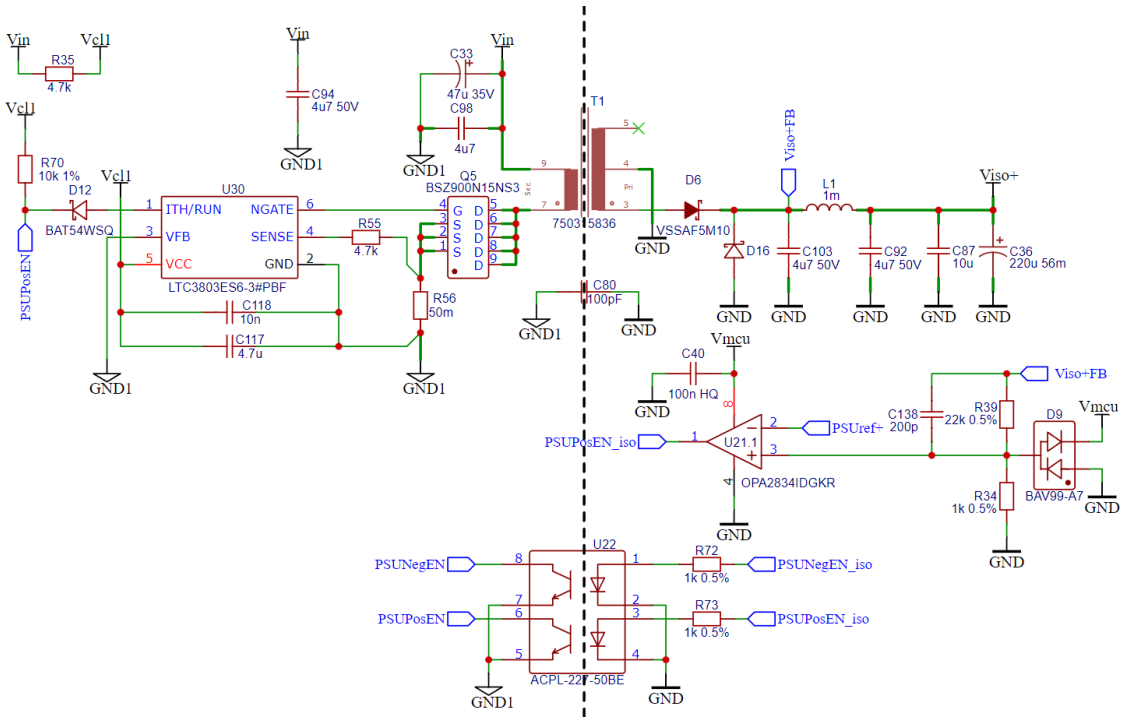

Figure 2.27: Isolated programmable DC-DC converter

The original circuit provides fixed voltage at the output, which can only be changed by altering feedback voltage divider ratio. This is why LT4430 was replaced by its equivalent circuit composed of more discrete components and thus the circuit displayed in Figure 2.27.

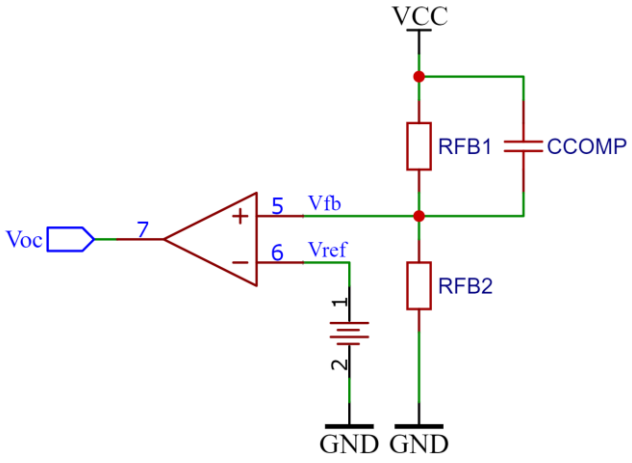

Figure 2.28: Simplified circuit of feedback regulator for positive supply

Figure 2.28 shows the circuit substituting function of LT4430. VCC is the output voltage, RFB1 and RFB2 form a feedback voltage divider and CCOMP is used for compensation of the feedback delay. Note that despite the voltage feedback being fed into the noninverting pin of OPAMP, the feedback type is still negative because increase of

OPAMP's output V_{OC} will result in more current being sunk from I_{TH}/RUN pin of LTC3803 which in the end will decrease the regulated voltage VCC.

The output voltage is determined by the voltage divider ratio and voltage reference V_{ref}. OPAMP will achieve its regulation when both inputs have the same voltage:

$$V_{ref} = V_{fb} = V_{CC} \cdot \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \rightarrow V_{CC} = V_{ref} \cdot \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \tag{36}$$

From formula 36 can be seen that the output voltage can be altered not only by changing the divider ratio as mentioned before but also by varying the reference voltage V_{ref}. Because the DAC, acting as V_{ref} source, will be fed with already existing onboard 2.5V reference voltage, divider ratio can be calculated:

$$V_{CCMAX} = V_{DACMAX} \cdot \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \rightarrow \left(\frac{V_{CCMAX}}{V_{DACMAX}} - 1\right) = \frac{R_{FB1}}{R_{FB2}} \tag{37}$$

For the R_{FB2} value of 1 kΩ was selected because of its previous use in other modules.

$$\left(\frac{V_{CCMAX}}{V_{DACMAX}} - 1\right) \cdot R_{FB2} = R_{FB1MIN} \rightarrow \left(\frac{20\ V}{2.5\ V} - 1\right) \cdot 1\ k\Omega = 7\ k\Omega \tag{38}$$

To further decrease the variety of different resistor values used, a 10kΩ resistor will be used. This will result in higher maximum output voltage and larger setting voltage step. The new maximum output voltage can be now derived:

$$V_{CCMAX} = V_{DACMAX} \cdot \left(1 + \frac{\mathrm{R_{FB1}}}{\mathrm{R_{FB2}}}\right) = 2.5\ V \cdot \left(1 + \frac{10\ k\Omega}{1\ k\Omega}\right) = 27.5\ V \tag{39}$$

Negative power supply will be designed with similar approach. However, because of its reversed polarity, the feedback circuit must be different.

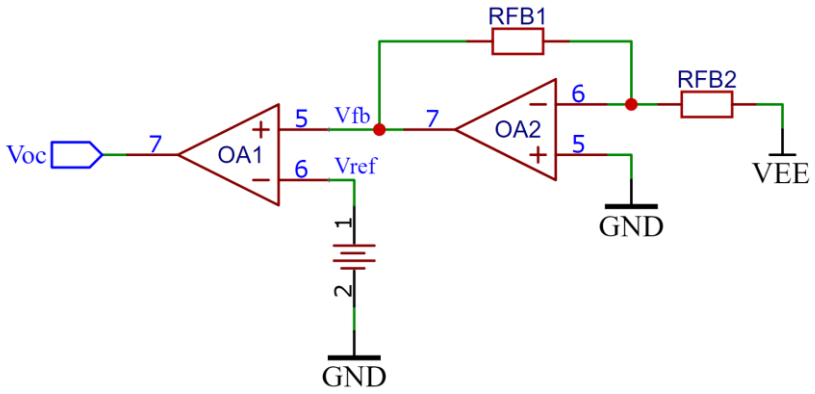

Figure 2.29: Simplified circuit of feedback regulator for negative supply

Operational amplifier OA1 expects positive voltage input, meaning that the negative voltage VEE needs to be inverted. OA2 together with R_{FB1} and R_{FB2} form an inverting amplifier, taking care of inverting the sensed voltage as well as scaling it down. Again, formula 40 can be derived for regulated state when both inputs of OA1 have the same voltage:

$$V_{ref} = V_{fb} = V_{EE} * GAIN = V_{EE} * -\frac{R_{FB2}}{R_{FB1}} \rightarrow V_{CC} = V_{ref} * \left(-\frac{R_{FB1}}{R_{FB2}}\right) \quad (40)$$

This formula shares similarities with the formula used for positive feedback, but the main difference is that there is no addition of 1 to the resistor ratio.

$$\left| V_{ref} * \left(-\frac{R_{FB1}}{R_{FB2}}\right)\right| \approx \left|V_{ref} * \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)\right| \dots \left\{if\ \frac{R_{FB1}}{R_{FB2}} \gg 1\right\} \quad (41)$$

The resistors ratio R_{FB1}/R_{FB2} will be around 10, and the addition of 1 will only introduce a negligible error to the maximum voltage setting, therefore same resistor values will be used as for the positive feedback circuit. The maximum negative voltage that can be produced by this circuit is:

$$V_{EEMAX} = V_{DACMAX} * \left(-\frac{R_{FB1}}{R_{FB2}}\right) = 2.5\ V * \left(-\frac{10\ k\Omega}{1\ k\Omega}\right) = -25\ V \quad (42)$$

Because the precision of the power supply nor its step size isn't important, an 8-bit DAC will suffice. The used component MCP47FEB02A0 is dual DAC controlled via I2C. If necessary, it can be replaced by its pin-to-pin compatible alternatives with higher resolution (10-bit or 12-bit).

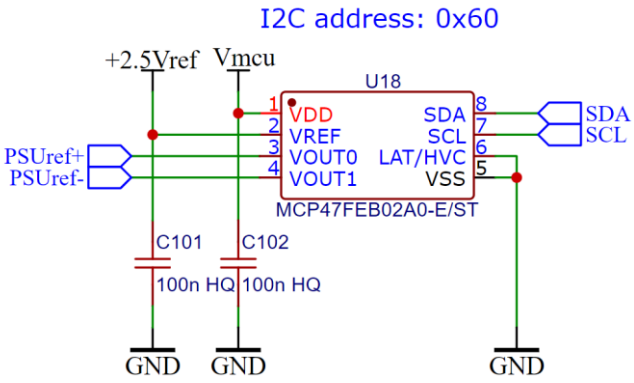

Figure 2.30: PSU reference DAC circuit

Figure 2.30 shows the circuit of DAC that functions as programmable voltage reference for the feedback circuitry, ultimately setting the PSU output voltage.

3. PRACTICAL IMPLEMENTATION

This chapter covers the mechanical implementation of the device, with a focus on PCB layout and thermal management. The figures below show pictures of the complete device.

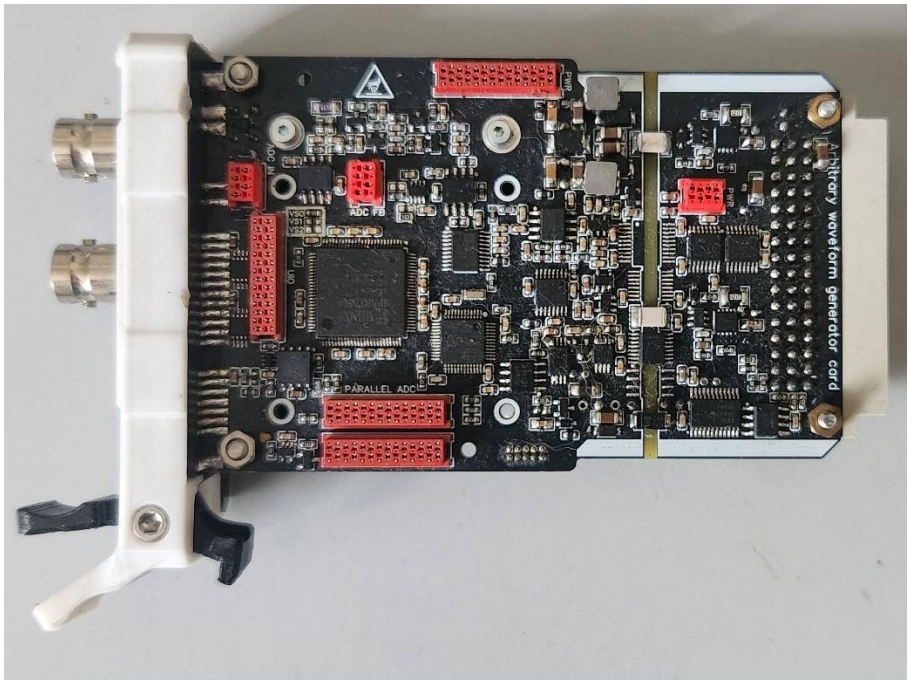

Figure 3.1: Top side of the device

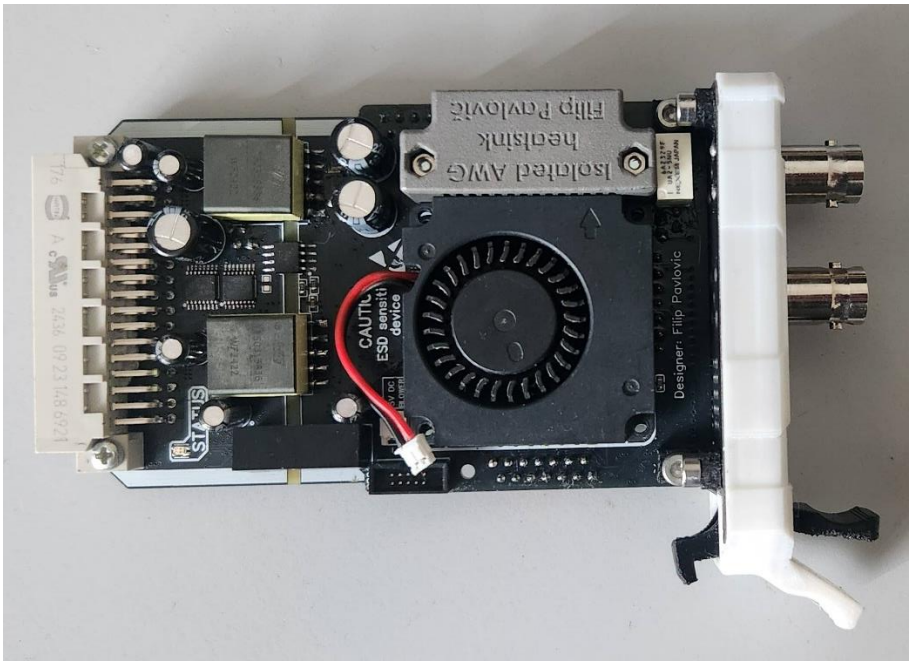

Figure 3.2: Bottom side of the device

The following subchapters will provide the layout of the PCB, explain the placement of the components and the design of the cooling system.

3.1 PCB layout

Due to the presence of switching power supplies and high-speed digital circuits, careful layout is required to prevent noise from interfering with the analog circuitry.

The simplest precaution that is taken is a 4-layer design, where one internal layer is dedicated for ground connection and one for the power supply traces. This will decrease the area of the ground loops and decrease the power supply impedance.

The second precaution involves dividing the functional blocks into the following groups:

1. High power supply
2. Digital power supplies
3. Digital circuits
4. Power amplifier
5. Low power analog

Careful placement of these blocks on the circuit board will decrease the crosstalk and noise. The goal is to maximize distance between the digital and analog sections while keeping the overall board dimensions as compact as possible.

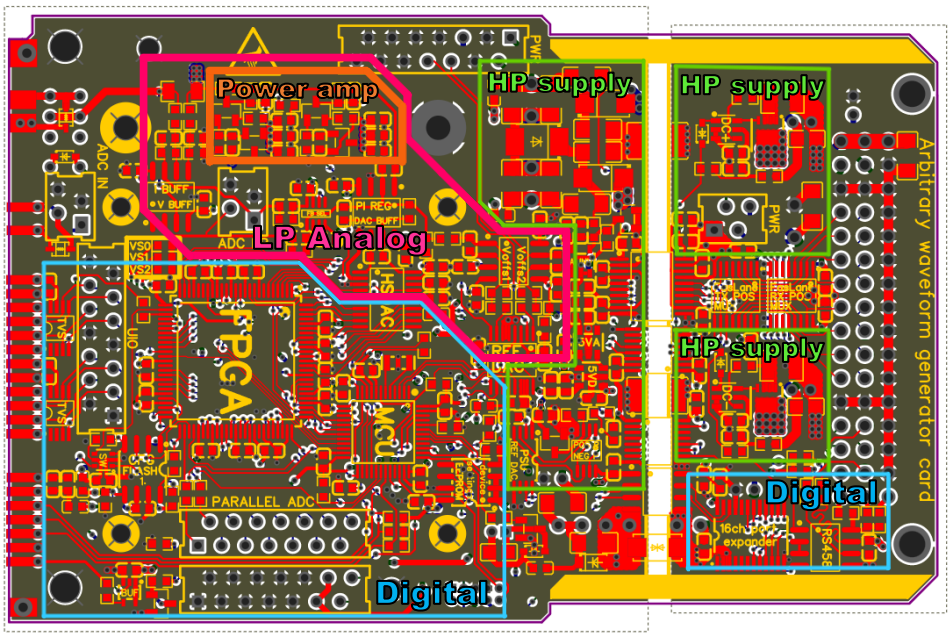

Figure 3.3: Board layout with highlighted circuit segments (Top side)

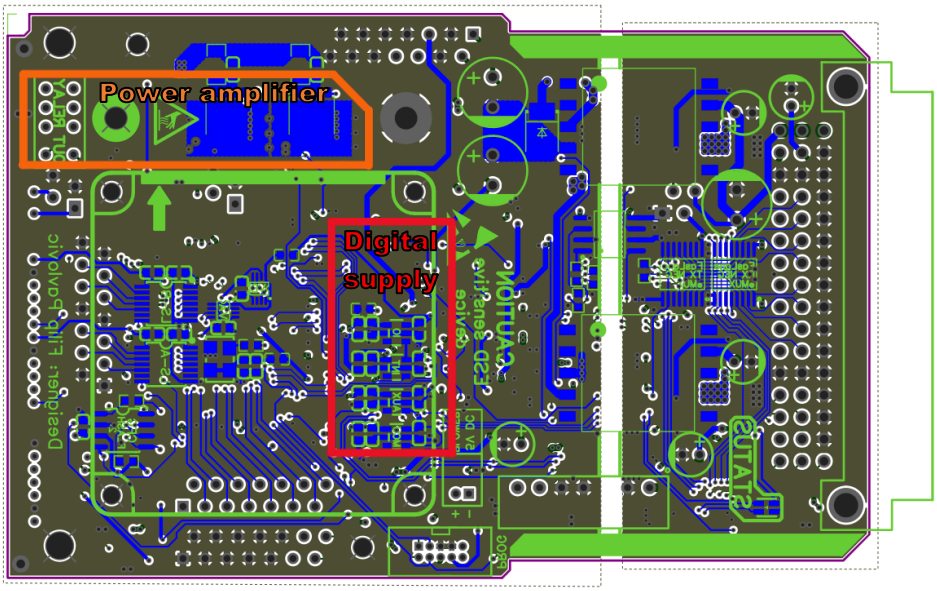

Figure 3.4: Board layout with highlighted circuit segments (Bottom side)

To simplify the assembly process, most of the SMD components were placed on the top layer, while the THT components are positioned on the bottom layer.

3.2 Thermal management

In the 3.1 PCB layout chapter it was mentioned that the output amplifier can dissipate 7W of thermal power in worst case situations. That's why this subchapter will focus on the design of the cooling system.

A custom made heatsink was necessary to fit within the devices boundaries while dissipating enough heat for the device to function properly even at higher loads.

The heatsink was designed and simulated in SolidWorks. A trial-and-error method was used to determine the optimal fin dimensions and spacing, which turned out to be 1 mm for both.

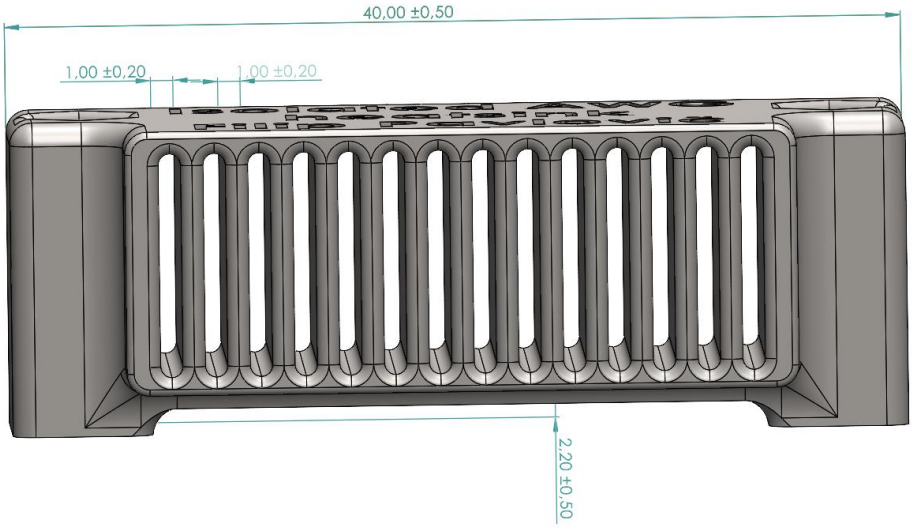

Figure 3.5: 3D model of heatsink

As the next step, a simplified board model was created, containing a base plate with the FR4 material, internal copper layer, both transistors modeled as rectangles with thermal properties of epoxy resin and the custom heatsink.

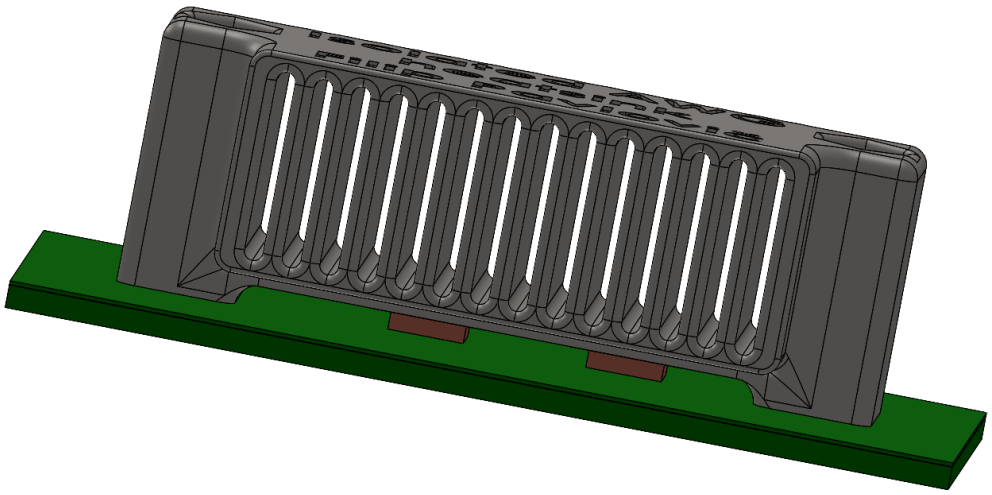

Figure 3.6: Heatsink simulation assembly

The ideal material for heatsink would be copper or aluminum for its high thermal conductivity, but unfortunately due to the small size of fins a custom CNC machined part would greatly increase the overall price of the device. This is why SLM (Selective laser melting) manufacturing was chosen.

The method shares similarities with 3D printing. Both are additive manufacturing processes, meaning that the cost is 5 times lower than conventional CNC machining [16]. The main downside is that the thermal conductivity of stainless steel is very poor when compared to popular heatsink materials such as copper or aluminum.

Table 3.1: Considered materials and their thermal conductivity

Material	Thermal conductivity [W ·m^{-1} ·K^{-1}]
aluminum	237
copper	401
stainless steel	15,1

Based on these values, a thermal simulation was made. An active cooling is used to improve the heat transfer from heatsink to air. The results are displayed on the figure below:

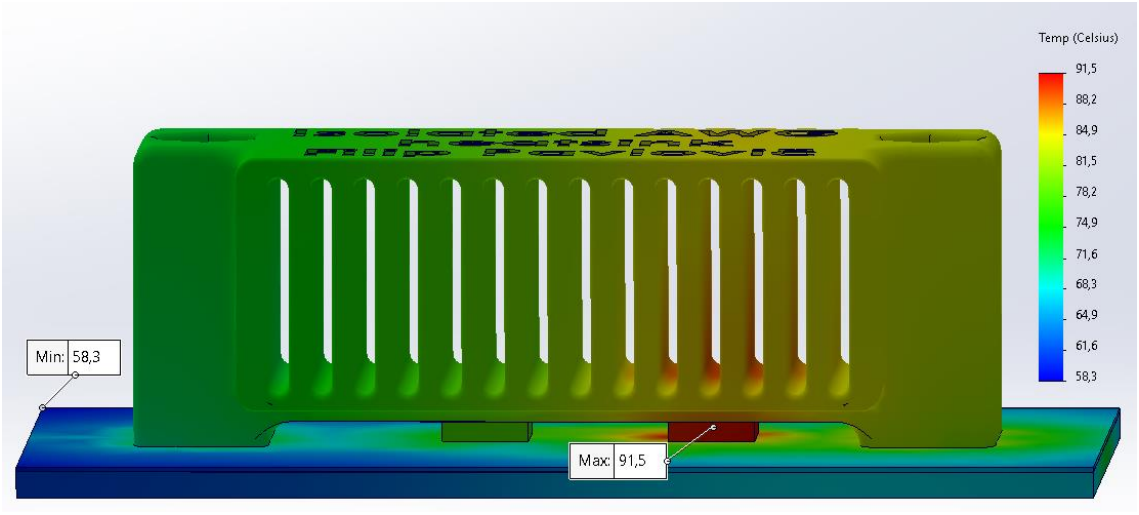

Figure 3.7: Static thermal simulation graphical results

The static thermal simulation result shown in Figure 3.7 reveals that the active transistor in the power amplifier block heats up to maximum of 91.5 °C at maximum the power dissipation of 7.5 W instead of 150 °C when cooled without heatsink.

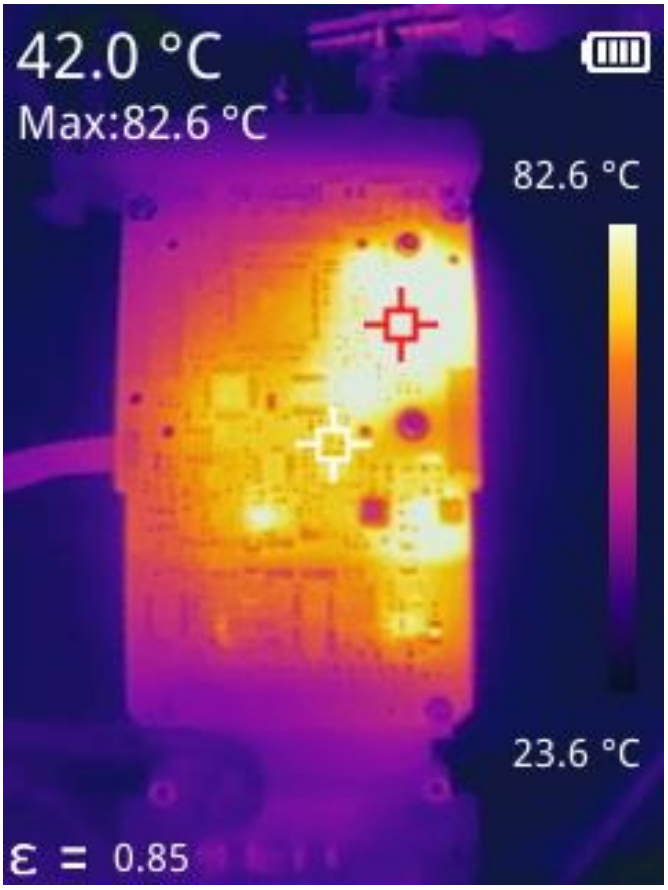

Figure 3.8: Thermal image of the device under maximum load

Figure 3.8 Shows the thermal image of the device when outputting 1 A and 10 V. The configuration was made so that the power amplifier will dissipate around 7.5 W of power. This experiment proved that the temperature doesn't rise above 90 °C as in the simulation.

4. FIRMWARE

The previous chapter explained the hardware of AWG, from the power supplies to the amplification and analog processing of the raw waveform provided by DAC. These functional blocks are essential to the device's operation, but for the generator to work at all, the DAC must receive a digital stream of data containing quantized points of the desired waveform.

This chapter will describe the digital aspects of the device, from user interface to signal generator core.

4.1 FPGA structure

The FPGA is the "hearth" of this device, responsible for generation of the waveform in digital format that is fed into the DAC. The firmware can be separated into three parts:

1. Communication
2. Clock management
3. DDS core

The device firmware was coded in Verilog using Xilinx ISE design suite.

4.1.1 Communication

The FPGA acts as a 4 wire SPI-inspired slave, receiving commands and data from the microcontroller. This type of communication protocol was selected because of its speed, simplicity and easy implementation into the programmable logic.

The data width of one frame is 32 bits, with the first 24 bits containing data and the last 8bits are the address of the internal register, to which the data are assigned.

Table 4.1: Data frame format

31 (MSB)	…	8	7	…	0 (LSB)
Data [31:8]			Reg Address [7:0]		

Table 4.2: FPGA configuration registers map

Register address	Register name	Register description	READ/ WRITE
1	AWG_D [LSB]	Least significant 24bits of DDS frequency control word	**W**
2	AWG_D [MSB]	Most significant 24bits of DDS frequency control word	**W**
3	ENABLERS	Device functions enable register	**W**
4	DACdirectData	DAC digital offset	**W**
5	DDSdata	DDS lookup table amplitude data and address	**W**
19	FIRMWARE_ID	Identification code of the current FPGA firmware	**R**

The communication runs on 40 Mb/s, which minimizes the time it takes to load all waveform into the DDS lookup table. The communication is implemented by the following model.

```
module SPI32bit(
      input CLK, SCK, LOAD, MOSI,
      output MISO,
      output [31:0] RECEIVE_DATA,
      input [31:0] TRANSMIT_DATA
    );

      reg LOADdelayed, DELAY1, DELAY2 = 0;
      reg [31:0] RXDATA = 0;
      assign RECEIVE_DATA = RXDATA;
      reg [31:0] TXDATA = 0;
      assign MISO = TXDATA[31];

      always @(posedge SCK)   // MOSI handler
            begin
                  RXDATA[31:0] <= {RXDATA[30:0],MOSI}; //shift in
            end

      always @(posedge LOADdelayed or posedge SCK)    //MISO handler
      begin
            if(LOADdelayed)
                  begin
                        TXDATA[31:0] <= TRANSMIT_DATA[31:0]; //load
                  end
            else
                  begin
                        TXDATA[31:0] <= {TXDATA[30:0],1'b0}; //shift out
                  end
            end

      // delayed load signal for SPI transmission back to MCU
      always @(posedge CLK)
            begin
                  LOADdelayed <= DELAY2;
                  DELAY2 <= DELAY1;
                  DELAY1 <= LOAD;
            end
endmodule
```

The MOSI process together with register RXDATA form a serial in, parallel out shift register, responsible for input data reception. The shift register's clock input is taken directly from the SCK pin, making the reception asynchronous from FPGA's clock. The load pin is wired through the SPI module directly to the registers that are connected to the peripherals output, latching them after the reception is done.

The MISO process handles data transmission. It consists of a parallel in, serial out shift register TXDATA, and a delay line used for loading data into the shift register. When the master (MCU) transmits a message that gets recognized as read command by the FPGA's register decoder, the already prepared data of interest is routed into the

communication peripheral's input TRANSMIT_DATA. The load signal that signals the end of transmission from master gets delayed by 3 clock cycles and then loads the input data into the TXDATA shift register, preparing it to be clocked out by the master. This delay is used to compensate for the time it takes register decoder and other parts of FPGA to process the command. The master then sends another command or empty stream and at the same time receives requested data from the FPGA.

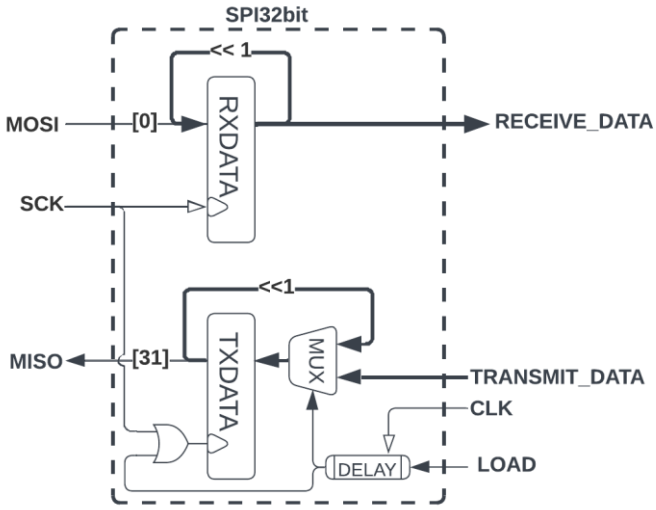

Figure 4.1: Functional diagram of SPI transceiver

Note that this implementation uses load signal instead of slave select. This means that the master must send a short pulse to this pin to latch the data that it just transmitted.

4.1.2 Clock management

As mentioned before, the DAC sampling rate is 20 MS/s. Since the provided external clock source has a frequency of only 10 MHz, a clock multiplier needs to be used to generate the required clock. This is achieved by utilizing one of the FPGA's inbuild DCM blocks (Digital Clock Management).

This peripheral is commonly used as clock conditioning block, not only capable of frequency multiplication and division, but also phase shifting, jitter removal, clock buffering and clock skew reduction [13].

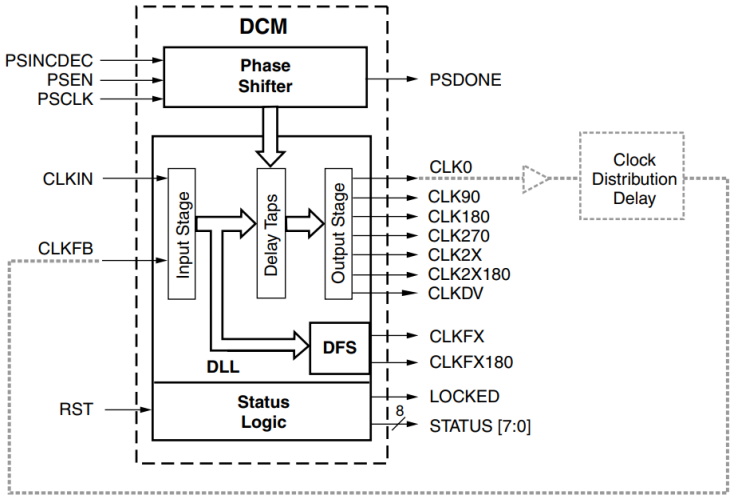

Figure 4.2: DCM Functional Block Diagram [13]

The selected XC3S50A features two DCMs, but only one will be used for DDS and SPI clock generation. The external clock is directly connected to the DCM's clock input CLKIN. Next the DFS (Digital Frequency Synthesizer) block is configured to multiply the clock by 4. This is achieved by setting the multiplier register to 4 and the divider to 1. The 40 MHz output is then routed from CLKFX pin to the communication block described in chapter 4.1.1.

To obtain the desired 20 MHz signal for DDS, the signal's frequency is conditioned by following circuit description.

```
always @(posedge SPI_CLK)
begin
      DDS_CLK <= ! DDS_CLK;
end
```

The process changes polarity of the output signal for each clock cycle, effectively halving its frequency.

4.1.3 DDS core

The implementation of DDS can be divided into 3 segments: the phase accumulator, the lookup table and the output enable gate.

For better resource utilization, internal RAM was used as the lookup table. This FPGA version features a 72 kbit distributed BRAM that can be configured in the following modes [14]:

1. **Single port:** allows access to only one word at a time.
2. **Simple dual port:** Provides one port for independent writing and another for independent reading.
3. **True dual port:** Offers two access points, both capable of writing and reading simultaneously. Writing conflicts are handled internally by the RAM.

Xilinx uses the term block RAM for this peripheral because it can be configured in these modes, but it works just like a regular parallel RAM.

The most suitable mode for this application is simple dual port. Port A is in write only mode and connects to the register decoder, allowing direct access to RAM through 4-wire. Port B is read only, and its address input is connected to the phase accumulators most significant bits. The output of this port is then fed through an enabling logic straight into the DAC.

The circuit description below shows implementation of the entire DDS module, featuring all three components:

```
module DDS(
      input CLK, EN, WR,
      input [23:0] D_MSB, D_LSB,
      input signed [11:0] DATA,
      output reg signed [11:0] OUT,
      input [10:0] ADDRESS
    );

//Phase accumulator
      reg [47:0] PhaseAccumulator = 0;
      wire [47:0] D;
      assign D = {D_MSB, D_LSB};

      always @(posedge CLK)
            begin
                  if(EN) PhaseAccumulator <= PhaseAccumulator + D;
                  else   PhaseAccumulator <= 0;
            end

      wire [11:0] sampleAddress;
      assign sampleAddress[11:0] = PhaseAccumulator[47:47-11];

      wire signed [11:0] AWGramOUT;

// output enable
      always @*
            begin
                  if(EN) OUT <= AWGramOUT;
                  else   OUT <= 0;
            end

// dedicated internal Block RAM
      AWG_BRAM AWGram (
        .clka(WR), // input clka
        .wea(1), // input [0 : 0] wea
        .addra(ADDRESS), // input [10 : 0] addra
        .dina(DATA), // input [11 : 0] dina
        .clkb(!CLK), // input clkb
        .addrb(sampleAddress), // input [10 : 0] addrb
        .doutb(AWGramOUT) // output [11 : 0] doutb
      );

endmodule
```

Content of PhaseAccumilator register is updated on each clock cycle with value depending on the enable input. If the DDS is enabled, it will be incremented by D, the DDS frequency control word. On the other hand, if the DDS is disabled, the register will be reset to 0, ensuring that the generator starts outputting waveform from beginning.

Because the control word's length is 48-bits and the maximum data length that can be received by the communication peripheral is 24bits (excluding the last 8 address bits), it is received in two messages containing first and last 24bits. The two are combined in this peripheral.

The last 12bits of the phase accumulator are connected to the block RAM's port A address input. Port B is used for loading the RAM with the waveform samples. The BRAM module was implemented using Xilinx ISE IP core generator tool, used for configuring FPGA peripherals.

The block output is routed to RAM's output if the DDS is enabled, otherwise the output is signed 0.

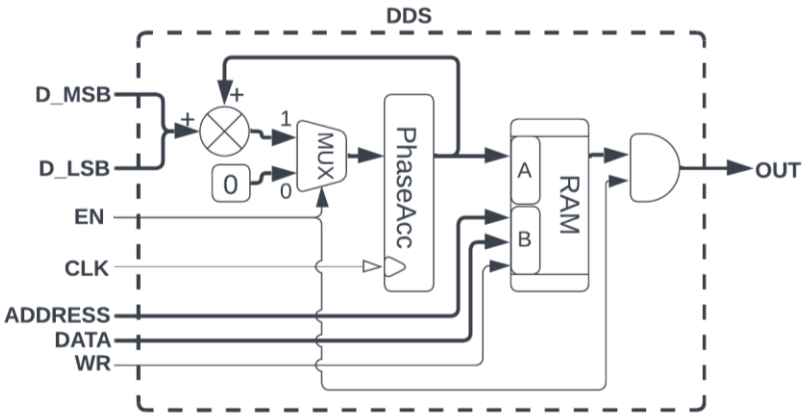

Figure 4.3: DDS Functional Block Diagram

The block diagram above shows simplified block diagram for the DDS peripheral. The output is directly connected to the high-speed DAC.

4.2 Microcontroller firmware

Another important part of the generator is the microcontroller. As mentioned before, its primary task is to oversee the device, monitor its temperature, configure FPGA, programmable power supplies and decode commands. The selected programming language is C and the STM32CubeIDE environment is used.

4.2.1 Temperature management

The MCU measures the temperature of the power amplifier and itself. The amplifier's temperature is crucial for controlling the cooling fan and overtemperature lockout of the output if the temperature is too high to prevent damaging the device.

The code implementation resides in ADC's interrupt routine that gets triggered after the conversion of all channels is complete. Next, the raw data is converted into temperature and the cooling fan speed is updated, as well as the overtemperature lockout state machine. The ADC conversion is periodically triggered via timer event with frequency of 10 Hz.

Both overtemperature lockout and fan control have hysteresis. If the temperature exceeds the 100 °C limit, the output is disabled and can be reenabled only when the output stage cools under 60 °C.

4.2.2 Command decoding

After the user sends command via RS485, it gets converted to UART and the DMA controller buffers the message in the RAM and triggers an interrupt routine when the communication line stays inactive for longer than 5ms. This UART mode ensures reception of messages with variable length and the usage of DMA controller offloads the MCU's core. Next, this command gets decoded, and the corresponding function gets called. The table below contains all the SCPI commands recognized by the device:

Table 4.3: SCPI commands

Command	Subcommand	Description	Read/ Write	accepted values
SYS	ID	returns unique ID of the device	R	N/A
	STATUS	returns FPGA configuration status	R	N/A
	TEMP	returns temperature of the AB amplifier [°C]	R	N/A
	RESET	resets whole device	W	1
	APPLY	apply all changes in settings	W	ALL, HFDAC, AWG
OUT	MAXAMPU	sets maximum output voltage in both current and voltage mode [V]	R/W	0 ... 20
	MAXAMPI	sets maximum current in current mode [mA]	R/W	0 ... 1000
	OFFSU	sets output offset in voltage mode [V]	R/W	-20 ... 20
	OFFSI	sets output offset in current mode [mA]	R/W	-1000 ... 1000
	MODE	sets voltage or current output mode	R/W	VOLTAGE, CURRENT
	EN	controls the output relay	R/W	ON, OFF
AWG	AMPU	sets the wave amplitude in voltage mode [V]	R/W	0 - 20
	AMPI	sets the wave amplitude in current mode [mA]	R/W	0 - 1000
	FREQ	sets the frequency [Hz]	R/W	0 - 2000000
	DC	sets the duty cycle [%]	R/W	0 - 100
	WF	selects the waveform type	R/W	Sine, Square, Triangle

The message frame is composed of a rack ID, which is a 3-digit number that specifies the position of card in the system, Command, Subcommand and value. The device responds back only if the sent ID and the binary code read from the backplane connector match.

The table below shows a few examples of commands and their usage:

Table 4.4: Typical SCPI communication example

Sent command frame	Typical response
000:AWG:WF:Sine	OK
000:SYS:STATUS ?	OK/ ERR INIT
000:OUT:EN:ON	OK/ ERR CFG
000:AWG:FREQ:100.0	OK
000:AWG:FREQ ?	100.0Hz

Note that if the response is ERR without any other specification shortcut, the command was not recognized by the device.

5. MEASUREMENTS

This chapter focuses on the verification of the function of the finished device in accordance with the requirements.

The now-complete device will be treated as a black box with a single output port. All measurements will be taken solely at the device's output, meaning no internal signals will be measured. The idea is that internal behavior is irrelevant as long as the output behaves as expected.

5.1 Output waveforms testing

This measurement serves only for detecting presence of desired waveform at the output with desired parameters. The waveform parameters will be selected far from the maximum operating range of the device, which are 1 MHz, 15 V and 1 A.

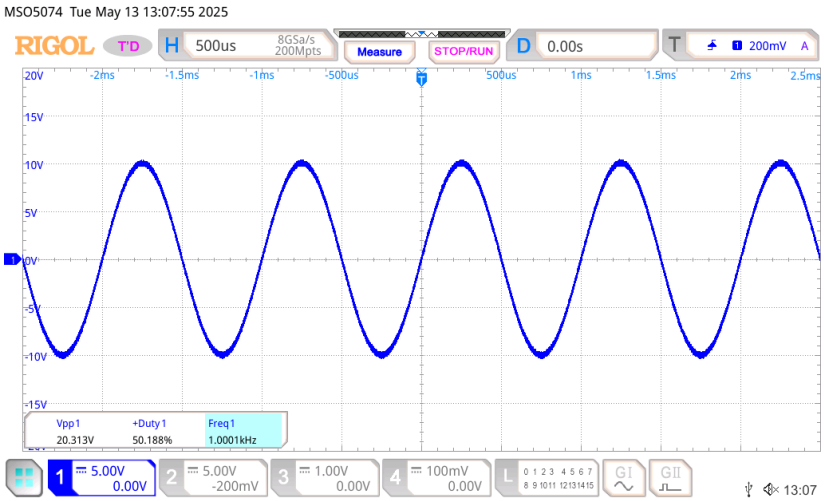

Figure 5.1: Sine waveform, 10 V peak, 1 kHz

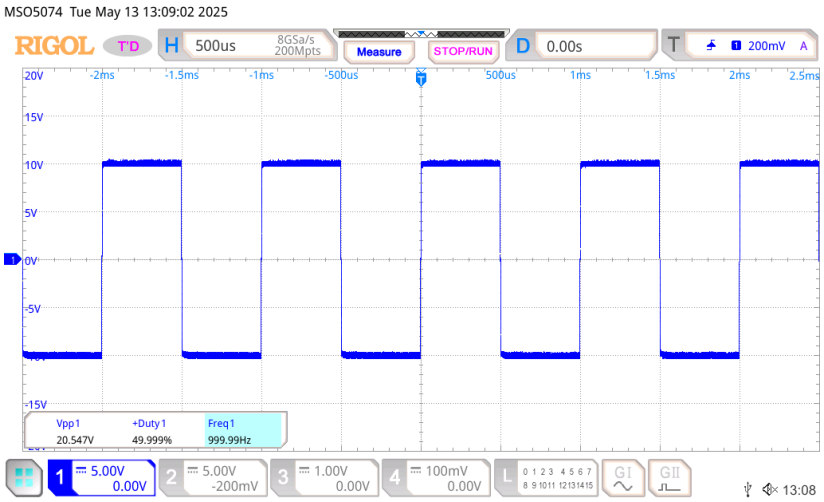

Figure 5.2: Square waveform, 10 V peak, 1 kHz, 50% duty cycle

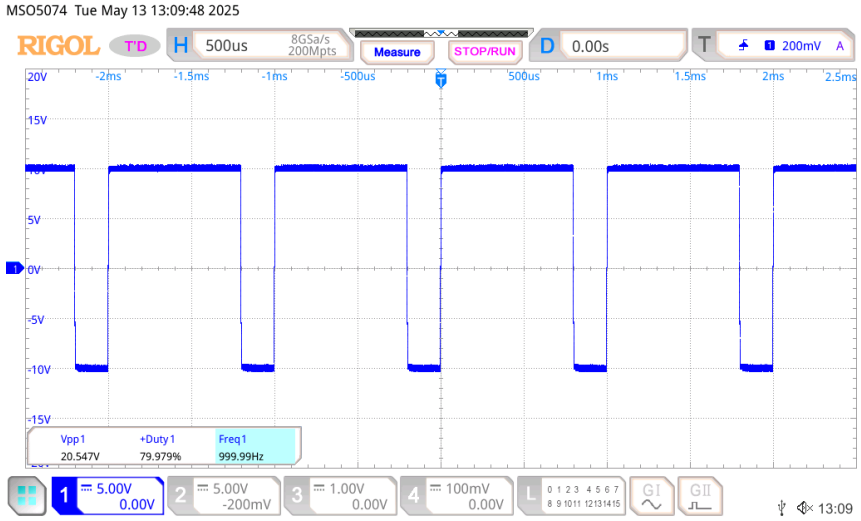

Figure 5.3: Square waveform, 10 V peak, 1 kHz, 80% duty cycle

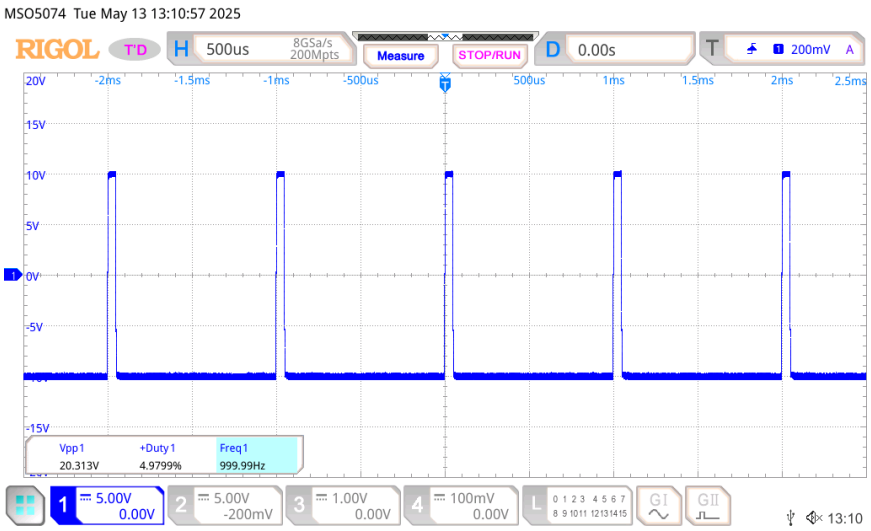

Figure 5.4: Square waveform, 10V peak, 1 kHz, 5% duty cycle

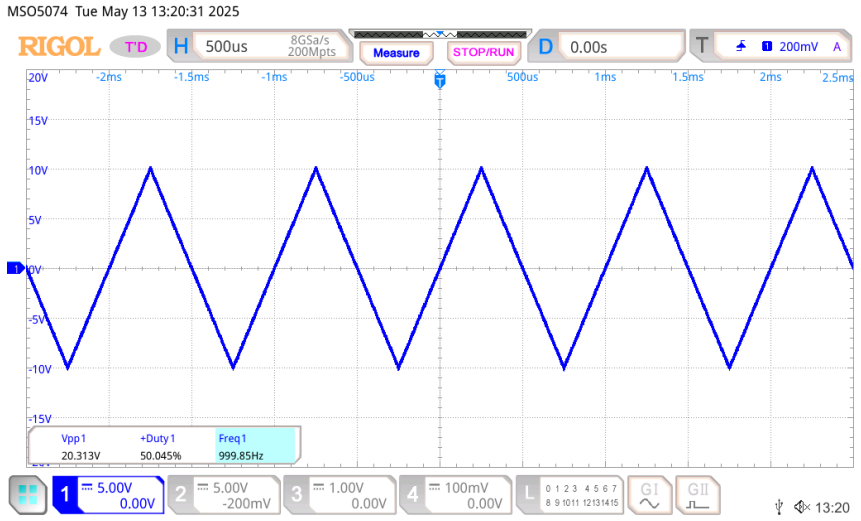

Figure 5.5: Triangle waveform, 10 V peak, 1 kHz, 50% duty cycle

Figure 5.6: Triangle waveform with 20% duty cycle

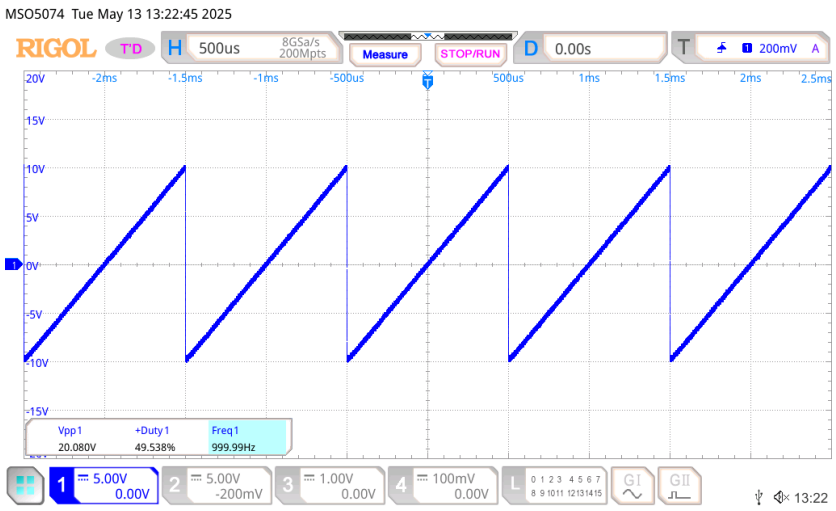

Figure 5.7: Triangle waveform with 100% duty cycle

This test proved that the generator is capable of producing 3 fundamental waveforms. The generated signals do not show any apparent flaws. For the last triangle waveform measurement 100% duty cycle was selected to effectively create a sawtooth wave.

5.2 DC loading characteristics

Because the generator was designed with high output current capability, it can be used as a programmable power supply. This can be achieved by setting the signal amplitude to 0 V and adjusting the offset voltage. By doing so, the power amplifier will be operating with highest efficiency.

One of the most important parameters of any power supply is its loading characteristics. It reveals the behavior of the output voltage when there is a large current draw from the output.

In ideal case, the voltage on output will remain the same no matter how large the current is, but of course that is not possible in real life. Not only does the switching power supply and output amplifier have their limitations, but also series resistances along the power path will cause the output voltage to drop. The simplified circuit representing the regulators is shown in Figure 5.8.

The output voltage or current should remain the same as long as both output amplifier and the switching regulator can compensate for the voltage drop caused by their internal resistances. A larger voltage headroom will allow drop compensation for higher currents, but it will decrease output voltage range and overall efficiency.

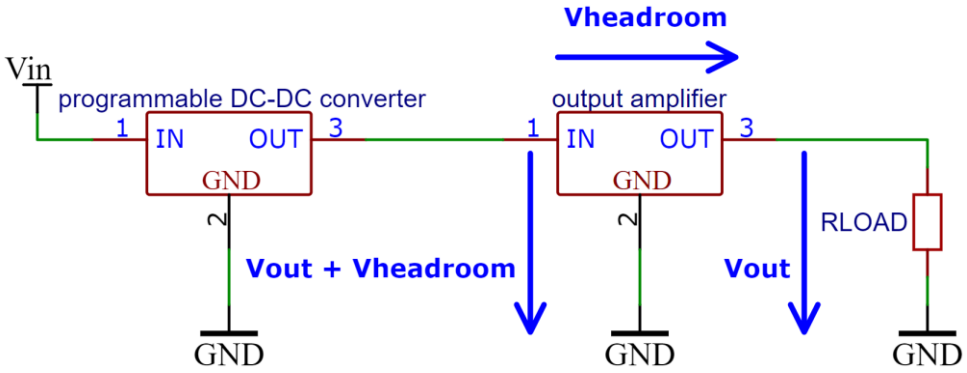

Figure 5.8: Equivalent circuit of AWG as power supply

The best headroom voltage was determined by real-life experiment, and its value is 1.6 V. Now the output voltage can be measured with respect to load current. The experiment will be conducted with 2 different voltage levels: 5 V, which is a common power supply voltage and 15 V, the maximum recommended output level.

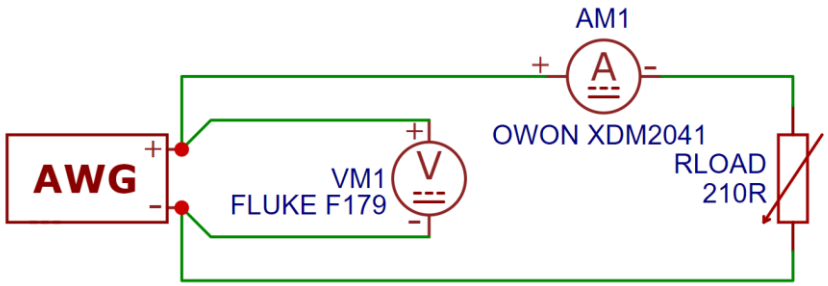

Figure 5.9: Schematic of loading characteristics measurement setup

Figure 5.9 shows the circuit diagram of the setup used to measure loading characteristics. First the generator ‘s output was set to voltage mode, and a DC value was entered. This value remained constant throughout the measurement. A table of load currents was generated, spanning from 0 mA to the maximum current of 1000 mA. Then,

the rheostat RLOAD was manually adjusted so that the ampere meter displayed the desired current and the output voltage was measured.

To obtain the best results, the voltmeter was connected directly to the generator's output.

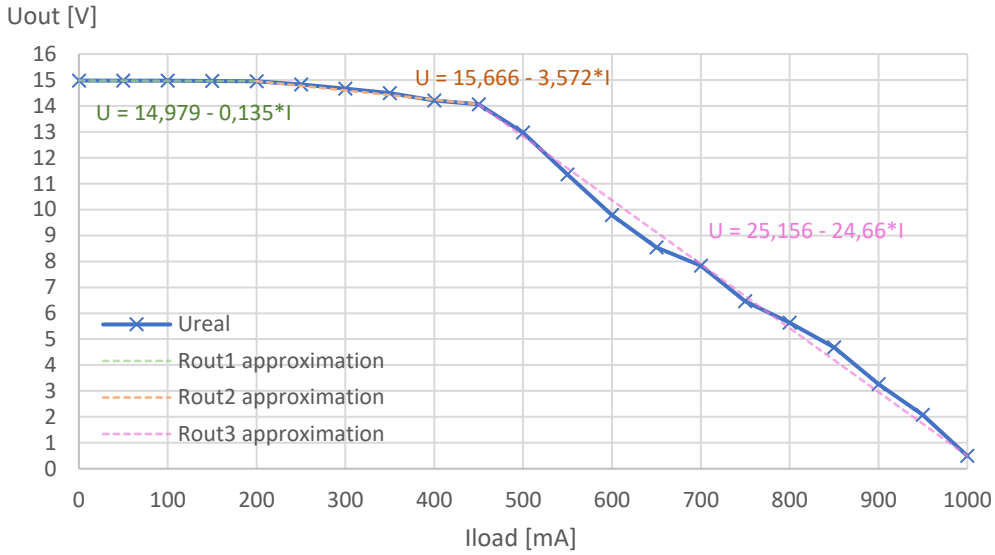

Figure 5.10: Output loading characteristics at 15 V

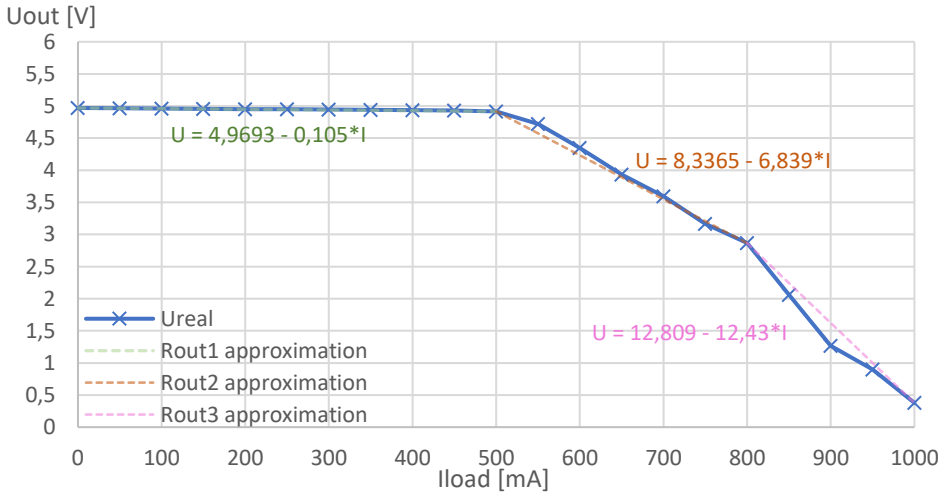

Figure 5.11: Output loading characteristics at 5 V

Figure 5.10 and Figure 5.11 show that the characteristics can be approximated by three linear segments, whose slope is equal to the output resistance. This means that the output resistance changes three times throughout the entire operating range.

Table 5.1: Measurement results of different resistance components

	5 V	15 V
R_{stray} [Ω]	0,135	0,105
R_{AB} [Ω]	3,437	6,734
R_{SMPS} [Ω]	21,088	5,591

These values shown in Table 5.1 were obtained by the following calculations:

$$R_n = \frac{dU}{dI} - R_{n-1} = \frac{\Delta U}{\Delta I} - R_{n-1} = \frac{U_2 - U_1}{I_2 - I_1} - R_{n-1} \tag{43}$$

Where R_n is the partial resistance of interest, R_{n-1} is the resistance calculated from previous slope. R_{n-1} is 0 for the first calculation. I_2 and I_1 are the highest and lowest currents where slope remains constant and U_2, U_1 are output voltages at given currents.

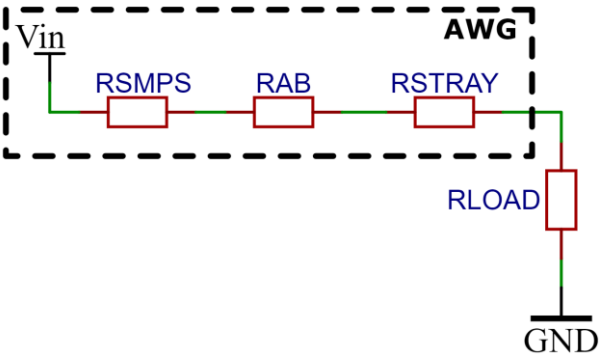

Figure 5.12: Equivalent circuit of internal resistance

The output resistance composes of R_{STRAY}, R_{AB} and R_{SMPS}. Figure 5.12 shows the equivalent circuit that is used to mathematically approximate the output resistance where R_{STRAY} is the resistance of the output connector and relay contacts, R_{AB} is the resistance of NPN transistor together with the current shunt and R_{SMPS} is the resistance of transformer's secondary winding together with its rectifier.

When the current is within specified range (0 – 500 mA and U = 5 V), both regulators are able to compensate for the voltage drop. In this case, R_{AB} and R_{SMPS} are zero and only R_{STRAY} takes effect. When the current is higher than the operating range, the output AB power amplifier cannot keep the output voltage constant because its headroom voltage budget is exceeded. This means that the output resistance is given by the sum of R_{STRAY} and R_{AB}. Finaly, with enough output current the switching power supply loses its ability to regulate.

5.3 DC voltage and current precision

Now, because some loads can be sensitive to power supply precision, it is essential to evaluate the DC precision of the output. This experiment will be conducted with the same AWG configuration as for the DC loading characteristics measurement, meaning that the amplitude will be set to 0 V or 0 mA and voltage or current will be controlled through offset. Both current and voltage precisions will be tested without loading the output externally, meaning that for the voltage mode, output will be left open and for current mode output will be shorted with an ampere meter.

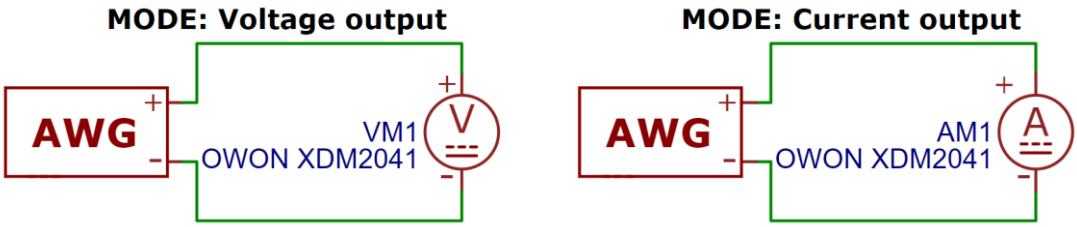

Figure 5.13: Schematic of DC precision of voltage and current measurement setup

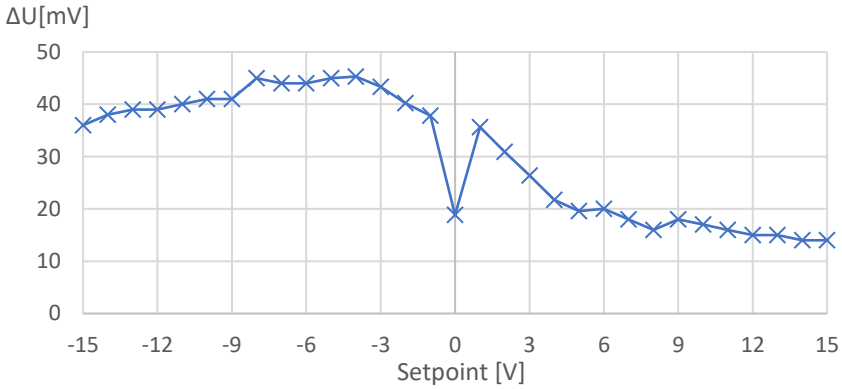

Figure 5.14: Absolute voltage error in relation to output voltage setpoint

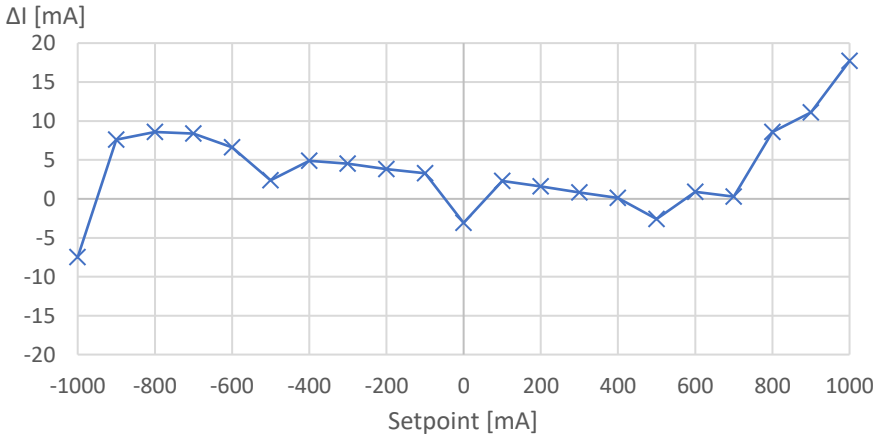

Figure 5.15: Absolute current error in relation to output current setpoint

Both characteristics displayed in Figure 5.14 and Figure 5.15 show signs of nonlinearity. This is due to the semiconductor analog switch that selects feedback source for the main regulator. Not only does it inject stray current into the regulator junction, which results in voltage/current offset, it also introduces parasitic resistance that varies with the input voltage. This resistance adds to the feedback resistors and alters gain of the regulator, making the output slightly nonlinear.

Table 5.2: Measurements result of DC offset

	Voltage mode		Current mode	
	Absolute	Relative	Absolute	Relative
Minimum error	14,00 mV	-3,78%	-7,50 mA	-3,30%
Maximum error	45,30 mV	3,56%	17,70 mA	2,30%
Standard deviation	11,75 mV	1,16%	5,37 mA	1,31%
Average error	30,15 mV	0,72%	5,08 mA	1,03%

The final results of this measurement are displayed in Table 5.2.

5.4 Frequency characteristics

The goal of this measurement is to test device output amplitude behavior in response to changing frequency. This is important because it will give us insight into what is the maximum achievable amplitude on specific given frequency. Tests will be conducted without output load connected and the maximum frequency will be 2 MHz to showcase generators behavior outside its operating range.

First, a table containing frequencies logarithmically distributed spanning from 10 kHz to 2 MHz was generated. Next, these frequencies were loaded into the AWG and output amplitude was measured with an oscilloscope. An average of 20 samples was used to obtain more precise data.

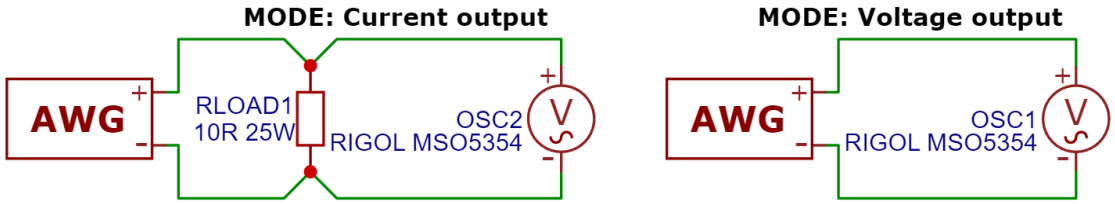

Figure 5.16: Schematic of frequency characteristics measurement setup

Because the oscilloscope can only measure voltage, in the current mode the current must be converted to voltage before measurement. The two available methods are current probe or shunt resistor. A 10Ω 25W wire-wound current shunt resistor was selected for its better precision and availability.

Because power resistors have loose tolerance, a 4-wire resistance measurement method was used to obtain the actual value of the resistor allowing for more precise current calculation. The biggest problem now is calculating shunt current at higher frequencies. This is because the wire-wound resistors behave like inductors, and their impedance increases with frequency. To counter this, first the inductance was measured using an RLC bridge and then the final formula was derived:

$$I_{out} = \frac{U_{shunt}}{Z_{shunt}} = \frac{U_{shunt}}{\sqrt{{R_{shunt}}^2 + (2\pi \cdot f \cdot L_{shunt})^2}} \tag{44}$$

Where U_{shunt} is the voltage measured directly across the shunt resistor with oscilloscope, R_{shunt} is the value measured via 4-wire method, L_{shunt} is the parasitic inductance measured using RLC bridge and f is the frequency.

The order of frequencies from the pre-made table was fed into generator in reverse, starting from 2 MHz. This allowed the extrapolation of amplitudes when they stopped changing on low frequencies. For better clarity, results for voltage mode were separated into two categories: small signal and large signal characteristics. The waveform used is sine.

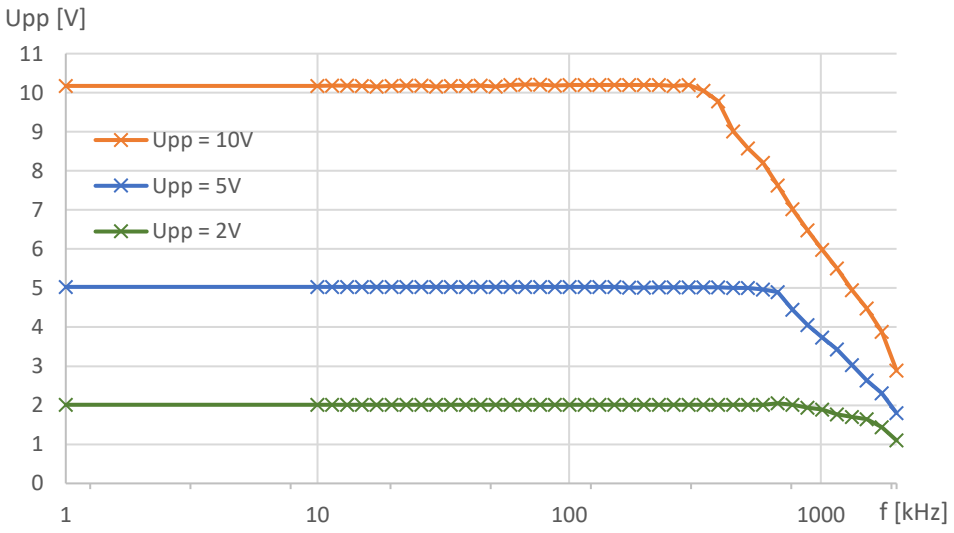

Figure 5.17: Frequency characteristics of small signals in voltage output mode

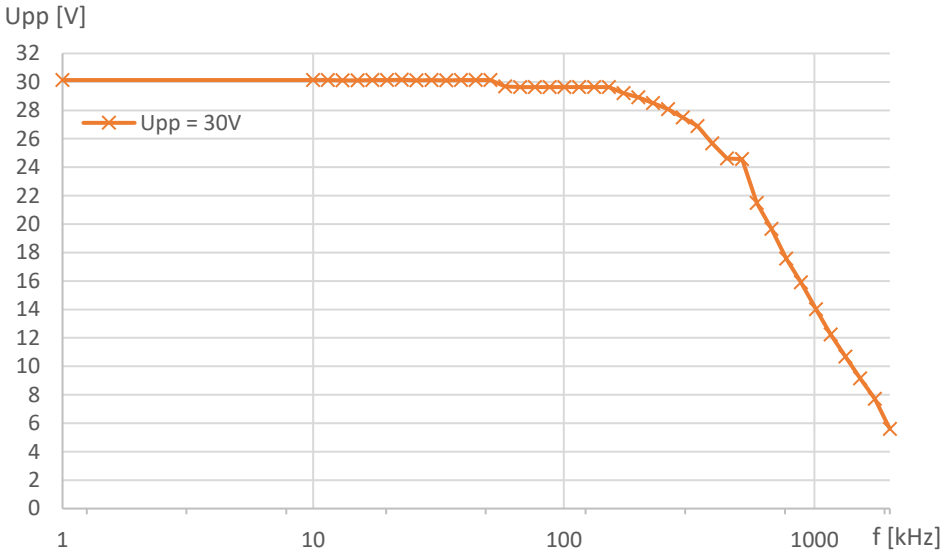

Figure 5.18: Frequency characteristics of large signals in voltage output mode

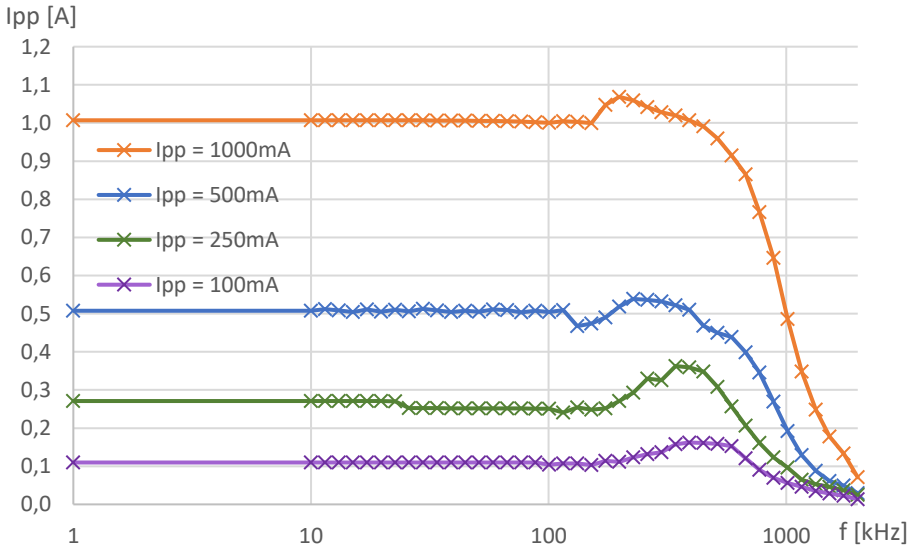

Figure 5.19: Frequency characteristics of the output in current mode

Figure 5.17, Figure 5.18 and Figure 5.19 show the output amplitude as a function of frequency. At low frequencies, the main regulator is able to keep track of the signal provided by the DDS through DAC and amplify it. As the frequency increases, the regulators limited bandwidth and slew rate does not allow amplification of the signal with the same gain and the output amplitude decreases. The higher the amplitude, the lower the cutoff frequency.

The same principle applies for the current mode measurement displayed in Figure 5.19 from frequencies 600 kHz and higher. The difference in this case is that at around 300 kHz the output amplitude begins to rise with increasing frequency. This is because of the small phase margin of the regulator when operating in current output mode.

As the frequency increases, the feedback phase shift approaches 180°, the regulator becomes more unstable, and the output begins to oscillate slightly.

The primary reason for this low phase margin is the current-to-voltage converting differential amplifier. Its gain is relatively high, so that the shunt resistor used for sensing output current can be low, which improves the device's efficiency and load regulation capability. The amplifier's high gain means that the amplifiers bandwidth is low. This causes delay and thus a phase shift in the feedback loop and the main regulator operates with outdated information about the current, resulting in the output overshooting.

Table 5.3: Cutoff frequencies at different output amplitudes in voltage mode

Upp [V]	f_{-3dB} [kHz]
30	588,9
10	772,7
5	1161,5
2	1745,9

Table 5.4: Cutoff frequencies at different output amplitudes in current mode

Ipp [mA]	f_{-3dB} [kHz]
1000	772,7
500	772,7
250	772,7
100	885,2

The cutoff frequencies shown in tables Table 5.3 and Table 5.4 were extracted from previous measurements by finding the amplitude value that is closest to a -3dB drop (70,7% of the starting amplitude). In the current mode, imperfect feedback compensation resulted in higher bandwidth but a less accurate amplitude.

5.5 Slew rate and rise/fall time

This measurement will determine how steep the transition from one voltage level to another is. A 100 kHz square wave is loaded into the generator and the time between 10% and 90% of the slope is taken, which represents rising and falling time. Slew rate is then calculated from the following formula:

$$SR = \left|\frac{U_{90\%} - U_{10\%}}{t_{90\%} - t_{10\%}}\right| = \left|\frac{U_{PP} \cdot (0.9 - 0.1)}{t_{90\%} - t_{10\%}}\right| = \left|\frac{0.8 \cdot U_{PP}}{\Delta t}\right| \quad (45)$$

Where SR is the slew rate in V/s, U_{PP} is the peak-to-peak voltage and Δt is the rising or falling time. The table below shows the results for both edge polarities:

Table 5.5: Slew rate and slope time results

Edge	rising	falling
Δt [ns]	753	835
SR [V/us]	31,55	28,71

Figure 5.20: 100kHz 30Vpp square wave used for slope measurement

The measurement was conducted on a 30 Vpp square wave shown in Figure 5.20: 100kHz 30Vpp square wave used for slope measurement to obtain the worst-case values of these parameters.

5.6 Noise spectrum

Because the analog circuitry is powered by a switching power supply, it is crucial to measure output spectrum. The noise spectrum was measured with AWG amplitude set to zero and output offset of 5 V. This way both power supplies will be operating.

Table 5.6: Highest peaks in output spectrum

N	1	2	3	4	5	6	7
f [kHz]	44,5	47,25	80	120	160	200	400
U [dBV]	-88,5	-87,5	-93,8	-93,5	-95,8	-93,5	-84,5

Table 5.6 shows values of the highest measured peaks. The values were obtained via oscilloscope FFT function. The frequency span is 1.25 MHz with resolution of 5 Hz.

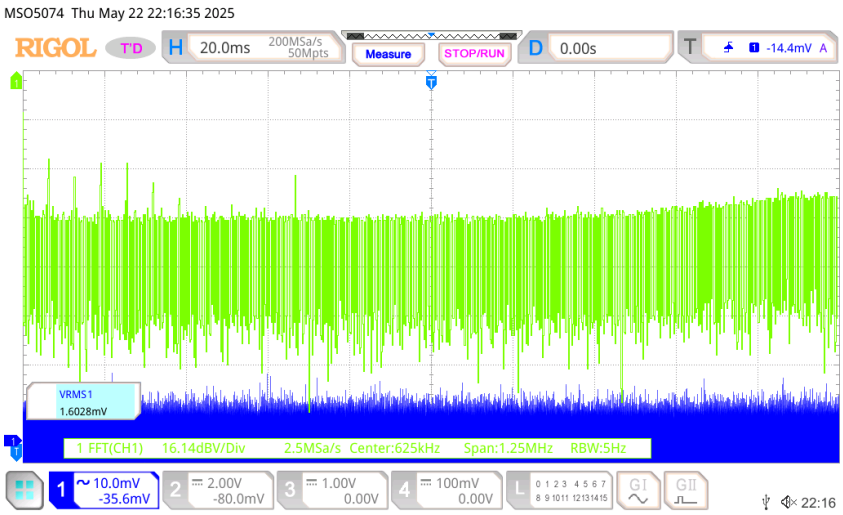

Figure 5.21: Output noise spectrum (green trace)

The noise floor is around -105dBV and is probably the oscilloscope's own noise. The spectral peaks are with the highest probability caused by the programmable isolated DC-DC converter, operating at 200kHz. Higher harmonics were filtered out by the power supply's LC filter.

CONCLUSION

In this bachelor thesis, an arbitrary waveform generator capable of both voltage and current output was successfully designed, implemented, and tested. The document provides a comprehensive analysis of various waveform generation methods, including their advantages and limitations, leading to the selection of the most suitable approach for this project.

A detailed block diagram of the entire device is included, along with the complete design and analysis of each functional block. For critical functional blocks, necessary calculations were performed to ensure their feasibility. The PCB design was carried out in EasyEDA design software, ensuring an efficient and practical layout of the components.

Thermal simulations were performed, which enabled the design of a heatsink, improving the device's performance under higher power loads. After the design was completed, all custom parts were manufactured by JLCPCB and assembled at the Brno University of Technology laboratories.

Finally, the complete device was put through real-life testing to confirm its performance under practical conditions. The measurement results proved that the device is capable of producing signals that meet the required specifications. Both voltage and current output modes were tested and their bandwidths measured. In voltage mode, the device can operate up to 1 MHz with the maximum output amplitude of 6 V. When tested at the maximum output amplitude of 15 V, the bandwidth decreased to 588 kHz. The DC output of the device was shown to be stable and sufficiently precise to allow the device to be used as a power supply.

Overall, the thesis demonstrated a successful implementation of theory into practical design, resulting in the creation of a versatile laboratory instrument.

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SYMBOLS AND ABBREVIATIONS

Abbreviations:

AC	Alternating Current
ASIC	Application specific integrated circuit
AGC	Automatic gain control
AWG	Arbitrary Waveform Generator
AFG	Arbitrary Function Gererator
BJT	Bipolar junction transistor
BUT	Brno University of Technology
DAC	Digital to analog converter
DC	Direct current
DCO	Digitally controlled oscillator
DDS	Direct digital synthesis
FEEC	Faculty of Electrical Engineering and Communications
FET	Field effect transistor
FPGA	Field programmable gate array
GND	Ground (0 V potential)
LUT	Lookup table
MCU	Microcontroller unit
MOSFET	Metal-oxide semiconductor field-effect transistor
NCO	Numerically controlled oscillator
OPAMP	Operational amplifier
PCB	Printed circuit board
PLL	Phase locked loop
DPLL	Digital phase locked loop
ADPLL	All-digital phase locked loop
RAM	Random access memory
ROM	Read-only memory
SCPI	Standard Commands for Programmable Instruments
SoC	System-on-Chip
VCC	Voltage of collector (positive supply voltage)
VEE	Voltage of emitter (negative supply voltage)
VCO	Voltage controlled oscillator
DCM	Digital clock management

Symbols:

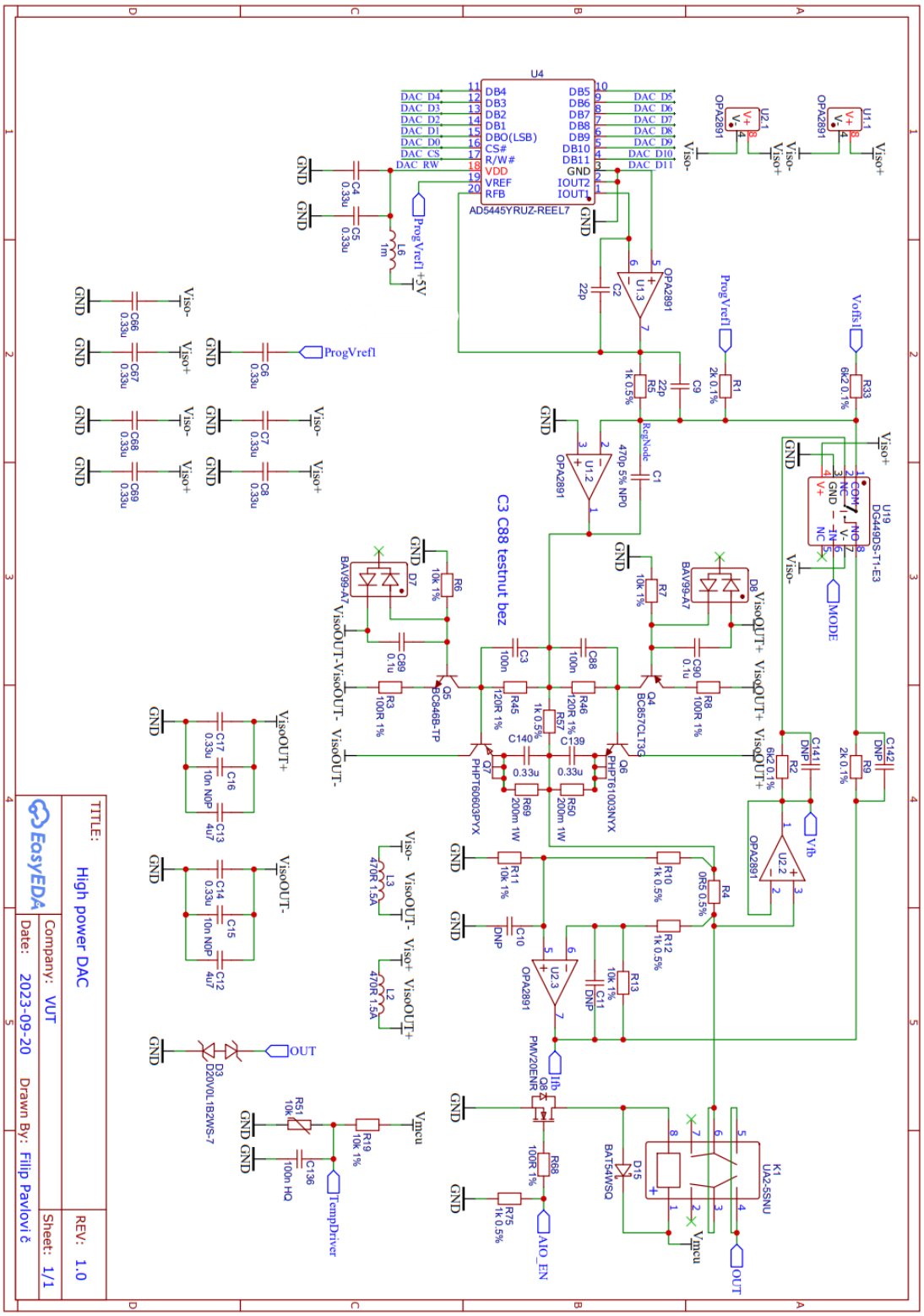
A	gain	(-)
f	frequency	(Hz)
I	current	(A)
I_{pp}	current peak-to-peak	(A)
R	resistance	(Ω)
U	voltage	(V)
U_{pp}	voltage peak-to-peak	(V)
β	bipolar junction transistor DC current gain	(-)

LIST OF APPENDICES

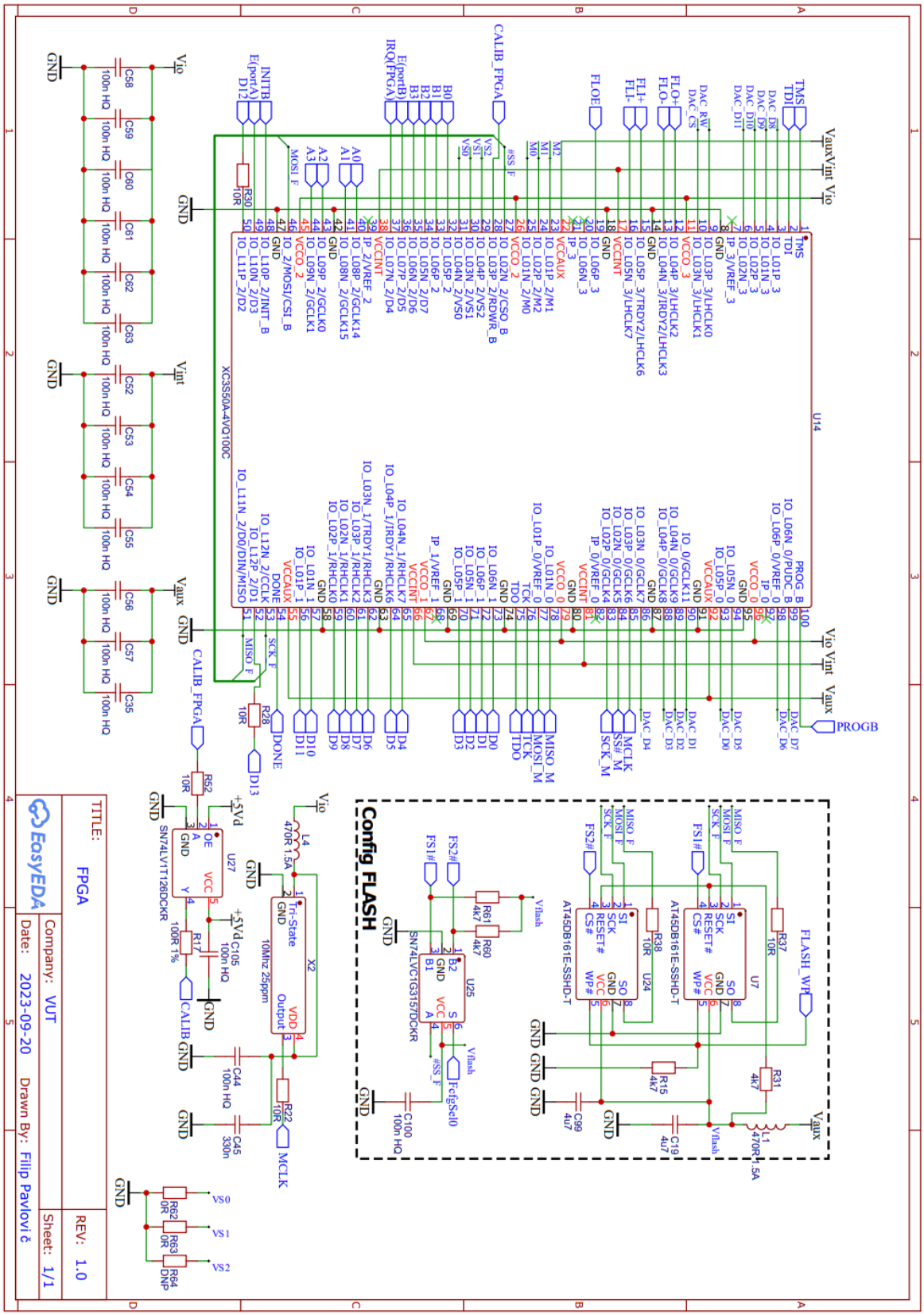
APPENDIX A - SCHEMATICS 90

Appendix A - Schematics

A.1 DAC with power amplifier



A.2 FPGA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U14
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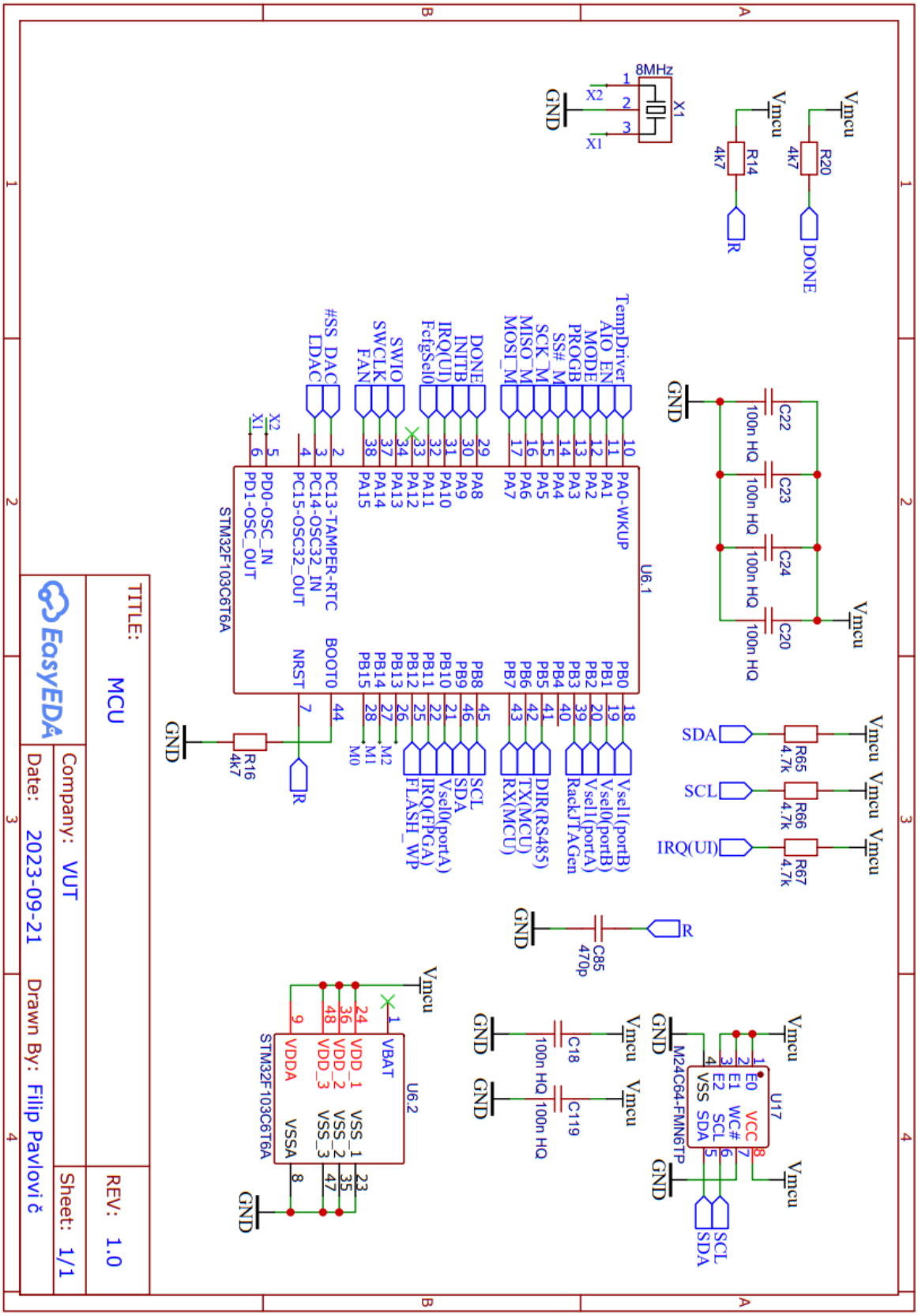
SN74LVT126DCKR
TITLE:
FPGA
REV: 1.0
Company: VUT
Sheet: 1/1
Date: 2023-09-20
Drawn By: Filip Pavlović
EasyEDA

A.3 MCU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MCU
REV: 1.0
Company: VUT
Date: 2023-09-21
Drawn By: Filip Pavlovič
Sheet: 1/1
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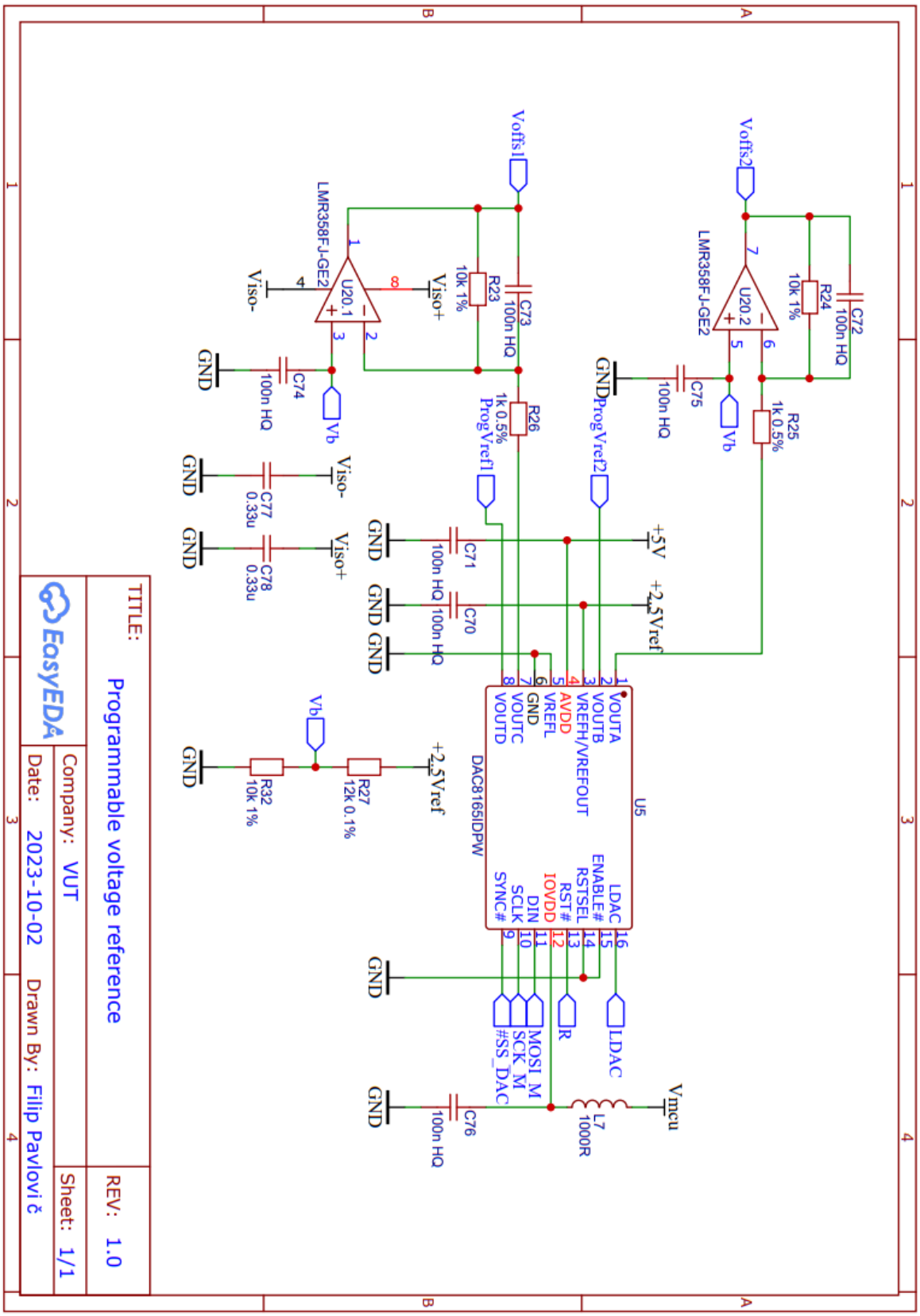
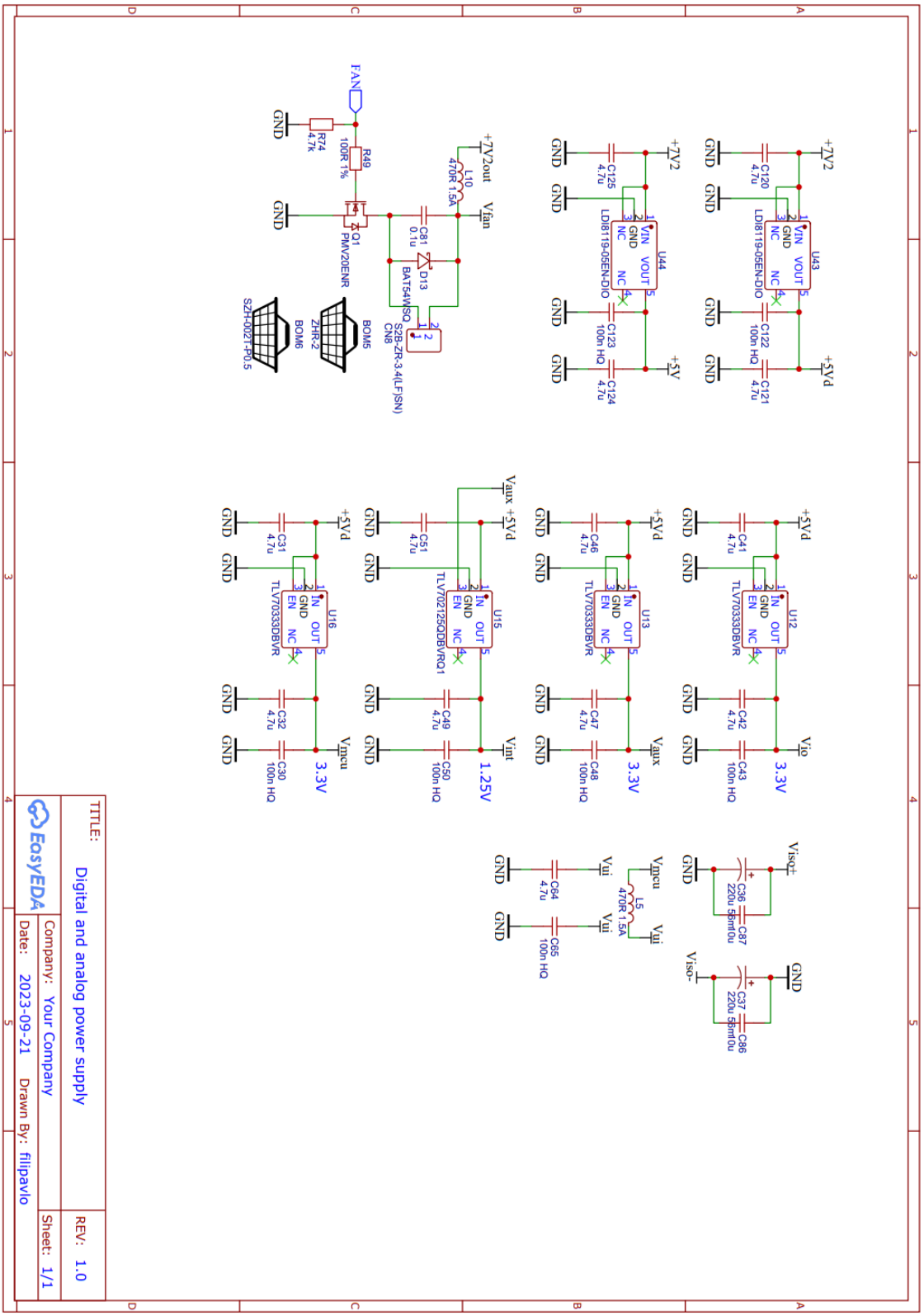
STM32F103C6T6A
U6.1
U6.2
8MHz
X1
X2
R20
4k7
R14
4k7
DONE
R
C22
C23
C24
C20
100n HQ
C85
470p
R16
4k7
R65
R66
R67
4.7k
SDA
SCL
IRQ(UI)
C18
C119
100n HQ
U17
M24C64-FMN6TP
TempDriver
AIO_EN
MODE
PROGB
SS#_M
SCK_M
MISO_M
MOSI_M
DONE
INITB
IRQ(UI)
FcfgSel0
SWIO
SWCLK
FAN
#SS_DAC
LDAC
Vsel1(portB)
Vsel0(portB)
Vsel1(portA)
RackJTAGen
DIR(RS485)
TX(MCU)
RX(MCU)
SCL
SDA
Vsel0(portA)
IRQ(FPGA)
FLASH_WP
M2
M1
M0
PA0-WKUP
PC13-TAMPER-RTC
PC14-OSC32_IN
PC15-OSC32_OUT
PD0-OSC_IN
PD1-OSC_OUT
NRST
BOOT0
VBAT
VDD_1
VDD_2
VDD_3
VSS_1
VSS_2
VSS_3
VDDA
VSSA
Vmcu
GND

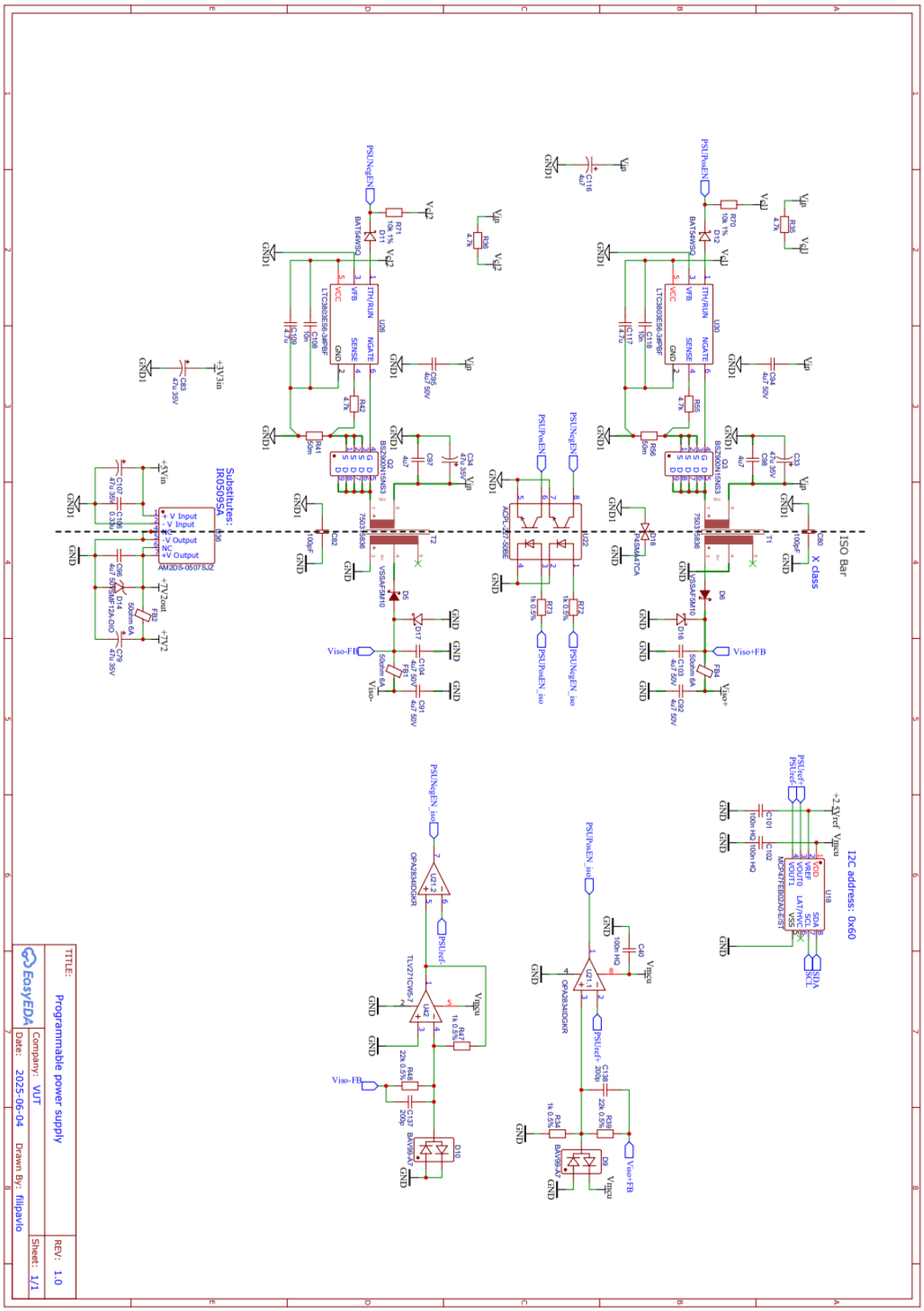
A.4 Programmable voltage reference



A.5 Digital and analog LDOs



A.6 Programmable isolated power supply



A.7 Data isolators and rack interface