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OTA-C Signal Delay Compensation Circuit for Transimpedance-Mode Audio Signal Processing Systems

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Abstract

This paper proposes an operational transconductance amplifier-capacitor-based (OTA-C) negative group delay (NGD) circuit for transimpedance-mode systems. The application areas extend from audio to sensor signal anticipation. Post-layout simulated NGD value of about 200 µs to 100 ns is observed to be achievable with three different capacitor values without any resistive passive components. The operation range varies from 700 Hz to 700 kHz. The NGD and the operation range are shown to be flexible without gain dependency. An example design is built for a specific NGD value of 15 µs and time-domain analysis is done with both a single-tone sinusoidal and a band-limited audio record in the range of 1 Hz–7 kHz. The calculated Root Mean Square Error for audio input to the system is only 4.70%.

1. Introduction

Real-time audio signal processing, sensor fusion, or speech processing data collecting is limited because of the signal delays, often caused by electrical signal transmission across a cable or network delays [1]. Depending on the system type and the solution to the problem, the issue might be classified as follows. First of all, by reducing the time delays of the system, a single sensor data monitoring system can be improved to be fairly close to a real-time application. Secondly, multiple sensor data monitoring systems can be improved by controlling the time delay differences of the different sensor outputs. For instance, if there are time-delay differences between several sensor data because of the physical obstacles of the signal paths, with different and fixed negative group delay (NGD) values, the sensor signal delays can be equalized. Data acquisition using statistical prediction methods or syncing the leading sensor outputs to the lagging sensor outputs are among the solutions to the second problem. However, the first technique highly depends on the statistical data parameters and may require high computing power. In addition, the second technique reduces the overall system's time delay to the system's poorest sensor output, which has the worst time delay. Using a transfer function with NGD is a promising solution for such delays. Therefore, an approach for such a time delay problem is to use the NGD structure to adjust the lagging sensor outputs to the leading sensor output. Suppose the system's operation frequency response matches the NGD structure's operation frequency range. In that case, this solution is valid and convenient for short-term prediction when the system model and parameters are unavailable [2]. Industrial sensors have not only static but also dynamic characteristics. Therefore, physical quantities, such as temperature, displacement, pressure, and others, cannot be converted to voltage or current instantaneously, but time is required for this conversion. Therefore, a certain amount of delay cannot be avoided. However, in many applications like sensor data acquisition in real-time, this delay is a challenge, as mentioned.

An interesting electronic circuit-based NGD system is introduced in [3]. There are several NGD studies with passive RC, RLC network [1, 4]; with operational amplifier (OA)-based active RC and RLC filters [3, 5, 6, 7, 8] or with Taylor type prediction using the mathematical model of NGD based circuit [2, 9]. A brief collection of proposed topologies in the literature is seen in Table 1. Voltages are used as input to the NGD structure in prior studies. Many industrial sensors have current outputs [10, 11]. In this paper, we present an operational transconductance amplifier (OTA)-based NGD circuit which accepts the current signal as its input and with its NGD property in a specific frequency operation range, it can be used for signal delay compensation for the current output systems without a current-voltage conversion needed. In this way, the time-delayed signal from the sensor can be made time advanced; in other words, the delay between the actual physical phenomenon and the input signal of the system can be reduced. Thus, for the first type of system time delay issue, it improves the system time domain response without relying on the statistical data parameters.

This study presents a transimpedance-mode (TIM – current-input-voltage-output) OTA-C-based NGD circuit without a resistive passive component, which may be useful for mixed-mode sensors. The metal-oxide-semiconductor field-effect transistors (MOSFETs) are used as resistive components in this, allowing an active NGD circuit implementation with lower power consumption and physical area. In the article, a single NGD value is determined to be selected and tested, which may be a solution for a single input delay problem.

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Table 1
A brief comparison of NGD circuit topology functions in the literature.

Reference	Circuit Topology	Transfer Function
[1, 12]	Passive RC Filter	$\frac{b_1 s + b_0}{b_1 s + a_0 + b_0}$
[2]	BJT Based Delay Summation	$a_0 + a_1.e^{(-st_d)} + a_2.e^{(-2st_d)}$
[3, 5, 6]	OA Based Differentiator	$b_1 s + b_0$
[4]	Passive RLC Network	$\frac{(a_1 b_0 + 1) b_1 s + a_1}{b_1 a_1 s}$
[7, 8]	OA Based Active RLC Filter	$\frac{b_2 s^2 + b_1 s + b_0}{a_2 s^2 + b_1 s + b_0}$
[9]	OA Based Active RC Filter	$\frac{b_1 s + b_0}{a_1 s + a_0}$
[13]	Cascaded CFOA Based Active Filter	$\frac{b_2 s^2 + b_1 s + b_0}{a_1 s + a_0}$
[14]	Function Based	$\frac{b_2 s^2 + b_1 s + b_0}{a_2 s^2 + a_1 s + a_0}$
This work	OTA-C Based NGD Circuit	$\frac{b_1 s + b_0}{b_1 s + a_0}$

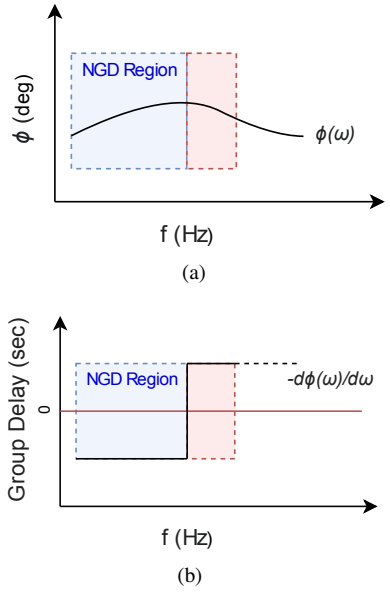

Figure 1: (a) A phase response example of a basic stable NGD circuit and (b) its group delay.

The article is arranged as follows: Section 2 introduces general NGD mathematical models. Sections 3 and 4 illustrate the design of a first-order OTA-based NGD circuit and its analysis. Simulation results are presented in Section 5. Finally, Section 6 concludes the study and discusses future work.

2. General Mathematical Models

In a linear time-invariant (LTI) system, with the input $x(t)$ and the output $y(t)$, the transfer function of the system is given as:

$$H(j\omega) = Y(j\omega)/X(j\omega), \tag{1}$$

where $Y(j\omega)$ and $X(j\omega)$ are the output and the input signal's Laplace transforms, with $(s \rightarrow j\omega)$, respectively. For the given system transfer function, the phase shift is defined as:

$$\phi = \arg(H(j\omega)) = \arg(Y) - \arg(X), \tag{2}$$

while the group delay is defined as:

$$\tau_g(\omega) = -\frac{d\phi(\omega)}{d\omega}, \tag{3}$$

where $\tau_g(\omega)$ denotes the group delay response of the system with respect to angular frequency, as depicted in Figure 1.

The phase and group delay properties can directly be derived from a circuit's transfer function. In this section, the first and second-order transfer functions are investigated in terms of group delay, showing how the transfer function's coefficients affect it.

2.1. Description of First-Order NGDs

The general first-order transfer function $H_1(s)$ is given as:

$$\begin{aligned} H_1(s) &= \frac{b_0 + b_1 s}{a_0 + a_1 s} \\ &= \frac{b_0}{a_0} \frac{1 + \frac{b_1 s}{b_0}}{1 + \frac{a_1 s}{a_0}} \\ &= \frac{b_0}{a_0} \frac{1 + \tau_z s}{1 + \tau_p s} \\ &= K \frac{1 + \tau_z s}{1 + \tau_p s} \end{aligned} \tag{4}$$

where $\tau_z = b_1/b_0$, $\tau_p = a_1/a_0$ are respectively zero and pole time constants and $K = b_0/a_0$. Here K is the gain of the circuit, and a_i, b_i are positive real numbers. Obviously, there are two parameters affecting the phase and one additional parameter defining the gain.

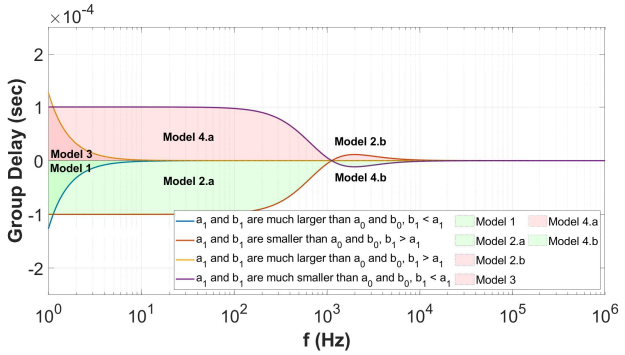

Figure 2: Regions illustrating the group delays for a different selection of parameters, $a_0 = b_0$.

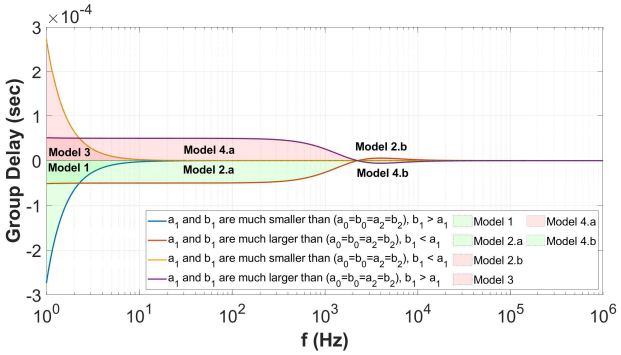

Figure 3: Regions illustrating the group delays for the second-order transfer function, $a_0 = b_0 = a_2 = b_2$.

For the first-order transfer functions, using (3), the group delay is expressed as:

$$\tau_{g1} = -\frac{d \arctan\left(\frac{b_1\omega}{b_0}\right)}{d\omega} + \frac{d \arctan\left(\frac{a_1\omega}{a_0}\right)}{d\omega}. \quad (5)$$

Rearranging (5) gives the group delay in the form:

$$\tau_{g1} = -\frac{b_1 b_0}{b_1^2\omega^2 + b_0^2} + \frac{a_1 a_0}{a_1^2\omega^2 + a_0^2}. \quad (6)$$

In Figure 1(b), the blue region corresponds to a phase response increment of the system, which results in an NGD, while the marked red region corresponds to the positive group delay of the example system.

In (6), there are four possibilities for four parameters a_0, a_1, b_0 and b_1, when the parameters a_0 and b_0 are selected equal:

- $a_1 > b_1$ and a_1 and b_1 are much larger (1000 times) than $a_0 = b_0$
- $a_1 < b_1$ and a_1 and b_1 are much smaller (1/1000 times) than $a_0 = b_0$
- $a_1 > b_1$ and a_1 and b_1 are much smaller (1/1000 times) than $a_0 = b_0$
- $a_1 < b_1$ and a_1 and b_1 are much larger (1000 times) than $a_0 = b_0$

Thus, the four possible parameter choice provides six group delay models. Note that four correspond to a proper NGD operation, as shown in Figure 2.

In Figure 2, the frequency and corresponding group delay values are shown depending on a_n and b_n coefficients. An actual circuit can be designed by properly selecting passive component values, resulting in the desired a_n and b_n values. In this section, they are selected to visualize the Models for the NGD.

2.1.1. Detailed Description of Model 1 NGD Operation

The Model 1 NGD structure, seen in Figure 2, is obtained by selecting $a_1 > b_1$ when a_1 and b_1 are substantially greater than $a_0 = b_0$. The downside of that concept is that the group delay varies significantly with frequency. As a result, there may be undesirable distortion in the output. The same operation is achieved when the a_1 and b_1 coefficients are selected equal and $b_0 > a_0$ and both b_0 and a_0 are much smaller than $a_1 = b_1$. Because of that, the symmetrical parameter selection is not included in the Figure.

2.1.2. Detailed Description of Model 2 NGD Operation

The Model 2 NGD structure, seen again in Figure 2, is obtained by selecting $a_1 < b_1$ when a_1 and b_1 are substantially smaller than $a_0 = b_0$. In contrast to Model 1, Model 2 achieves a flat NGD until a frequency value is reached. In Figure 2, Model 2.b shows how the group delay varies from negative to positive at a particular frequency setting. Furthermore, with Model 4.b, an NGD can be achieved in a frequency operation range. However, similar to Model 1, the group delay value varies with frequency. The same operation is achieved when the a_1 and b_1 are selected equal, and $a_0 > b_0$ and both b_0 and a_0 are much larger than $a_1 = b_1$. Because of that, the symmetrical parameter selection is not included in the Figure. In general, Model 4.b is used for high-frequency NGD applications, as reported in [4, 15, 16, 17] while Model 1 corresponds to [1]. The value, adaptability, and frequency range applicability to the input signal and system amplification are all essential NGD circuit design features. In that manner, in this study, Model 2 is used for the NGD operation with constant gain in the NGD operation range. Studies [2, 3, 12, 13, 18, 19, 20] also implement Model 2.

2.2. Description of Second-Order NGDs

Similarly to Section 2.1, the second-order transfer function can also be investigated. The general second-order transfer function $H_2(s)$ is given as:

$$H_2(s) = \frac{b_0 + b_1 s + b_2 s^2}{a_0 + a_1 s + a_2 s^2}. \quad (7)$$

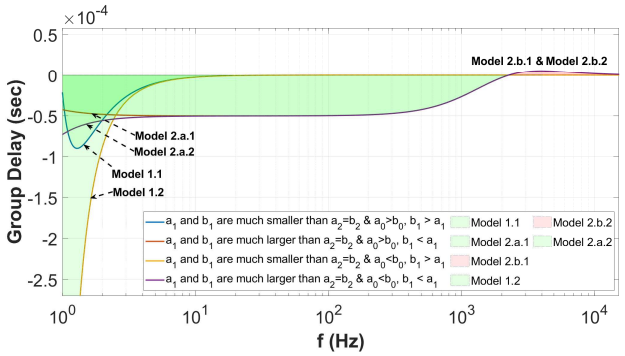

Figure 4: Regions illustrating the NGD for the second-order transfer function for different a_0 and b_0 values, while $a_2 = b_2$.

For the second-order transfer functions, using (3) gives the group delay as:

$$\tau_{g2} = -\frac{d\arctan\left(\dfrac{b_1\omega}{b_0 - b_2\omega^2}\right)}{d\omega} + \frac{d\arctan\left(\dfrac{a_1\omega}{a_0 - a_2\omega^2}\right)}{d\omega}. \tag{8}$$

Rearranging (8), the group delay can be written as:

$$\tau_{g2} = -\frac{b_1\left(b_0 + b_2\omega^2\right)}{b_1^2\omega^2 + \left(b_0 - b_2\omega^2\right)^2} + \frac{a_1\left(a_0 + a_2\omega^2\right)}{a_1^2\omega^2 + \left(a_0 - a_2\omega^2\right)^2}. \tag{9}$$

First, selecting $a_2 = b_2 = a_0 = b_0$, there are four possibilities for selecting a_1 and b_1, which results in the same group delay models with the first-order transfer function group delay models, shown in Figure 3.

In Figure 3, with the following parameter selections, similar NGD regions with the first-order transfer function are possible:

- $b_1 > a_1$ and a_1 and b_1 are much smaller (1/1000 times) than $a_0 = b_0 = a_2 = b_2$
- $a_1 > b_1$ and a_1 and b_1 are much larger (1000 times) than $a_0 = b_0 = a_2 = b_2$
- $a_1 > b_1$ and a_1 and b_1 are much smaller (1/1000 times) than $a_0 = b_0 = a_2 = b_2$
- $b_1 > a_1$ and a_1 and b_1 are much larger (1000 times) than $a_0 = b_0 = a_2 = b_2$

Moreover, for the NGD models achieved from these possibilities, to see the effect of the parameters a_0 and b_0 on NGD Models 1 and 2, a_2 and b_2 kept equal and 2 NGD models are categorized as follows:

- $a_0 > b_0$ and a_1 & b_1 are much smaller (1/1000 times) than $a_2 = b_2$, $b_1 > a_1$
- $a_0 > b_0$ and a_1 & b_1 are much larger (1000 times) than $a_2 = b_2$, $b_1 < a_1$
- $b_0 > a_0$ and a_1 & b_1 are much smaller (1/1000 times) than $a_2 = b_2$, $b_1 > a_1$
- $b_0 > a_0$ and a_1 & b_1 are much larger (1000 times) than $a_2 = b_2$, $b_1 < a_1$

Figure 4 illustrates that different selection of the parameters a_0 and b_0 changes the original NGD Model 1 and Model 2.a at low frequencies. As mentioned previously, in the first-order NGD models, in Model 1, the group delay is negative. However, it varies significantly with frequency. In the second-order transfer function Model 2.a.1 and Model 2.a.2, although NGD varies with frequency, that effect is small compared to the first model.

3. Circuit Description

In this section, we present the design of a first-order OTA-based NGD circuit as an application in light of the above-presented theory. The OTA symbol is depicted in Figure 5 and its operation is given in (10):

$$i_o = g_\mathrm{m}\left(V_a - V_b\right), \tag{10}$$

where i_o is the output current of the OTA, V_a and V_b are the voltages at the input terminals, while g_m is the transconductance of the OTA.

The circuit schematic of the proposed NGD circuit is shown in Figure 6, while its transfer function is given by (11):

$$H(s) = \frac{V_\mathrm{o}}{I_\mathrm{in}} = \frac{1}{g_{\mathrm{m}2}}\frac{g_{\mathrm{m}2} + sC}{g_{\mathrm{m}1} + sC}. \tag{11}$$

Note that the pole, zero frequencies, and the gain can be adjusted independently by fine-tuning $g_{\mathrm{m}1}$ and/or $g_{\mathrm{m}2}$ values, which allows selecting a wide range of the NGD value of the circuit and permits easy design. Keep in mind that the g_m values are chosen in advance of the circuit's construction. The phase and the group delay responses of the circuit are given in (12) and (13), respectively.

$$\begin{aligned}\phi(\omega) &= \arctan\left\{\frac{\Im[Y(j\omega)]}{\Re[Y(j\omega)]}\right\} - \arctan\left\{\frac{\Im[X(j\omega)]}{\Re[X(j\omega)]}\right\} \\ &\cong \frac{\omega C}{g_{\mathrm{m}2}} - \frac{\omega C}{g_{\mathrm{m}1}},\end{aligned} \tag{12}$$

$$\tau_g(\omega) = -\frac{d\phi(\omega)}{d\omega} = C\left(\frac{1}{g_{\mathrm{m}1}} - \frac{1}{g_{\mathrm{m}2}}\right). \tag{13}$$

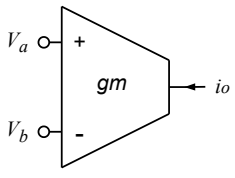

Figure 5: The OTA symbol.

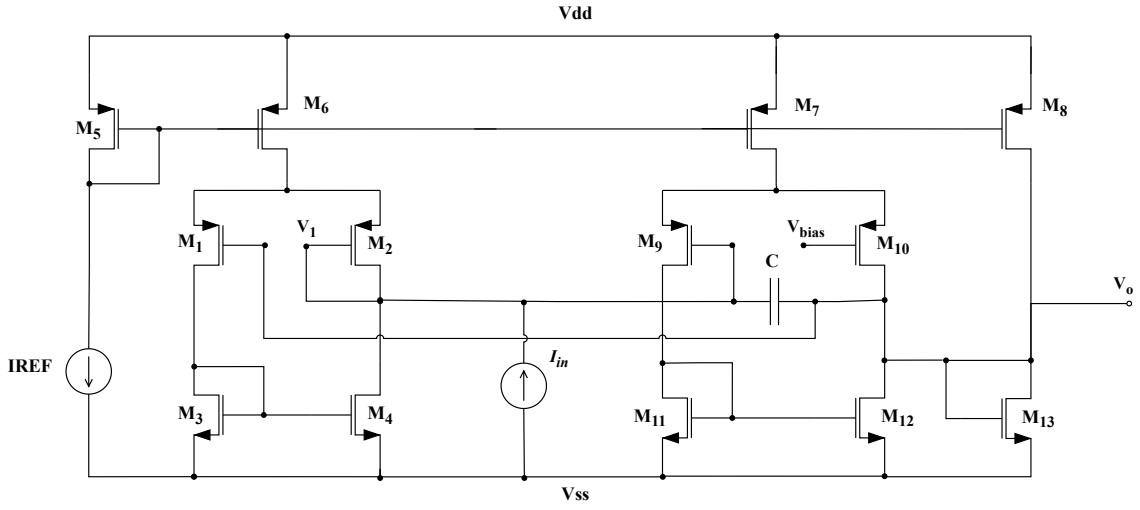

Figure 8: CMOS implementation of the OTA-C-based NGD

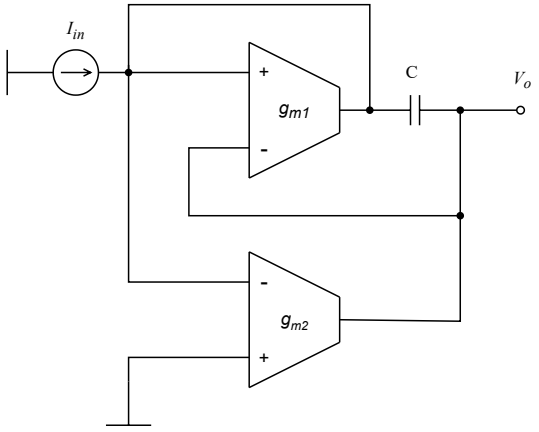

Figure 6: Proposed OTA-C NGD circuit.

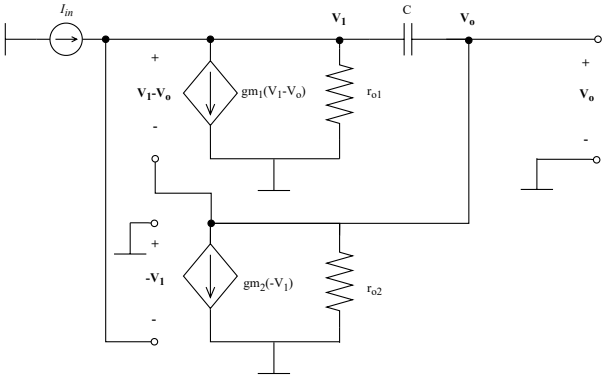

Figure 7: The equivalent small-signal model of the OTA-C NGD circuit.

These formulas are valid for sufficiently low frequencies. Equation (13) indicates that if the transconductance values are positive, condition (14) is satisfied, and NGD can be achieved with:

$$g_{\mathrm{m1}} > g_{\mathrm{m2}}. \tag{14}$$

The gain of the system in the low- and high-frequency regions are given in (15) and (16), respectively, as follows:

$$\mathrm{H}_{\omega\to 0} = \frac{1}{g_{\mathrm{m1}}}, \tag{15}$$

$$\mathrm{H}_{\omega\to \infty} = \frac{1}{g_{\mathrm{m2}}}. \tag{16}$$

The equations (15) and (16) show that amplification is possible, maintaining the NGD operation of the circuit. Moreover, changing g_{m2} without changing g_{m1} provides group delay adjustment without changing the gain in the low-frequency region.

The operation of the circuit can be summarized as follows:

- Adjustment of C alters both NGD operation range and NGD value,
- Adjustment of g_{m2} changes NGD value only.

The constant gain in the NGD area ensures that designing an NGD circuit is simple and adjustable. In terms of group delay, the circuit's output differs from the input signal, but not in terms of amplification or attenuation. As a result, without making dramatic changes to the design, the same circuit can be utilized for different required NGD values for the sensor outputs in the same system. For further studies g_{m} values can be controlled to change the NGD value during the operation.

4. Design Example and Analysis

The small-signal model of the proposed OTA-C NGD circuit is given in Figure 7, where the input and the parasitic capacitance of OTAs are ignored since their values are expected to be small [21, 22].

The CMOS realization of the circuit, depicted in Figure 8, is composed of 13 transistors and a single capacitor. The OTA_1 and the OTA_2 be formed by the transistors $M_{1-4,6}$ and $M_{7,9-12}$, respectively. The aspect ratios of the OTA_2 transistors with respect to the OTA_1 transistors are given in (17):

$$\frac{W_{\mathrm{OTA}_2}}{L_{\mathrm{OTA}_2}} = \alpha \frac{W_{\mathrm{OTA}_1}}{L_{\mathrm{OTA}_1}}. \tag{17}$$

The overdrive voltages (V_{ov}) of the transistors are selected to be in the range of 0.2 to 0.3 V, while the g_{m} values of the transistors are calculated using (18) [22]:

$$g_{\mathrm{m}} = \sqrt{2\mu_{\mathrm{n,p}} C_{\mathrm{ox}} \frac{W}{L} I_{\mathrm{D}}}. \tag{18}$$

To keep the OTA_1 block transistors V_{ov} values about 0.2 V range, the transistor sizes are selected as in considering the current equation of the MOSFET in the saturation region in (19):

$$I_{\mathrm{D}} = \frac{1}{2}\mu C_{\mathrm{ox}} \frac{W}{L} \left(V_{\mathrm{ov}}\right)^2. \tag{19}$$

If the mismatches of the transistor sizes are neglectable, the transconductance values of the OTAs are equal to the transconductances of the transistors M_1 and M_9, respectively.

Equations (17)–(19) indicate that the second block's transconductance is dependent to α in the form of (20):

$$g_{\mathrm{m9}} = \alpha g_{\mathrm{m1}}, \tag{20}$$

where α in (17) is a positive number smaller than 1. In this design, I_{REF} is selected as 100 µA. Therefore, to achieve a 10 µA current flowing to the OTA_2, the α is limited to be at least 0.1. Using (18), (20), and parameters in Table 2, the transconductance of OTA_1 and OTA_2 results as 453 µA/V and α 453 µA/V, respectively.

The gate-to-drain (C_{gd}) and gate-to-source (C_{gs}) capacitors of the OTA_1 stage are given by (21), the technology values of the gate to drain capacitances are $7.9{\cdot}10^{-10}$ F/m and $6.34{\cdot}10^{-10}$ F/m for the n-type and p-type transistors, respectively:

$$\begin{aligned} C_{\mathrm{gs2}} &= C_{\mathrm{gs0_p}}{\cdot}W_2, \\ C_{\mathrm{gd4}} &= C_{\mathrm{gd0_n}}{\cdot}W_4, \\ C_{\mathrm{o1}} &= C_{\mathrm{gd2}} + C_{\mathrm{gd4}}{\cdot} \end{aligned} \tag{21}$$

The total output capacitances of the first and second OTAs are given by (22), respectively:

$$\begin{aligned} C_{\mathrm{o1}} &\cong 9.13\ \mathrm{fF} + 2.84\ \mathrm{fF} = 11.97\ \mathrm{fF}, \\ C_{\mathrm{o2}} &= \alpha{\cdot}(9.13\ \mathrm{fF} + 2.84\ \mathrm{fF}) = \alpha{\cdot}11.97\ \mathrm{fF}. \end{aligned} \tag{22}$$

Table 2
Parameters of the transistors in OTA-C NGD.

Reference	Value
V_{DD}	1.8 V
V_{SS}	0 V
I_{REF}	100 µA
V_{bias}	0.6 V
V_{THON}	0.371 V
V_{THOP}	−0.395 V
μ_{n}	276.47 cm^2/Vs
μ_{p}	118.02 cm^2/Vs
T_{ox}	$4.1{\cdot}10^{-9}$
$W_{1,2}$	14.4 µm
$W_{3,4}$	3.6 µm
$W_{5,6}$	28.8 µm
$W_{9,10}$	$\alpha{\cdot}$14.4 µm
$W_{11,12}$	$\alpha{\cdot}$3.6 µm
$W_{7,8}$	$\alpha{\cdot}$28.8 µm
W_{13}	$\alpha{\cdot}$7.2 µm
L_{1-13}	0.36 µm

The output resistance of the first block is given by (23):

$$R_{o1} = r_{o2} \parallel r_{o4}, \tag{23}$$

Hence, the transfer function (11) turns to (24) as follows:

$$H(s) = \frac{V_{\mathrm{o}}}{I_{\mathrm{in}}} = \frac{1}{g_{\mathrm{m9}}} \frac{g_{\mathrm{m9}} + sC}{g_{\mathrm{m1}} + sC} \frac{1}{1 + sR_{o1}C_{o1}}. \tag{24}$$

Here, the last term introduces a higher frequency pole to the system, which is further investigated in the next section.

5. Simulation Results

Taking into account (20) and rearranging (13), the group delay is given by (25):

$$\tau_g(\omega) = \frac{C}{g_{\mathrm{m1}}} \frac{\alpha - 1}{\alpha}. \tag{25}$$

For three capacitor values $C = \{0.1, 1, 10\}$ nF, the calculated group delay values with expected g_{m} and constants α are compared with the SPICE simulations, as shown in Figure 9. The three clusters in the Figure represent the different capacitor values. The x-axis is the transistor sizing factor value. Note that in Figure 9, calculated group delay and simulation values are well-correlated in the range of $\alpha = 0.1$ to 0.8 values. To test the circuit with $C = 1$ nF, $\alpha = 0.125$, and using the parameter in Table 2, the group delay is calculated to be −15.50 µs. The dominant zero of the system determines the group delay change of the system, as indicated in (26):

$$f_{\mathrm{NGD}_{cross}} = \frac{g_{\mathrm{m9}}}{2\pi C} = 8.95\ \mathrm{kHz}. \tag{26}$$

On the other hand, the dominant pole of the system determines the 3 dB gain drop of the system, as indicated

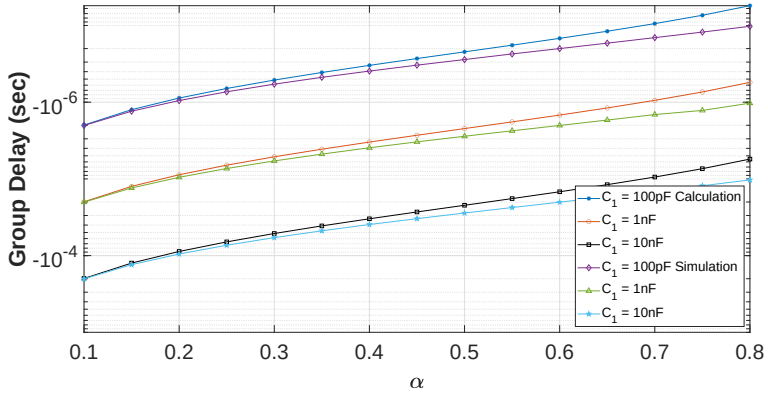

Figure 9: Simulation of α vs. group delay for $C = \{0.1, 1, 10\}$ nF.

in (27), while the gain value beyond this frequency is given by (16):

$$f_{-3\,\mathrm{dB}} = \frac{g_{\mathrm{m1}}}{2\pi C} = 71.6\ \mathrm{kHz}. \tag{27}$$

Note that the output resistance of the OTA_1 is approximately 75 kΩ. Assuming the capacitance of the OTA_1 given in (22), the high-frequency pole of the NGD circuit can be calculated as (28), without load:

$$f_{-3\mathrm{dB}_{hf}} = \frac{1}{2\pi C_{\mathrm{o1}} \times 75 \cdot 10^3} = 178\ \mathrm{MHz}. \tag{28}$$

With a capacitive load seen in the next stage, a high-frequency pole can be calculated with total capacitances $C'_{o1} = C_{o1} + C_{load}$. The next stage capacitance should satisfy the condition $f_{-3\mathrm{dB}_{hf}} > f_{\mathrm{NGD}_{cross}}$ not to change the NGD value and the operation range.

The proposed NGD circuit was simulated in SPICE software using the calculated circuit parameters and TSMC 180nm CMOS process. The simulated magnitude, phase, and group delay-frequency responses are shown in Figure 10.

The time-domain analysis is done with a single tone current input @1 kHz and 1 ms delay. At the end of the cycles, a small oscillation may occur at the output, [6, 23]. In order to demonstrate that this effect does not exist in this design, the signal applied to the system is opened 1 ms after the simulation started, as depicted in Figure 11. Note that a DC offset of 730 mV exists at the output due to a non-symmetrical supply.

To examine the circuit under more realistic conditions, an example audio record is inserted into the system as an input; see the time-domain responses in Figure 12. The audio record is band-limited @7 kHz, to be within the negative group delay operation range. The time-advanced signal obtained from the output terminal of the NGD circuit is not an exact replica of the input. Therefore, to investigate the signal error, a similar method is used as in studies [19] and [20]. The input signal is reconstructed by adding a delay equal to the magnitude of the NGD value to calculate the error in the NGD circuit output, as depicted in Figure 13.

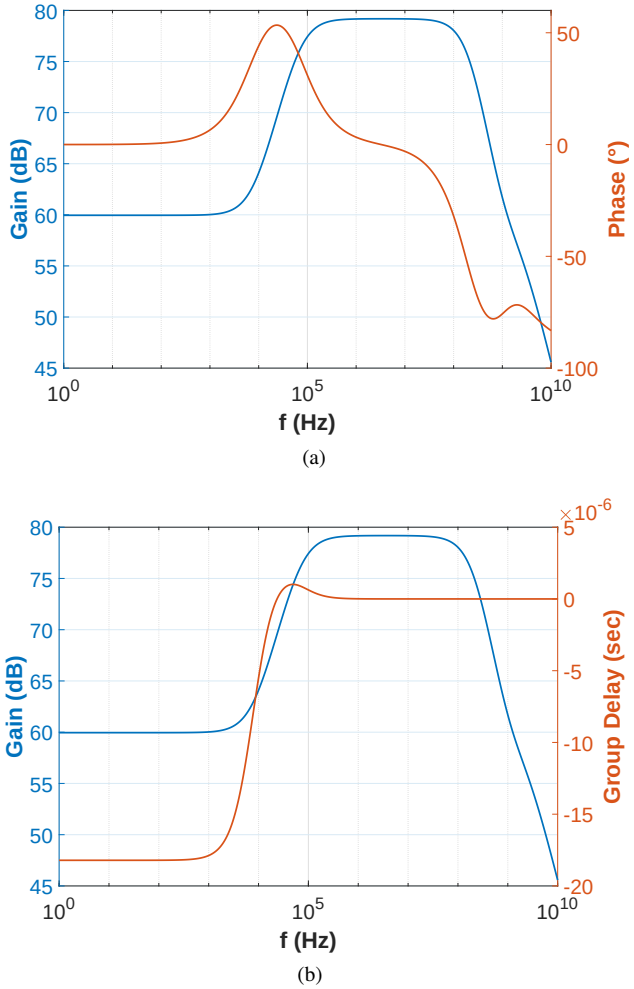

Figure 10: AC analysis: (a) magnitude and phase response, (b) magnitude and group delay response for $C = 1$ nF and $\alpha = 0.125$.

Root Mean Square Error (RMSE) is calculated as in the

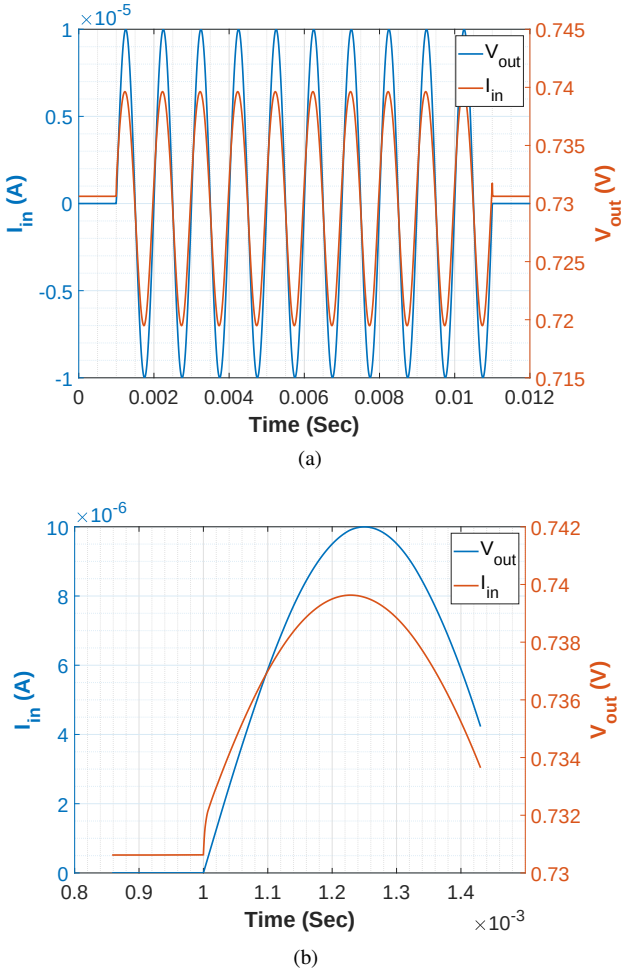

Figure 11: Time domain analysis at $f = 1$ kHz: (a) 12ms simulation, (b) zoom.

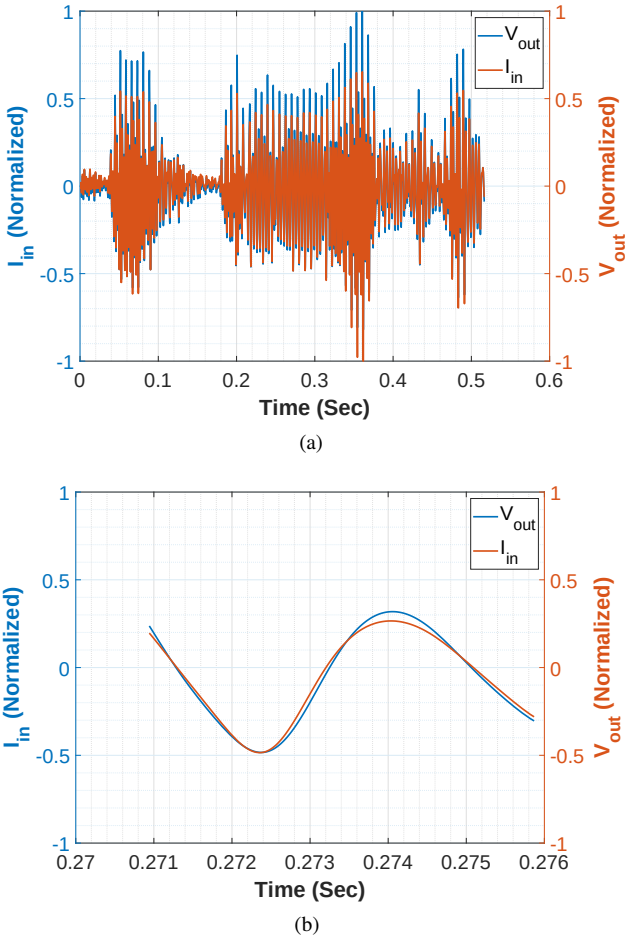

Figure 12: Time domain analysis: (a) Input audio signal and corresponding output, (b) zoom.

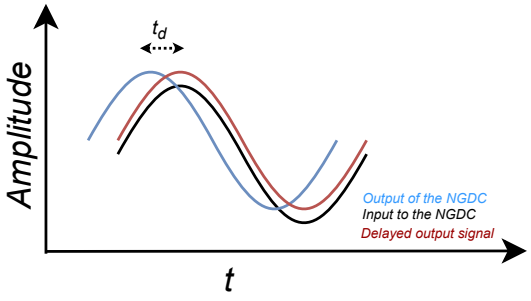

Figure 13: The outputs of NGD circuit with reconstructed input signal.

equation (29):

$$\mathrm{RMSE} = \sqrt{\frac{1}{b-a}\sum_{i=a}^{b}\left(x_{in}[i] - x_{out}[i + \tau_{ngd}/T_{sample}]\right)^2}, \tag{29}$$

where $x_{in}[i]$ and $x_{out}[i + \tau_{ngd}/T_{sample}]$ are the normalized input to NGD circuit and the normalized delayed output of the NGD circuit, respectively, while a and b denote the start and the end indexes of the sampled signals. Here, the aim is to eliminate the time delay advance at the output to give a numerical result of how well the output and the input signals match with each other. Using MATLAB software, the input and the output signals of the NGD circuit are sampled with $T_{sample} < |\tau_{ngd}|$, where i denotes the index of the sampled input and output. Note that τ_{ngd}/T_{sample} is selected as an integer, and τ_{ngd} has a negative group delay value. Using (29), the calculated RMSE for the normalized audio signal is 4.70%.

The layout of the NGD circuit in open-source Magic VLSI Layout Tool software with the dimension of 14.94 µm × 27 µm is given in Figure 14. For the design α is selected as 0.125. The transistor dimensions are given in Table 3. Electrical characteristics of OTAs are listed in Table 4. The frequency and time-domain post-layout simulation results are depicted in 15 and 16, respectively, while the comparison is given in Table 5.

The NGD value and the operation frequency limit circuit are inversely proportional. As a result, the Figure of Merit (FoM) is calculated by applying the formula $\mathrm{FoM} = f_{zerocross} \times \tau_g(\omega)$ [12]. The product of the NGD circuit frequency operation range and the NGD value must

Table 3
The transistor aspect ratios.

Transistors	W	L	W/L Ratio
$M_{1,2}$	14.4 µm	0.36 µm	40
$M_{3,4}$	3.6 µm	0.36 µm	10
$M_{5,6}$	28.8 µm	0.36 µm	80
$M_{9,10}$	1.80 µm	0.36 µm	5
$M_{11,12}$	0.36 µm	0.36 µm	1
$M_{7,8}$	3.60 µm	0.36 µm	10
M_{13}	0.72 µm	0.36 µm	2

Table 4
Electrical characteristics of OTAs

Parameters	OTA_1	OTA_2
Gain (dBS)	–91.54	–91.54
f_{-3dB} (GHz)	3.05	3.05
CMRR (dB)	37	37
Power dissipation (mW)	0.475	0.319

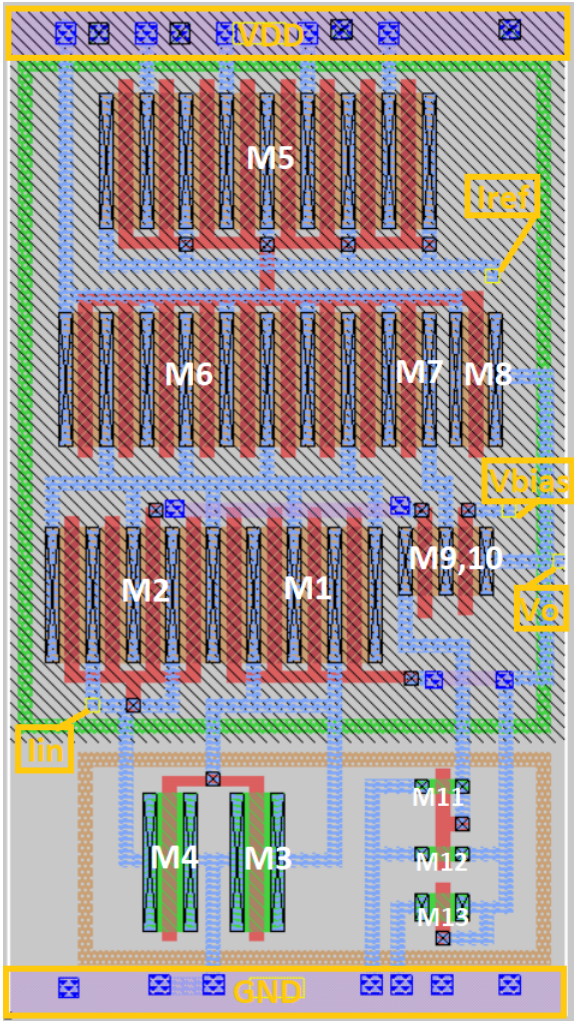

Figure 14: The layout of the designed NGD with the dimension of 14.94 µm × 27 µm.

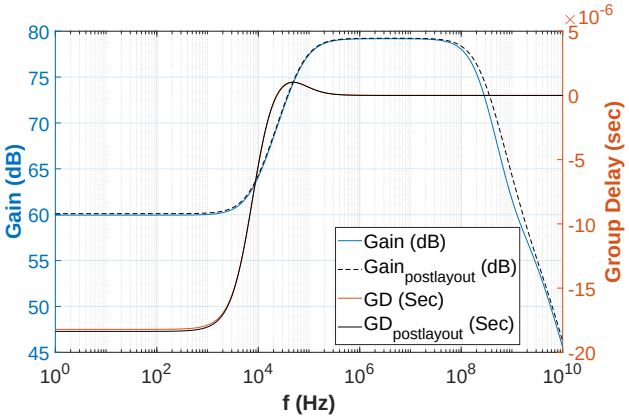

Figure 15: Simulated pre- and post-layout magnitude and group delay-frequency responses.

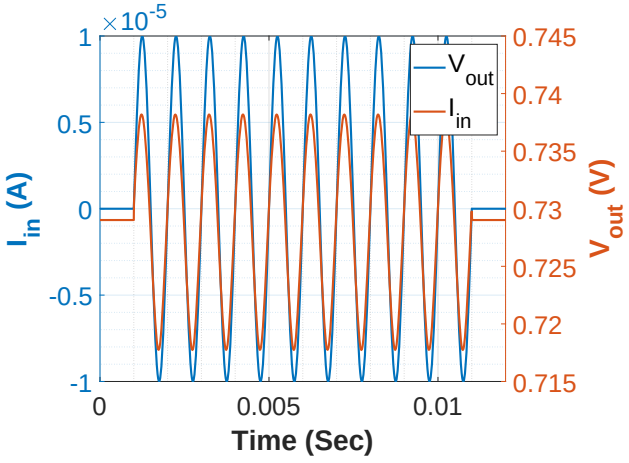

Figure 16: Post-layout simulated time-domain response.

be maximized in magnitude, where the group delay is a negative value. Here, the green area in Model 2.a in Figure 2 is estimated as a rectangular area and that area is the magnitude of FoM. The comparison of several NGD studies is summarized in Table 6. A negative smaller number of FoM indicates a better result regarding the NGD operation frequency range and NGD value.[1]

6. Conclusion and Future Applications

This article introduced a resistorless OTA-C-based active NGD circuit. NGD value from 200 µs to 100 ns is achieved considering different capacitor values and α values. Thus, the NGD operation range changes from 700 Hz to 700 kHz. The total area of the circuit and power consumption is lower than prior active NGD circuits. The post-layout simulations show that the study will suit mixed-mode sensor delay compensation. In future applications, the given circuit will be used to achieve different NGD values in the same system. In addition to that, g_m value controlling can be

[1]This study is based on a gaussian pulse input when the pulse width is approximately 100ms.

Table 5
Brief comparison of the simulation results.

$\alpha = 0.125$	GD (µs)	NGD Operation Range (kHz)	$f_{-3dB_{hf}}$ (MHz)	Gain in the NGD Operation Range (dB)
Calculation	–15.50	8.95	178	66.88
LTspice pre-layout simulation	–18.21	7.05	173	59.95
Magic post-layout simulation	–18.37	7.73	205	60.11

Table 6
Comparison of the NGD studies.

Study	GD (µs)	NGD Operation Range (kHz)	FoM	Circuit Structure
[1]	–74.5	3.95	$-294 \cdot 10^{-3}$	Passive RL-RC Network
[6]	–12000	0.010[1]	$-120 \cdot 10^{-3}$	OA Based Active Filter
[12]	–100	1	$-100 \cdot 10^{-3}$	Passive RL-RC Network
[13]	–0.8	10	$-8 \cdot 10^{-3}$	Cascaded CFOA Based Active Filter
This Study	–18.37	7.73	$-142 \cdot 10^{-3}$	OTA-C Based Active Filter

future research as a solution to designing different layouts for different transistor sizing.

Compliance with Ethical Standards

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Ethical Approval: This article does not contain any studies with human participants or animals performed by any of the authors.

Consent to Participate: All the authors involved have agreed to participate in this submitted article.

Consent to Publish: All the authors involved in this manuscript give full consent for publication of this submitted article.

CRediT authorship contribution statement

Onat Baloglu: Conceptualization of this study, Software, Validation, Formal Analysis, Investigation, Data Curation, Writing – original draft preparation, Writing – review and editing, Visualization. **Oguzhan Cicekoglu:** Conceptualization of this study, Methodology, Formal Analysis, Writing – original draft preparation, Writing – review and editing, Supervision, Project Administration. **Norbert Herencsar:** Conceptualization of this study, Methodology, Resources, Writing – original draft preparation, Writing – review and editing, Visualization, Supervision, Funding Acquisition.

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