

Product Technical Specification

Device MTRD

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1.0 FUNCTIONAL AND PARAMETRICAL SPECIFICATIONS

The reference design will comply with the specifications listed in this section. All warranted parameters and functions in this section are put in trackers.

1.1 Block Diagram

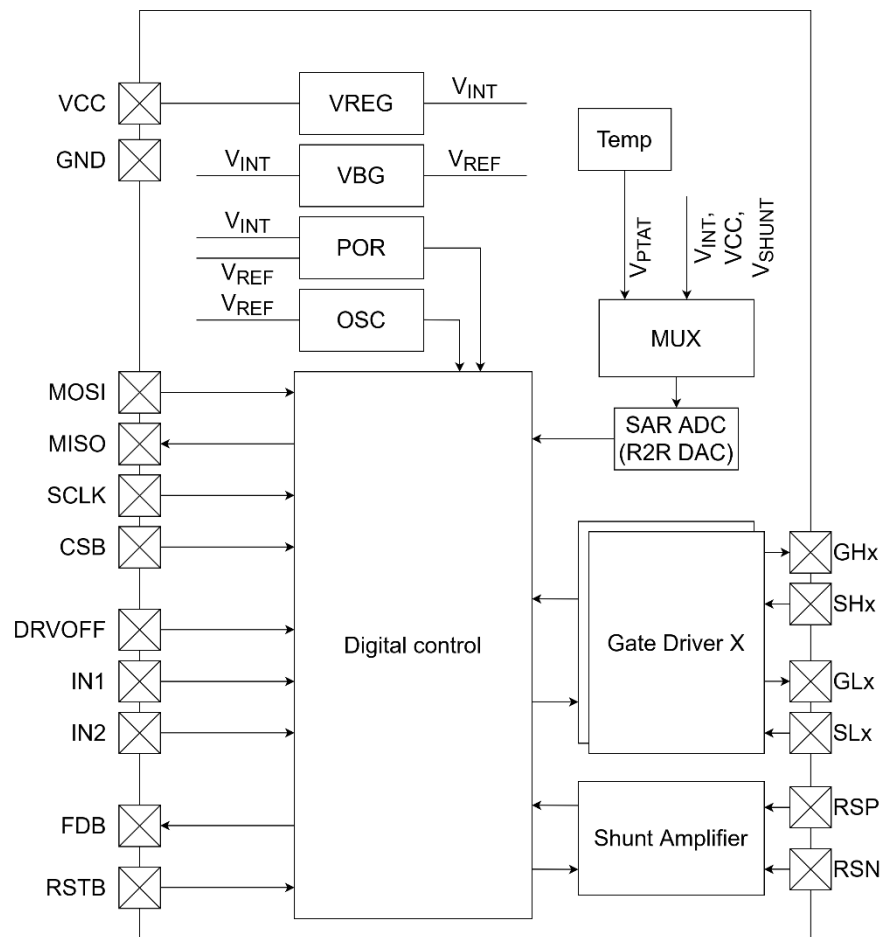


Figure 1: Block diagram

1.2 Analog Blocks Specification

The analog blocks specification is out of the scope of the diploma thesis.

1.2.1 RC Oscillator

The trimmable RC oscillator generates system clock for the whole reference design. The frequency calibration is performed by onsemi (register trim_osc[3:0]).

Table 1: RC oscillator parameters

Tracker	Symbol	Parameter	Min	Typ	Max	Units	Notes
P_RCOSC_01.0	fs	System clock frequency after trimming	19	20	21	MHz	
P_RCOSC_02.0	RC_DUC	Oscillator duty cycle at trimmed frequency	45	50	55	%	

1.3 Digital Blocks Specification

1.3.1 Reset generator

[Main reset (rst_main_b) shall be asserted if at least one of the following conditions is met:

- RSTB pin is low
- PORB comparator output is low [F_MTRD_RSTGEN_0010.v01](#)

[Main reset (rst_main_b) shall be asserted asynchronously. [F_MTRD_RSTGEN_0020.v01](#)

[Main reset (rst_main_b) shall be released synchronously after two rising edges of main clock. [F_MTRD_RSTGEN_0030.v01](#)

[System reset (rst_sys_b) shall be asserted synchronously on rising edge of main clock if the following condition is met:

- Main FSM is not in NORMAL state [F_MTRD_RSTGEN_0040.v01](#)

[System reset (rst_sys_b) shall be asserted asynchronously at the same time as main reset (rst_main_b). [F_MTRD_RSTGEN_0050.v01](#)

[System reset (rst_sys_b) shall be released synchronously on rising edge of main clock. [F_MTRD_RSTGEN_0060.v01](#)

[Communication interface reset (rst_comm_b) shall be asserted synchronously on rising edge of main clock if all of the following conditions are met:

- DRVOFF pin is below V_{TMTHR}
- Main FSM is in INIT state [F_MTRD_RSTGEN_0070.v01](#)

[Communication interface reset (rst_comm_b) shall be asserted asynchronously at the same time as main reset (rst_main_b). [F_MTRD_RSTGEN_0080.v01](#)

[Communication interface reset (rst_comm_b) shall be released synchronously on rising edge of main clock. [F_MTRD_RSTGEN_0090.v01](#)

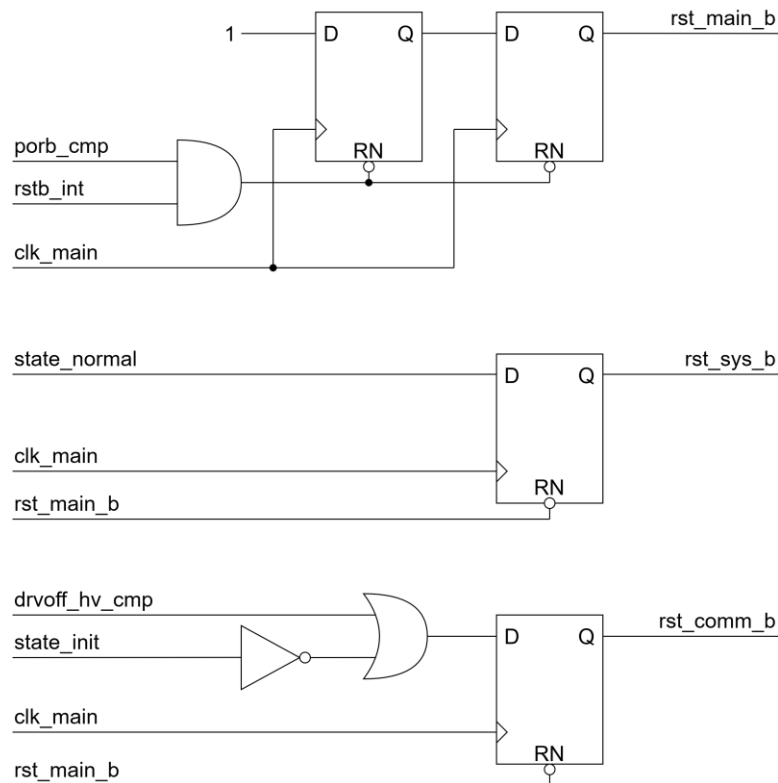


Figure 2: Reset generators

1.3.2 Main FSM

[INIT state shall be entered asynchronously when main reset is asserted. [F_MTRD_MFSM_0010.v01](#)]

[Main FSM FAIL state shall be entered when at least one of the following status flags is set:

- st_mem
- st_wdg
- st_opc
- st_hb [F_MTRD_MFSM_0020.v01](#)]

[Pin FDB shall be low when main FSM is in FAIL state. [F_MTRD_MFSM_0030.v01](#)]

[Main FSM shall be implemented according to figure 3. [F_MTRD_MFSM_0040.v01](#)]

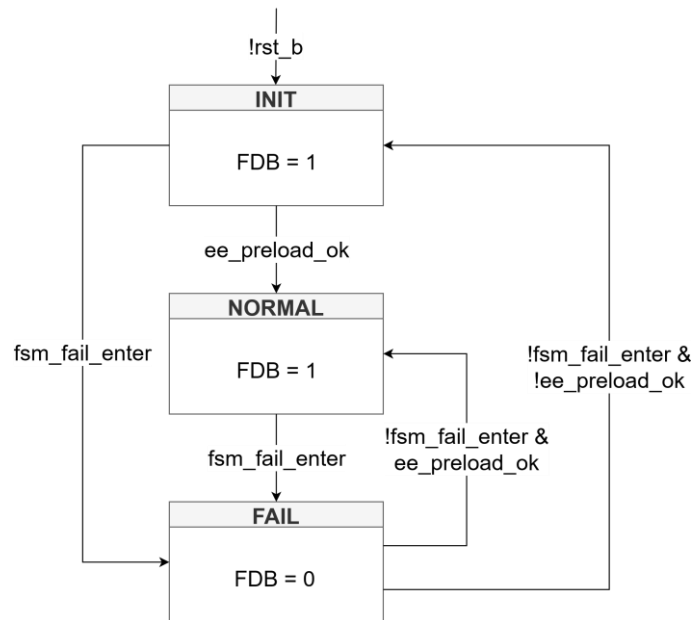


Figure 3: Main FSM

1.3.3 Watchdog

[Watchdog shall be enabled only in NORMAL state of main FSM when SPI register wdg_ena is set to 1.

[F_MTRD_WDG_0010.v01](#)]

[Watchdog timeout period shall be defined by SPI register wdg_to according to table 2. [F_MTRD_WDG_0020.v01](#)]

Table 2: Watchdog timeout period

wdg_to [1:0]	Timeout period [ms]
00	125
01	250
10	500
11	1000

[Watchdog timeout period shall be passivated by valid SPI frame reception in NORMAL state of main FSM.

[F_MTRD_WDG_0030.v01](#)]

[Status flag err_wdg_to shall be set to 1 when timeout period elapsed without passivation.

[F_MTRD_WDG_0040.v01](#)]

[Watchdog timer shall be reset in FAIL state of main FSM or by main reset. [F_MTRD_WDG_0050.v01](#)]

[First timeout period after timer reset (not by passivation) shall be 1000 ms regardless of SPI register wdg_to.

[F_MTRD_WDG_0060.v01](#)]

1.3.4 Measurement controller

[Measurement controller shall be enabled in all main FSM states [F_MTRD_ADCSAR_0010.v01](#)]

[Result of ADC measurement shall be stored in SPI registers according to table 3. [F_MTRD_ADCSAR_0020.v01](#)]

Table 3: SAR ADC measurement channels

Register	Stored value source
vcc	external supply voltage
vint	internal supply voltage
vtemp	temperature of the die
vshunt	voltage on external shunt resistor

[Measurements shall be updated in loop following pattern: vcc, vint, vtemp, vshunt. [F_MTRD_ADCSAR_0030.v01](#)]

[Value of vtemp shall be calculated from measured voltage V_{PTAT} and vtemp_offset:

- when vtemp_offset [6] = 0: vtemp = measured value + vtemp_offset [5:0]

- when vtemp_offset [6] = 1: vtemp = measured value – vtemp_offset [5:0]

overflow and underflow protection shall be implemented. [F_MTRD_ADCSAR_0040.v01](#)]

1.3.5 H-bridge controller

[Two flip-flops shall be used for resynchronization of DRVOFF, IN1 and IN2 inputs. [F_MTRD_HBRIDGE_0010.v01](#)]

[Pulses shorter than 4 main clock periods (200 ns) on gate driver V_{GS} comparators shall be filtered (gdX_lsgs_low_deb and gdX_hsgs_low_deb). [F_MTRD_HBRIDGE_0020.v01](#)]

[H-bridge controller shall be enabled only in NORMAL state of main FSM. [F_MTRD_HBRIDGE_0030.v01](#)]

[GHx and GLx output pins shall be low when main FSM is not in NORMAL state. [F_MTRD_HBRIDGE_0040.v01](#)]

[Minimum PWM period of H-bridge control signals shall be 5000 ns. [F_MTRD_HBRIDGE_0050.v01](#)]

[Duty cycle of PWM H-bridge control signals shall be 50%. [F_MTRD_HBRIDGE_0060.v01](#)]

[H-bridge controller shall have two modes selectable by SPI register hb_mode according to table 4. [F_MTRD_HBRIDGE_0070.v01](#)]

Table 4: H-bridge controller modes

H-bridge controller mode	hb_mode
Half-bridge	0
H-bridge	1

[Dead-time t_{DEAD} shall be implemented according to table 5. [F_MTRD_HBRIDGE_0080.v01](#)]

Table 5: H-bridge dead-time configuration

hb_dead	Dead-time t_{DEAD} [ns]
0	0
1	200
2	400
3	800
4	1000
5	2000
6	4000
7	8000

[Dead-time shall be defined as time between reaching V_{GSTHR} amplitude on falling voltage (gdX_lsgs_low_deb or gdX_hsgs_low_deb rising edge) and start of rising voltage on opposite side (gdX_hs_drv_deb or gdX_ls_drv_deb rising edge respectively). [F_MTRD_HBRIDGE_0090.v01](#)]

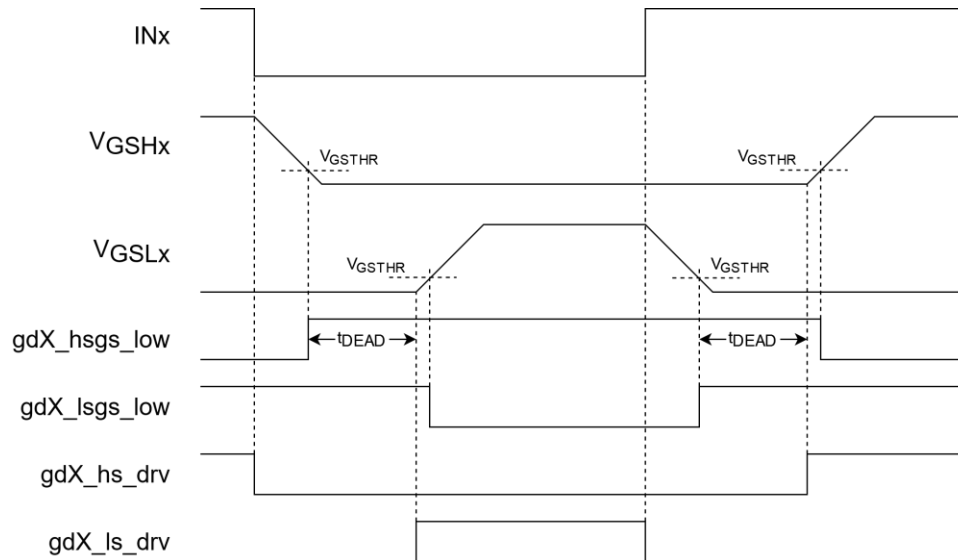


Figure 4: H-bridge dead-time waveform

1.3.5.1 Half-bridge mode

[In half-bridge mode, each gate driver shall be controlled independently. [F_MTRD_HBRIDGE_0100.v01](#)]

[Outputs of gate drivers shall be driven according to table 6. [F_MTRD_HBRIDGE_0110.v01](#)]

Table 6: Half-bridge mode behavior

DRVOFF or hb_drvoff or hb_disx	INx	GHx	GLx
0	0	L	H
0	1	H	L
1	X	L	L

1.3.5.2 H-bridge mode

[Outputs of gate driver shall be driven according to table 7. [F_MTRD_HBRIDGE_0120.v01](#)]

Table 7: H-bridge mode behavior

DRVOFF or hb_drvoff	IN1 (PWM)	IN2 (direction)	hb_fw	GH1	GL1	GH2	GL2	Description
0	0	X	0	L	H	L	H	Low-side active freewheel
0	0	X	1	H	L	H	L	High-side active freewheel
0	1	0	X	L	H	H	L	Reverse drive
0	1	1	X	H	L	L	H	Forward drive
1	X	X	X	L	L	L	L	Diode freewheel

1.3.6 SPI interface

[Two flip-flops shall be used for resynchronization of MOSI, SCLK and CSB inputs. [F_MTRD_SPICTRL_0010.v01](#)]

[Data on MOSI pin shall be sampled on SCLK rising edge, from MSB to LSB. [F_MTRD_SPICTRL_0020.v01](#)]

[Data on MISO shall be shifted-out on SCLK falling edge, from MSB to LSB. [F_MTRD_SPICTRL_0030.v01](#)]

[MISO shall be in high-impedance state when CSB is high or when communication interface reset is asserted. [F_MTRD_SPICTRL_0040.v01](#)]

[SPI interface shall be functional in INIT state of main FSM when pin DRVOFF is above threshold V_{TMTHR} (drvoff_hv_cmp_deb = 1). [F_MTRD_SPICTRL_0050.v01](#)]

[Pulses shorter than 16 main clock periods on DRVOFF threshold comparator shall be filtered [F_MTRD_SPICTRL_0060.v01](#)]

[Functionality in NORMAL and FAIL state of main FSM shall be enabled regardless of the DRVOFF pin. [F_MTRD_SPICTRL_0070.v01](#)]

[SPI interface timing parameters shall be implemented according to figure 5 and table 8. [F_MTRD_SPICTRL_0080.v01](#)]

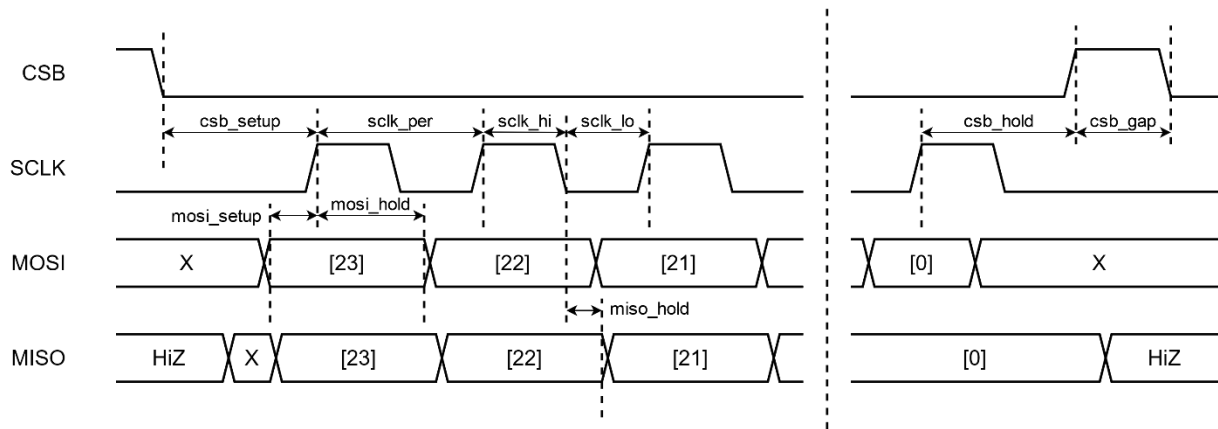


Figure 5: SPI frame waveform

Table 8: SPI parameters

Tracker	Symbol	Parameter	Min	Typ	Max	Units
P_CSB_SETUP	csb_setup	CSB setup time before first SCLK rising edge	300			ns
P_CSB_HOLD	csb_hold	CSB hold time after last SCLK rising edge	150			ns
P_CSB_GAP	csb_gap	Gap between two CSB low pulses	500			ns
P_SCLK_PER	sclk_per	SCLK clock period	300			ns
P_SCLK_HI	sclk_hi	Duration of SCLK high level pulse	0.4 x sclk_per		0.6 x sclk_per	ns
P_SCLK_LO	sclk_lo	Duration of SCLK low level pulse	0.4 x sclk_per		0.6 x sclk_per	ns
P_MOSI_SETUP	mosi_setup	MOSI setup time before each SCLK rising edge	25			ns
P_MOSI_HOLD	mosi_hold	MOSI hold time after each SCLK rising edge	25			ns
P_MISO_HOLD	miso_hold	MISO hold time after each SCLK falling edge	0		100	ns

[Transmitted data shall be 24 bits long. [F_MTRD_SPICTRL_0090.v01](#)]

[Format of write frame shall be implemented as described by table 9. [F_MTRD_SPICTRL_0100.v01](#)]

Table 9: SPI write frame

Bits	[23]	[22:16]	[15:8]	[7:6]	[5:0]
MOSI	CMD	WRITE_ADDR [6:0]	WRITE_DATA [7:0]	FRM_CNT [1:0]	CRC [5:0]
MISO	STATUS [7:0]		1	WRITE_ADDR [6:0]	FRM_CNT [1:0]
					CRC [5:0]

[Format of read frame shall be implemented as described by table 10. [F_MTRD_SPICTRL_0110.v01](#)]

Table 10: SPI read frame

Bits	[23]	[22:16]	[15:8]	[7:6]	[5:0]
MOSI	CMD	READ_ADDR [6:0]	DONT_CARE [7:0]	FRM_CNT [1:0]	CRC [5:0]
MISO	STATUS [7:0]		READ_DATA [7:0]	FRM_CNT [1:0]	CRC [5:0]

[CMD shall be 1 for write frame and 0 for read frame. [F_MTRD_SPICTRL_0120.v01](#)]

[STATUS part of response frame shall be read from SPI register map address 0x00. [F_MTRD_SPICTRL_0130.v01](#)]

[DONT_CARE data shall be considered only for CRC calculation. [F_MTRD_SPICTRL_0140.v01](#)]

[READ_DATA part of response frame shall be read from SPI register map address selected by READ_ADDR. [F_MTRD_SPICTRL_0150.v01](#)]

[Read from reserved address shall return all zeroes in READ_DATA. [F_MTRD_SPICTRL_0160.v01](#)]

[Internal frame counter shall be incremented when valid frame is received (frame counter shall overflow to 0). [F_MTRD_SPICTRL_0170.v01](#)]

[SPI frame CRC shall use polynomial 0x2C and starting value 0x3F (HD = 4). [F_MTRD_SPICTRL_0180.v01](#)]

[SPI frame CRC shall be calculated after CSB rising edge. [F_MTRD_SPICTRL_0190.v01](#)]

[SPI frame shall be considered invalid when at least one of the following occurs:

- received SPI frame has incorrect length
- CRC calculated over all bits (including CRC) of received SPI frame is not 0
- internal frame counter is not equal to received FRM_CNT [F_MTRD_SPICTRL_0200.v01](#)

[WRITE_DATA shall be written to WRITE_ADDR address in SPI register map only when received SPI frame is valid and registers on requested address are writeable. [F_MTRD_SPICTRL_0210.v01](#)]

[Status flag err_spi_wro shall be set to 1 when received SPI frame requests write to read-only SPI register. [F_MTRD_SPICTRL_0220.v01](#)]

[Status flag err_spi_len shall be set to 1 when received SPI frame is not 24 bits long. [F_MTRD_SPICTRL_0230.v01](#)]

[Status flag err_spi_crc shall be set to 1 when CRC calculated over all bits (including CRC) of received SPI frame is not 0. [F_MTRD_SPICTRL_0240.v01](#)]

[Status flag err_spi_fc shall be set to 1 when internal frame counter is not equal to received FRM_CNT. [F_MTRD_SPICTRL_0250.v01](#)]

1.3.6.1 SPI register map

[SPI register map shall be implemented as described by table 11 [F_MTRD_SPIREGS_0010.v01](#)]

Ready only (RO)
Clear by write (CBW)
Read/Write (RW)
Read/Write Locked (RWL)

Table 11: SPI register map

Address\Bit		7	6	5	4	3	2	1	0
0	0x00	fsm_state		st_mem	st_wdg	st_opc	st_hb	st_spi	wrn
1	0x01								err_ee
2	0x02								err_wdg_to
3	0x03						err_tsd	err_ov	err_uv
4	0x04								err_hb_oc
5	0x05					err_spi_wro	err_spi_len	err_spi_crc	err_spi_fc
6	0x06							wrn_tw	wrn_por
7	0x07					pin_csb	pin_drvoff	pin_in2	pin_in1
8	0x08	vshunt [7:0]							
9	0x09	vcc [7:0]							
10	0x0A	vint [7:0]							
11	0x0B	vtemp [7:0]							
12	0x0C								msk_wdg_to
13	0x0D						msk_tsd	msk_ov	msk_uv
14	0x0E								msk_hb_oc
15	0x0F					msk_spi_wro	msk_spi_len	msk_spi_crc	msk_spi_fc
16	0x10							msk_tw	msk_por
17	0x11						wdg_ena	wdg_to [1:0]	
18	0x12	hb_drvoff	hb_dis2	hb_dis1	hb_dead [2:0]			hb_fw	hb_mode
19	0x13	hb_vsthr [7:0]							
20	0x14	tw_offset [7:0]							
...	...								
64	0x40	keycode [7:0]							
65	0x41	vtemp_offset [6:0]							msk_all
66	0x42	tsd_thr [7:0]							
67	0x43	uv_thr [7:0]							
68	0x44	ov_thr [7:0]							
69	0x45	trim_bg [3:0]				trim_osc [3:0]			
70	0x46	trim_vreg [3:0]				trim_porb [3:0]			
71	0x47	trim_shunt [3:0]				trim_temp [3:0]			
72	0x48	trim_adc_cmp [3:0]				trim_adc_ref [3:0]			
73	0x49	trim_gd2 [3:0]				trim_gd1 [3:0]			

74	0x4A	dlt_wafer [3:0]	dlt_lot [3:0]
75	0x4B	dlt_x [7:0]	
76	0x4C	dlt_y [7:0]	

[All clear by write registers shall prioritize set function (rather than clear function). [F_MTRD_SPIREGS_0020.v01](#)]

[Any clear by write (CBW) SPI register shall be cleared by writing 1 to it. [F_MTRD_SPIREGS_0030.v01](#)]

[SPI register map reset values shall be implemented as described:

- wrn_por: 1

other registers shall be initialized to 0 [F_MTRD_SPIREGS_0040.v01](#)]

[Masking of threshold signals used in error detection shall be disabled only after successful preload:

- tsd_thr: 240,

- tw_offset: 15,

- uv_thr: 15,

- ov_thr: 240,

- hb_vsthr: 240 [F_MTRD_SPIREGS_0050.v01](#)]

[Masking of trimming signals to analog shall be disabled only after successful preload:

- trim_bg: 8,

- trim_osc: 8,

- trim_vreg: 8,

- trim_porb: 8,

- trim_adc_ref: 8,

- trim_adc_cmp: 8 [F_MTRD_SPIREGS_0060.v01](#)]

[Read/Write Locked (RWL) SPI registers shall be readable and writeable only when SPI register keycode = 0xAC and pin DRVOFF is above threshold V_{TMTHR} (drvoff_hv_cmp = 1). [F_MTRD_SPIREGS_0070.v01](#)]

[Read of RWL SPI registers shall return all zeroes when SPI register keycode is not equal to 0xAC or pin DRVOFF is below threshold V_{TMTHR} . [F_MTRD_SPIREGS_0080.v01](#)]

[Read of SPI register keycode shall always return all zeroes. [F_MTRD_SPIREGS_0090.v01](#)]

[Status flag fsm_state (main FSM state) shall be driven according to table 12. [F_MTRD_SPIREGS_0100.v01](#)]

Table 12: SPI register fsm_state behavior

Main FSM state	fsm_state
INIT	1
NORMAL	2
FAIL	3

[Status flag st_mem (Memory status) shall be set to 1 when any of the following status flags is set set to 1:

- err_ee [F_MTRD_SPIREGS_0110.v01](#)]

[Status flag st_wdg (Watchdog status) shall be set to 1 when any of the following status flags is set to 1:

- err_wdg_to [F_MTRD_SPIREGS_0120.v01](#)]

[Status flag st_hb (H-bridge status) shall be set to 1 when any of the following status flags is set to 1:

- err_hb_oc [F_MTRD_SPIREGS_0130.v01](#)]

[Status flag st_opc (operational conditions) shall be set to 1 when any of the following status flags is set to 1:

- err_tsd

- err_ov

- err_uv [F_MTRD_SPIREGS_0140.v01](#)]

[Status flag st_spi (SPI status) shall be set to 1 when any of the following status flags is set to 1:

- err_spi_wro

- err_spi_len

- err_spi_crc

- err_spi_fc [F_MTRD_SPIREGS_0150.v01](#)]

[Status flag wrn (warning) shall be set to 1 when any of the following status flags is set to 1:

- wrn_tw
- wrn_por [F_MTRD_SPIREGS_0160.v01](#)]

[Logic associated with masked status registers shall behave as if they were clear, even when they are set to 1. [F_MTRD_SPIREGS_0170.v01](#)]

[Status flags shall be masked according to table 13. [F_MTRD_SPIREGS_0180.v01](#)]

Table 13: SPI register masking

Mask	Masked status register
msk_wdg_to	err_wdg_to
msk_uv	err_uv
msk_ov	err_ov
msk_tsd	err_tsd
msk_hb_oc	err_hb_oc
msk_spi_fc	err_spi_fc
msk_spi_crc	err_spi_crc
msk_spi_len	err_spi_len
msk_spi_wro	err_spi_wro
msk_por	wrn_por
msk_tw	wrn_tw

[SPI register pin_csb shall hold resynchronized (2xFF) value of input pin CSB. [F_MTRD_SPIREGS_0190.v01](#)]

[SPI register pin_drvoff shall hold resynchronized (2xFF) value of input pin DRVOFF. [F_MTRD_SPIREGS_0200.v01](#)]

[SPI register pin_in1 shall hold resynchronized (2xFF) value of input pin IN1. [F_MTRD_SPIREGS_0210.v01](#)]

[SPI register pin_in2 shall hold resynchronized (2xFF) value of input pin IN2. [F_MTRD_SPIREGS_0220.v01](#)]

[Status flag err_tsd shall be set to 1 when value in SPI register vtemp is equal or above value in SPI register tsd_thr. [F_MTRD_SPIREGS_0230.v01](#)]

[Status flag wrn_tw shall be set to 1 when value in SPI register vtemp is equal or above (tsd_thr - tw_offset). [F_MTRD_SPIREGS_0240.v01](#)]

[Status flag err_ov shall be set to 1 when value in SPI register vcc is equal or above value in SPI register ov_thr. [F_MTRD_SPIREGS_0250.v01](#)]

[Status flag err_uv shall be set to 1 when value in SPI register vcc is equal or below value in SPI register uv_thr. [F_MTRD_SPIREGS_0260.v01](#)]

[Status flag err_hb_oc shall be set to 1 when value in SPI register vshunt is equal or above value in SPI register hb_vsthr. [F_MTRD_SPIREGS_0270.v01](#)]

1.3.7 Non-volatile memory (EEPROM)

[Data stored in EEPROM shall be divided into two sections: customer and onsemi. [F_MTRD_EE_0010.v01](#)]

[Customer data shall be secured by crc_customer. [F_MTRD_EE_0020.v01](#)]

[onsemi data shall be secured by crc_onsemi. [F_MTRD_EE_0030.v01](#)]

[Customer data CRC shall use polynomial 0x97 and starting value 0xFF (HD = 4). The CRC calculation shall be performed from MSB to LSB of each word and from the first to the last address. Unused EEPROM bits shall be substituted with value of 0. [F_MTRD_EE_0040.v01](#)]

[onsemi data CRC shall use polynomial 0x97 and starting value 0xFF (HD = 4). The CRC calculation shall be performed from MSB to LSB of each word and from the first to the last address. Unused EEPROM bits shall be substituted with value of 0. [F_MTRD_EE_0050.v01](#)]

[All data stored in EEPROM shall be preloaded into shadow memory at startup and on request.

[F_MTRD_EE_0060.v01\]](#)

[EEPROM refresh/preload shall be followed by CRC check of each shadow memory section, using crc_customer and crc_onsemi. [F_MTRD_EE_0070.v01\]](#)

[Failed CRC check after EEPROM refresh/preload shall trigger one more EEPROM refresh. Only two consecutive EEPROM refreshes are allowed. [F_MTRD_EE_0080.v01\]](#)

[Status flag err_ee (EEPROM error) shall be set to 1 after two failed refreshes from EEPROM.

[F_MTRD_EE_0090.v01\]](#)

[Shadow memory of customer data shall start at SPI register address 0x0C and end on address 0x14.

[F_MTRD_EE_0100.v01\]](#)

[Shadow memory of onsemi data shall start at SPI register address 0x41 and end on address 0x4C.

[F_MTRD_EE_0110.v01\]](#)

[EEPROM map shall be implemented as described by table 14. [F_MTRD_EE_0120.v01\]](#)

Customer
onsemi

Table 14: EEPROM map

Address\Bits		7	6	5	4	3	2	1	0	
0	0x00								msk_wdg_to	
1	0x01						msk_tsd	msk_ov	msk_uv	
2	0x02								msk_hb_oc	
3	0x03					msk_spi_wro	msk_spi_len	msk_spi_crc	msk_spi_fc	
4	0x04							msk_tw	msk_por	
5	0x05						wdg_ena	wdg_to [1:0]		
6	0x06	hb_drvoff	hb_dis2	hb_dis1	hb_dead [2:0]				hb_fw	hb_mode
7	0x07	hb_vsthr [7:0]								
8	0x08	tw_offset [7:0]								
9	0x09	crc_customer [7:0]								
10	0x0A	vtemp_offset [6:0]							msk_all	
11	0x0B	tsd_thr [7:0]								
12	0x0C	uv_thr [7:0]								
13	0x0D	ov_thr [7:0]								
14	0x0E	trim_bg [3:0]				trim_osc [3:0]				
15	0x0F	trim_vreg [3:0]				trim_porb [3:0]				
16	0x10	trim_shunt [3:0]				trim_temp [3:0]				
17	0x11	trim_adc_cmp [3:0]				trim_adc_ref [3:0]				
18	0x12	trim_gd2 [3:0]				trim_gd1 [3:0]				
19	0x13	dlt_wafer [3:0]				dlt_lot [3:0]				
20	0x14	dlt_x [7:0]								
21	0x15	dlt_y [7:0]								
22	0x16	crc_onsemi [7:0]								

1.4 Analog-digital interface

Table 15: AD interface

Digital signal name	Direction	Function description
mosi_int	from ana	SPI data input
miso_out	to ana	SPI data output
miso_hiz	to ana	SPI data output in high-impedance state when '1'
sclk_int	from ana	SPI clock
csb_int	from ana	SPI chip-select (active low)
drvoff_int	from ana	DRVOFF input
in1_int	from ana	IN1 input
in2_int	from ana	IN2 input
fdb_out	to ana	FDB output (active low)
rstb_int	from ana	RSTB input (active low)
clk_main	from ana	Main clock signal for digital
drvoff_hv_cmp	from ana	Pin DRVOFF voltage is above V_{TMTHR} threshold
porb_cmp	from ana	PORB comparator output (active low)
gd1_hs_drv	to ana	Gate driver 1 high side switch (GH1 is high when '1')
gd1_ls_drv	to ana	Gate driver 1 low side switch (GL1 is high when '1')
gd1_hsgs_low	from ana	Gate driver 1 high side V_{GSH1} below V_{GSTHR}
gd1_lsgs_low	from ana	Gate driver 1 low side V_{GSL1} below V_{GSTHR}
gd2_hs_drv	to ana	Gate driver 2 high side switch (GH2 is high when '1')
gd2_ls_drv	to ana	Gate driver 2 low side switch (GL2 is high when '1')
gd2_hsgs_low	from ana	Gate driver 2 high side V_{GSH2} below V_{GSTHR}
gd2_lsgs_low	from ana	Gate driver 2 low side V_{GSL2} below V_{GSTHR}
meas_sel	to ana	ADC measurement multiplexer channel selection
sar_cmp	from ana	SAR comparator output (meas. voltage > ref. voltage when '1')
sar_sh	to ana	SAR sample & hold (sampling when '1')
sar_bus	to ana	SAR bus to ref. DAC
trim_osc	to ana	Trimming of oscillator
trim_bg	to ana	Trimming of bandgap reference
trim_porb	to ana	Trimming of PORB comparator
trim_vreg	to ana	Trimming of voltage regulator
trim_temp	to ana	Trimming of V_{PTAT}
trim_shunt	to ana	Trimming of shunt amplifier
trim_adc_ref	to ana	Trimming of SAR ADC reference voltage
trim_adc_cmp	to ana	Trimming of SAR ADC comparator
trim_gd1	to ana	Trimming of gate driver 1
trim_gd2	to ana	Trimming of gate driver 2