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ÚSTAV MIKROELEKTRONIKY

SPICE MODEL OF LDMOS STRUCTURE

SPICE MODEL STRUKTURY LDMOS

BACHELOR'S THESIS
BAKALÁŘSKÁ PRÁCE

AUTHOR Dmitrii Loginov
AUTOR PRÁCE

SUPERVISOR Ing. Edita Hejátková
VEDOUCÍ PRÁCE

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Student: Dmitrii Loginov ***ID:*** 195380

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TITLE OF THESIS:

SPICE model of LDMOS structure

INSTRUCTION:

Create SPICE macro-model of LDMOS transistor structure. Explain physical difference between structure LDMOS and MOS. Discuss how to model such structures using SPICE models. Measure DC and CV characteristics of LDMOS transistor in particular process at ON Semiconductor lab. Choose a way of SPICE modeling. Create a SPICE model for all geometries that covers DC and CV behavior. Describe the procedure of parameters extraction. Document results.

RECOMMENDED LITERATURE:

According to recommendations of supervisor

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Supervisor: Ing. Edita Hejátková
Consultant: Ing. Petr Běťák, Ph.D, ON Design Czech s.r.o.

doc. Ing. Jiří Háze, Ph.D.
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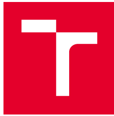

VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ
FAKULTA ELEKTROTECHNIKY A KOMUNIKAČNÍCH TECHNOLOGIÍ

Bakalářská práce

bakalářský studijní obor **Mikroelektronika a technologie**
Ústav mikroelektroniky

Student: Dmitrii Loginov ***ID:*** 195380
Ročník: 3 ***Akademický rok:*** 2018/19

NÁZEV TÉMATU:

SPICE model struktury LDMOS

POKYNY PRO VYPRACOVÁNÍ:

Vytvořte SPICE model tranzistorové struktury LDMOS. Vysvětlete čím se liší struktura tranzistoru LDMOS od konvenční struktury tranzistoru MOS. Rozeberte možnosti modelovaní takové struktury pro SPICE simulátory. Změřte DC a CV charakteristiky LDMOS tranzistoru v konkrétní technologii v laboratoři ON Semiconductor. Zvolte způsob jakým budete takový tranzistor modelovat. Vytvořte SPICE model pro kompletní matici rozměrů změřeného tranzistoru, který bude popisovat změřené DC a CV charakteristiky. Popište postup extrakce SPICE parametrů. Zdokumentuje výsledek.

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Vedoucí práce: Ing. Edita Hejátková
Konzultant: Ing. Petr Běťák, Ph.D, ON Design Czech s.r.o.

doc. Ing. Jiří Háze, Ph.D.
předseda oborové rady

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ABSTRACT

In this bachelor thesis, comparison of Lateral Double-diffused MOS against conventional MOS structure is presented. Anomalous effects, issues that this high-voltage device brings to modeling and characterization, and theoretical analysis of this type of structure are described in the first chapter. Next part of this project is focused on possible approaches in characterization that is used in the semiconductor industry, of LDMOS. The BSIM methodology, described in chapter two, has been chosen to create a DC and CV model of an n-type LDMOS device measured at the ON semiconductor laboratory. The steps of characterization, such as measurement, tuning of characteristics to an optimized BSIM4 parameter set are reported in the last chapters of this work.

KEYWORDS

High Voltage MOS, LDMOS, MOSFET, DC model, CV model, characterization, BSIM, BSIM4

ABSTRAKT

V této bakalářské práci je provedeno porovnání struktury LDMOS oproti konvenční MOS struktuře. Anomální efekty, výzvy, které tato struktura přináší do oblasti modelování a charakterizace jsou popsány v první kapitole. Další část této práce se zaměřuje na existující možné přístupy v charakterizaci LDMOS struktury, které se používají v polovodičovém průmyslu. V druhé kapitole je také popsána BSIM metodologie, která je dále použitá pro vytváření modelu LDMOS popisujícího DC a CV chování. Kroky charakterizace, která probíhala v laboratoři ON Semiconductor, jakožto měření součástky a ladění charakteristik modelu až do výsledného souboru parametrů BSIM4, jsou uvedeny v posledních kapitolách této práce.

KLÍČOVÁ SLOVA

Vysokonapěťový MOS, LDMOS, MOSFET, DC model, CV model, charakterizace, BSIM, BSIM4

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ROZŠÍŘENÝ ABSTRAKT

V dnešní době existuje čím dál větší poptávka po vysokonapěťových součástkách na bázi CMOS technologií. Jako příklad si uveďme neustálé zvyšování počtu funkčních elektronických bloků v moderních automobilech. Jejich správný provoz a funkce vyžaduje čím dál větší napájecí napětí a výkony. Proto se od osmdesátých let minulého století technologové zabývají polovodičovými strukturami, které to dokáží zvládnout. Od té doby bylo vytvořeno velké množství různých architektur principiálně shodných s konvenční MOS strukturou. Jedna z nich je LDMOS, jehož modelováním se zabývá táto práce.

Charakterizace součástky je velice důležitá pro její další použití. Správně fungující model pomáhá pochopit fyzikální podstatu a zaručuje patřičnou funkci prvků v zapojení či struktuře. Čím lépe charakteristiky odpovídají měřeným datům, tím je vyšší spolehlivost a jakost výrobků obsahujících tuto součástku.

V této práci je popsána charakterizace laterálního tranzistorů DMOS. Na začátku jsou rozebrány rozdíly této vysokonapěťové součástky od konvenčního tranzistorů MOS. A to jsou:

- Rozšířená driftová oblast
- Krátká a fixní délka kanálu
- Asymetrická struktura
- Větší napěťový rozsah

Těmito rozdíly jsou značně ovlivněny charakteristiky a chování tranzistoru . Vyskytují se zde anomální jevy netypické pro konvenční MOS strukturu. Jako významné můžeme označit: Kvazisaturace, Self-heating, kink a Kirkův jevy.

Následně byly prodiskutované možnosti modelování LDMOS struktury. Hlavní požadavky na model jsou:

- Kompatibilita se SPICE simulátory
- Rychlost
- Zaručená konvergence
- Množství parametrů
- Fyzikální podstata

Na základě těchto požadavků byl zvolen jeden z pěti způsobů modelování, který byl vyvinut na státní Kalifornské univerzitě v Berkley – BSIM. Tento model byl původně vytvořen pro IGFET tranzistor s krátkým kanálem, ale díky své univerzál-

nosti a velkému počtu speciálních parametrů je použitelný i pro LDMOS strukturu. BSIM je kompatibilní s většinou SPICE simulátorů, je poměrně rychlý, standardní sada jeho parametrů zaručuje dobré konvergenční vlastnosti a některé z nich se dají vyčíst z fyzikálních vlastnosti struktury. Charakterizace součástek je postavena na znalosti jejich struktury, ze které můžeme vyextrahovat základní parametry: technologické i geometrické. Na nich se pak v BSIM metodě dále postaví celý model. Následujícím krokem je měření charakteristik součástek potřebných pro vytváření modelů. Pro účely této práce byly změřeny DC a CV testy popisující výstupní a převodové chování:

- I_D-V_D jak lineární, tak i oblast saturace
- I_D-V_G od nízkého V_{DS} do větších
- C-V profil začínající kapacitami oxidu hradla až do kapacit přechodu

Realizace modelu dále spočívá v ladění těchto charakteristik pomocí úprav BSIM parametrů. Výsledek této změny je vidět na grafech, hlavní snahou je dosáhnout co nejlepší shody simulací a měřených dat. Pro každou z výše popsaných charakteristik jsou zde uvedené použité parametry a jejich vliv na chování křivek. Následně je provedena korekce s ohledem na několik geometrií vybrané struktury. Na závěr kapitoly o DC modelu je uvedena tabulka použitých BSIM parametrů spolu s jejich hodnotami.

Kapacitní model LDMOS tranzistorů, se dále vytvoří na základě výsledků z předchozího kroku. Reprezentuje chování součástky v časové a frekvenční doméně. Pro lepší reprezentaci byl použit obvod se zkratovaným MOS tranzistorem a dvěma diodami. Tyto přídavné elementy nemají vliv na chování součástky v oblasti stejnosměrného použití – slouží tedy pro natvarování celkové kapacitní "jámy" a dílčích kapacit p-n přechodů.

BSIM přístup avšak není ideální. Má své výhody a nevýhody. Některé dílčí části charakteristik nejsou dost dobře ovlivnitelné standardní sadou parametrů. I přesto se podařilo vytvořit model který zohledňuje korektní chování součástky v různých provedeních/geometriích a v DC a AC oblasti použití.

DECLARATION

I declare that I have written the Bachelor's Thesis titled "SPICE model of LDMOS transistor structure" independently, under the guidance of the advisor and using exclusively the technical references and other sources of information cited in the thesis and listed in the comprehensive bibliography at the end of the thesis.

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Brno ....

author's signature

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Introduction

Recent trends in the electronics industry have produced great demand in high-voltage devices. To demonstrate this, we can look at automotive production. Various functions such as electric doors control, air-conditioning, auto-parking, camera sensors and etc. that are now available in modern cars cannot be satisfied with a 12 V battery commonly used in elderly vehicles. The problem leads us forward to increasing the supply voltage to a higher limit to fulfill these requirements. Previous models of smart power devices, based on a standard low-voltage MOS technology, which ensured only a limited number of functions can no longer suffice nowadays. That is why the new approach developed from the conventional MOS, has found demand [1, 2].

Such a high voltage device is a lateral double-diffused MOS, and is examined in this work. The LDMOS is particularly attracting as a power switch and is compatible with standard the CMOS technology [3].

However, existing models representing LDMOS are not accurate enough to respond growing requirements of the industry standards. The difficulty lies in the peculiar physical behavior of this high voltage device compared to MOSFET; thus, many studies proposed a complete LDMOS model trying to represent all deviations and peculiarities of this structure [4].

The first chapter of this thesis is an introduction to LDMOS transistors and their main physical differences compared to conventional MOS transistors. Their use and advantages are reviewed. Anomalous effects compared to conventional MOSFET are discussed as well.

The second chapter describes possible approaches in the modeling of the LDMOS transistor, which are now used in the semiconductor industry. The BSIM4 approach is chosen for further modeling. Its parameters are presented and described.

The third chapter discusses the parameters extraction starting from measurement of DC characteristics of the LDMOS measured on a silicon wafer, to the final model

set. Thus, step by step,empirically obtaining a feedback from the comparison of model output graphs with measured data, the DC model is built.

In the fourth chapter of this work the process of creation capacitance model is reported. C-V measurements, connection diagrams are establishing a basis in the first half. The characterization process including sub-circuit implementation and BSIM parameters fitting follows. Scalable C-V model of the LDMOS is available.

Chapter 1

Comparing LDMOS and MOS

This chapter consists of a comparison between conventional MOS transistor structure and its LDMOS counterpart. They are basically similar to each other : both have matching terminals, same principle of work, based on field-effect, and similar architecture.

Each device is further described with relevant cross-section presented. The main purpose of this chapter is to point out their properties and to introduce the LDMOS structure to a reader.

1.1 MOS Structure

MOSFET — *Metal-Oxide-Semiconductor Field-Effect Transistor*, is a four terminal device which are a gate, a source, a drain, and a substrate. In such a transistor, the gate is separated from the channel by a layer of silicon oxide grown upon the substrate. Gate, is usually made of metal or doped silicon, is completely non-conductive to the drain-source region and affects device only by the applied voltage. Thus, by the appropriate electric field, the inversion layer connecting drain and source terminals, is established, enabling current to flow. However, the gate oxide is very thin and therefore this device is vulnerable to higher voltages [5, 6].

1.1.1 MOS Cross-section

Behavior of a MOSFET is easily demonstrable on the cross-section below. By applying sufficient voltage on the gate terminal the carriers will be brought up to the top, thus gate oxide creates a “capacitor“ which holds the charge in area between drain and source. Hence carriers are able to transfer from drain to source and the device is open.

On the other hand opposite voltage will be pushing the carriers down to the substrate, largely obstructing the current flow path, even for higher voltages between drain and source. Thanks to the symmetry of the device either the drain and the source terminal can act as the effective source, which means that a MOSFET can be used bidirectionally [3, 6].

Bulk terminal is used to influence threshold voltage. With the appliance of reverse bias of V_{BS}, threshold voltage of a MOS transistor increases due to changes in depletion layer width and charge. Therefore such is the practical use of so-called *body effect* [7].

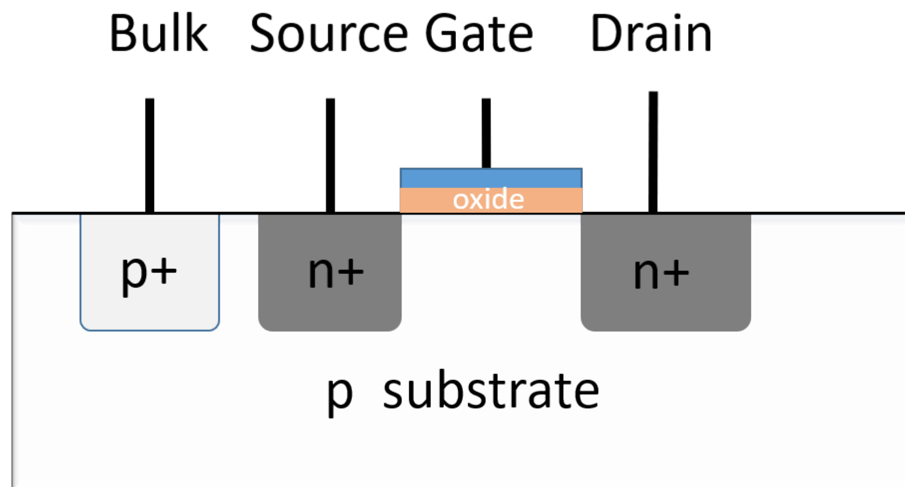

Fig. 1.1: Cross-section of N-type MOSFET [6]

The MOS transistor type is defined by the charge carriers in the drain-source region; N-type — whether the majority of carriers are electrons, or a P-type — in case of holes [6].

1.2 LDMOS Structure

The LDMOS, which stands for *Lateral double-Diffused Metal Oxide Semiconductor*, is a High-Voltage transistor device with a short channel and a self-aligned architecture. The channel is lateral, and doping is gradually non-uniform across it. The working principle of LDMOS is quite similar to that of the conventional low-voltage MOSFET. Both have a drain, source, gate and substrate terminals and also a channel between a drain and a source. In lateral double-Diffused MOS, the current flows across the channel in the horizontal direction. The presence of a low-doped drift region, in addition, helps to preserve higher voltages [1, 4, 6]

However, there are many other implementations of current flows and channel geometries in High-Voltage MOS device technology, such as EDMOS, VMOS, VD-MOS, UMOS, XDMOS and etc. [4]; these, however, will not be discussed in this paper.

As well as MOSFET LDMOS devices are also divided by the type of carries or operation mode as n-type and p-type or as enhancement and depletion mode.

1.2.1 LDMOS Cross-section

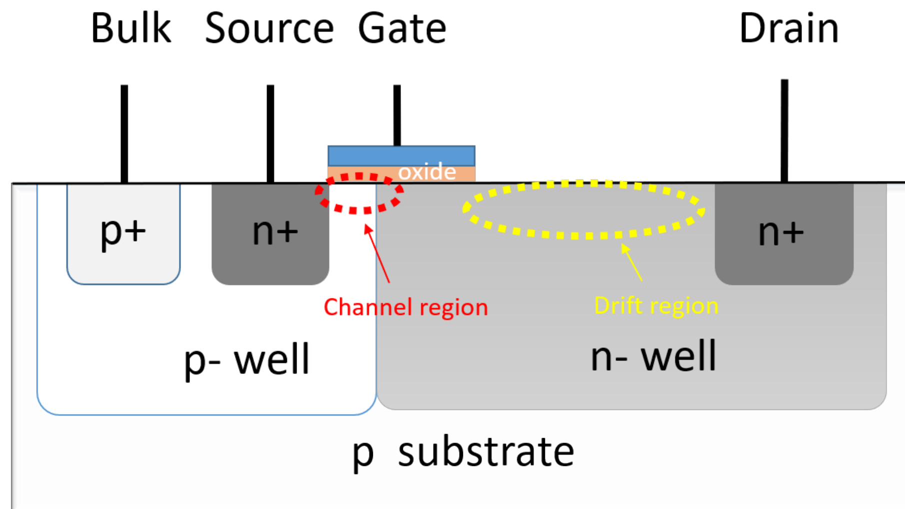

Fig. 1.2: Cross-section of N-type LDMOS transistor[3]

Comparing figures 1.1 and 1.2 one would easily find several differences. First is presence of $n-$ well, which encloses $n+$ drain region and creates a drift region, so the drain terminal is located further than in conventional MOS. That leads to asymmetry of the device and creates issues connected with capacitance modeling. The second is gate and its location. It covers channel completely, but does not expand up to $n+$ drain region as it was in original structure. Last one is the length of a channel that takes narrow part of the region under the gate, only between source $n+$ region and drift area of $n-$ well.

The channel of LDMOS device is relatively short but, thanks to its large area and gradually distributed drain region, it can sustain higher voltages and currents. Hence, this channel quality helps to postpone the impact ionization effect at high voltages. An additional electric field boosts g_m due to the lateral distribution across the channel with doping concentration and its drift resistance [3, 6].

1.2.2 LDMOS applications and advantages

LDMOS transistors with their fine frequency characteristics are commonly used as audio or RF-power amplifiers. Having a proper linearity and a negative temperature coefficient they are used in switching applications and microwave operations [5]. At the same time for their ability to handle high voltages they are appropriate for switch-mode power supplies, motor drivers and other HV applications.[2]

LDMOS can be easily integrated into the CMOS process and therefore they are often used in integrated circuits.

The short channel is an advantage in favor of LDMOS. Thus the transistor works all the time in velocity saturation and high trans-conductance is easy-to-achieve [3].

1.3 Physical differences between LDMOS and MOS

The main physical deviations, anomalous effects of an LDMOS from a conventional MOSFET structure are briefly outlined in this section.

1.3.1 Quasi-saturation

Quasi-saturation is an anomaly that can not be detected in a classic MOSFET structure. In LDMOS, this effect appears because of the existence of drift region and high velocity of saturation in it; the drain current tends to be saturated first not because of the pinch-off of the channel at the drain end, but rather because of the above-stated. At a high gate bias, the drain current dominates in drift region [6].

This phenomenon gives rise to several intriguing consequences. One, as it was mentioned, is linear drain current cut-off at high gate bias, which is presented in fig 1.3. The other is C_{DG}, which can be higher than total gate capacitance due to change in surface potential, which is to be seen further in fourth chapter in fig. 4.3 and in fig. 4.6.

By increasing the doping level in the drift region, this effect can be minimized [8]. As for N-LDMOS that will be outlined in chapter 3, this effect is barely noticeable (fig. 3.6 for instance).

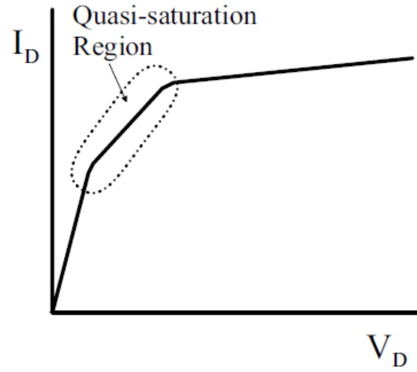

Fig. 1.3: Quasi-saturation on I_D-V_D [6]

1.3.2 Self-heating

Greater operating voltage are accompanied with a higher power which is the reason for the self-heating effect. As in conventional MOSFETs constructed on thick silicon substrates and operating on low voltages, self-heating is a very rare effect. This, however is not true of an LDMOS device. Internal resistance dissipates the flowing current into heat; thus, a higher temperature produces lattice scattering decrease, which leads to a drop in a charge carrier mobility. Additionally to this effect is further magnified by recombination and Thomson heat. In the output characteristic, it is to be seen as current fall with increasing V_{DS} [6].

To demonstrate this effect a P-LDMOS architecture was measured at the ON Semiconductor laboratory. The output graph of this measurement is shown in fig. 1.4 *(Explicit selfheating is on higher gate voltage, light-blue curve saturation decrease).*

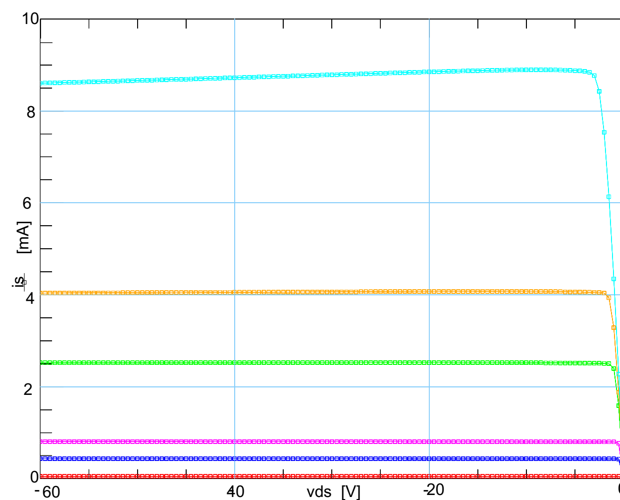

Fig. 1.4: Self-heating effect on I_S-V_D saturation curve

1.3.3 Kink effect

The kink effect is a step-wise increase in drain current which can be seen in the output characteristics of the device. The excess I_{DS} in the saturation region arise from the V_{th} shift due to the forward biasing of the source-substrate diode, which resulted from impact ionization of drain current. The impact ionization rate in a low-doped drift region is insufficient for this effect to occur, thus it is present only in a high doped counterpart [6, 9].

In high-voltage MOSFETs this effect is considered as unwanted, although might be useful in various types of devices and applications. On different measured P-LDMOS this effect appears on several geometries, the step-wise I_{DS} shift due to it is seen in fig 1.5.

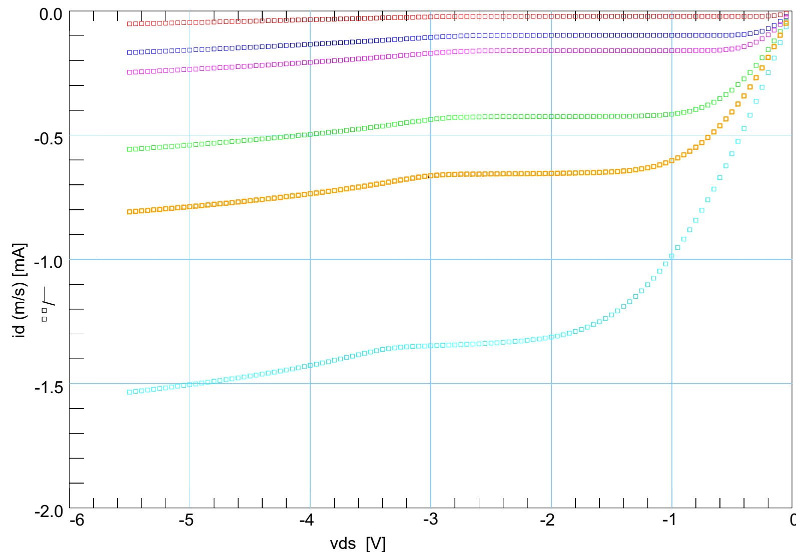

Fig. 1.5: Kink effect measured on P-LDMOS, I_D-V_D

1.3.4 Kirk effect

Kirk effect was discovered during investigation of cut-off frequency in power BJT at high current densities [6]. Kirk effect is described as a breakdown of the drain current on higher V_{DS}. At that moment the increasing amount of minority carriers in the depletion region becomes greater than it can be negligible. Thus Kirk effect leads to a sharper field and an avalanche multiplication on the drain edge, resulting from the impact ionization. In the paper [10], depressing this effect is suggested by increasing majority carriers concentration in the drift region and drift region length [4].

The condition, assuming full ionization, for Kirk effect to occur is presented in inequality 1.1 adduced from [6].

$$J \geq n \cdot q \cdot \nu_s \tag{1.1}$$

where

J is current density in $[A/m^2]$,
n is the minority charge carrier density in depletion region $[m^{-3}]$,
ν_s is the scattering limited velocity in $[m/s]$
q is elementary charge in [C].

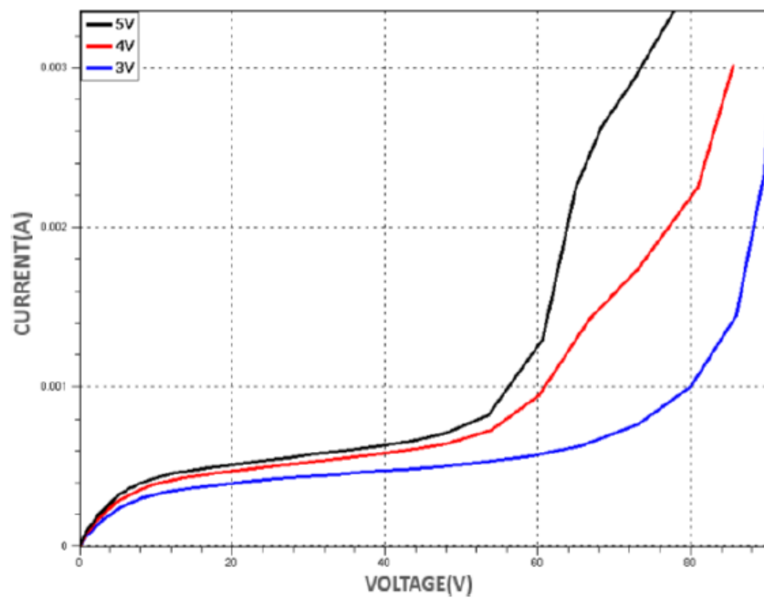

Fig. 1.6: Kirk effect in LDMOS, I_D-V_D [11]

Chapter 2

Possible modeling approaches

Modeling of a device allows to achieve better control and understanding its physical essence. It is vital for a model to be simple and at the same time mathematically derived from device physics. Besides, the output for a model should be compatible with the widest distributed software — SPICE for example.

The Lateral DMOS transistor is a device with a promising future for being compatible with standard CMOS technology and a high range of operations and working voltages. To meet the needs of industry, plenty of software vendors and research institutions are trying to present the most accurate and efficient approach to sustaining the characterization process for High-Voltage devices, and for LDMOS in particularly [12].

2.1 Overview of existing approaches

LDMOS models are presented as mathematical formulations, macro-models or sub-circuits and mixed forms [1, 12].

2.1.1 Macro model

Combination of MOSFET SPICE models with the addition of diodes and JFETs has been used to represent LDMOS behavior. This approach simplifies the structure of the device (especially the drift region), the thermal changes in outputs are not taken into consideration [12]. An example of such circuit for HV-DMOS model is given below.

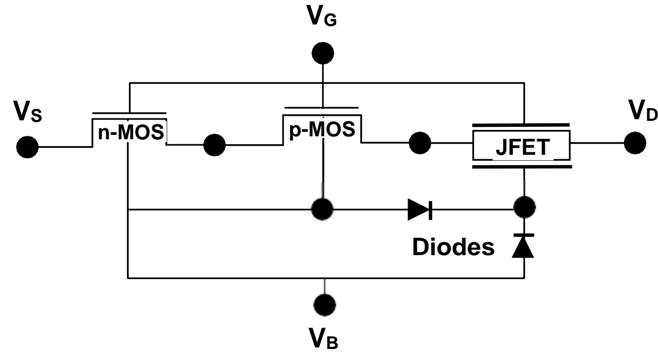

Fig. 2.1: Example of HV-DMOS macro model using SPICE circuit elements[12]

2.1.2 Lumped-Charge Model

Lumped-Charge methodology describes the device behavior using a set of physically based equations that calculate a total charge in specific regions as a basis. In a MOS structure, this approach works by "lumping" or in other words by discretizing charge distribution in accumulation, depletion, and inversion regimes. The resulting current is determined from terminal voltages and this distribution. The one set of equations is used regardless of the type of analysis. Process information, in this approach, represents the majority of model parameters.

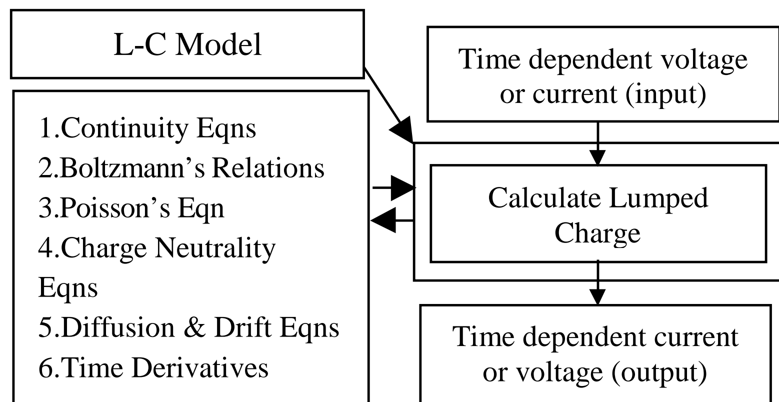

Fig. 2.2: The Lumped-Charge Methodology[13]

The limitation of the Lumped-charge approach is the implicit, simultaneous differential equations in the model require iteration. Thus simulators like SPICE can have problems with such a complex process.

LDMOS structure in this approach is divided into two MOS structures that are connected electrically. These are the Body Region MOS and the Drain Region MOS. For each of them, the L-C model is created [13].

2.1.3 EKV Model

EKV is a Verilog-based MOS transistor model. The abbreviation "EKV" stands for the names of its creators Enz-Krummenacher-Vittoz. Basically, that is a charge-based model designed for conventional MOSFET that uses an inversion charge rather than surface potential as the controlling physical mechanism [14].

There are also examples of an appliance of EKV model in HV-devices, or in VDMOS and LDMOS [12, 15]. The EKV team proclaims an improvement in the drift region and solving quasi-saturation issue and resolving self-heating challenge on the sub-circuit level. Moreover, the scalability and temperature parameters are being correctly reproduced. The following approach of the modeling LDMOS is to split the device structure into two significant regions and characterize them independently. So, the model is built on the combination of intrinsic MOSFET and the drift region [15].

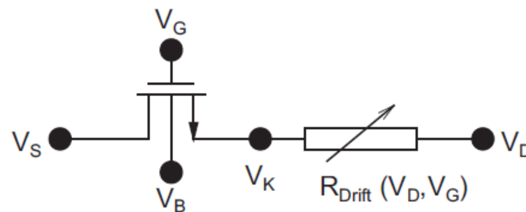

Fig. 2.3: EKV LDMOS modeling principle[2]

Major advantages of the EKV model are the following: a small number of parameters, which simplifies the intrinsic MOS calibration and easy-to-integrate modules like mathematical drift-expression [12]. The EKV model represents many physical effects and structure-related behaviors [14].

Recently the collaboration has been announced between BSIM and EKV group on development of the new BSIM6 as an open-source MOSFET SPICE model [16].

2.1.4 BSIM

BSIM (Berkeley Short-channel IGFET Model) is a physics-based MOSFET model developed at the University of California, Berkeley. Although sometimes physical parameters extracted in the model might yield values that are not consistent with their physical intent. It was founded for a low voltage MOSFET. The model has a great number of parameters, good accuracy, fast convergence and compatible with almost all known SPICE circuit simulators. Therefore it is widely accepted and supported.

History of BSIM started from the appearance of circuit simulators in 1970's, particularly SPICE1 at the Electronics Research Laboratory of the University of California, Berkeley. After that there was a strong need for accurate models. Thus in 1984 the first generation of submicron MOS transistor model was presented — BSIM1. Later in 1991 they released BSIM2 model. In 1994 U.C. Berkley introduced more physical modeling approach — BSIM3, whether later became the standard for semiconductor industry.

The actual version of the model is the fourth generation BSIM4. It addresses the physical effects in the sub-micron level [17, 18, 19].

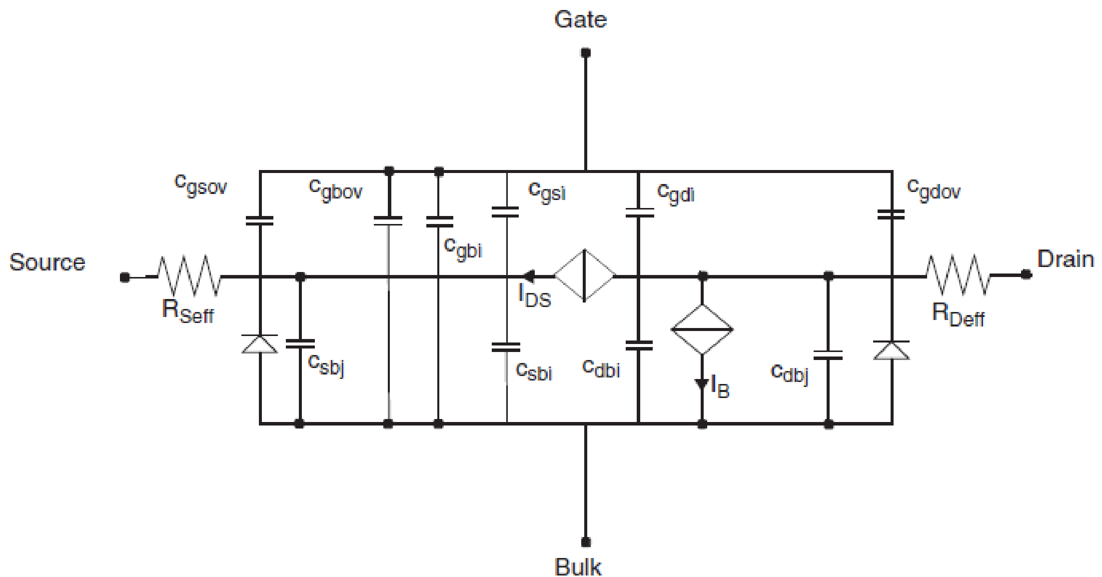

Fig. 2.4: BSIM4 Equivalent circuit [20]

The BSIM model will be used as a basis for modeling our devices

2.1.5 HISIM

HiSIM (Hiroshima-university STARC IGFET Model) is a surface-potential model for conventional bulk MOSFET. HiSIM-HV, which is an extension of the HiSIM basic model for high-voltage devices, adds the consistent potential extension to the drift region. Being represented by creators, HiSIM-HV can characterize the potential distribution in the entire asymmetric LDMOS or the symmetric HVMOS structures and determine all electrical and thermal high-voltage MOSFET properties without using macro- or sub-circuit formulation. Also, the scalability of this modeling approach may be done just with a single global parameter set.

The HiSIM core model for conventional bulk MOSFET implements the drift-diffusion theory and combines it into the form of a compact model for circuit simulator. HiSIM-HV also determines the potential distribution between a source and drain contacts by solving the Poisson equation iteratively. It includes the resistance effect in the drift region and considers the bias dependence of it [21]

2.2 BSIM parameters description

In this section, a review of the vital parameters for LDMOS BSIM4 model is given. The complete set of BSIM4 model parameters with its description is freely available at [18, 19].

Basic parameters

Model version, type of transistor whether it's P or N, channel width (w), channel length (l), electrical gate oxide thickness toxe.

Threshold and subthreshold parameters

Vth0 — Threshold voltage at zero V_{BS}.
k1,k2 — Body bias coefficients
k3 — Narrow width coefficient
k3b — Body effect on k3
lpe0,lpeb — Lateral non-uniform doping effects
dvt0, dvt1, dvtp0 — Coefficients of short-channel effects.
dvt0w, dvt1w — Coefficients for narrow width effect on threshold for small channel length
nfactor — Sub-threshold swing factor
lint — Channel length offset parameter

wint — Channel width offset parameter
dwg, dwb — Coefficients for gate/drain bias dependence of effective width
voff — Threshold voltage offset.
minv — Effective V_{GS}-Vth function fitting parameter for moderate inversion
vtl — Thermal velocity
vsat — Carrier saturation velocity at nominal temperature.
w0 — Narrow width effect parameter

Mobility parameters

MobMod — Mobility model selector, choosing involves several approaches to solving effective mobility equations.
U0 — Low-field surface mobility
Ua, Ub, Uc - Coefficients of mobility correction.

Saturation parameters

eta0 — Drain-induced barrier lowering coefficient in a sub-threshold region
keta — Body-bias coefficient of bulk charge effect
ags — Gate bias coefficient of the bulk charge effect
a0 — Bulk charge effect coefficient for channel length
a1, a2 — Non-saturation effect parameters.

Rout parameters

drout — Drain-induced barrier lowering effect on output resistance coefficient
alpha0 — Substrate current impact ionization coefficient
beta0 — Substrate current impact ionization exponent
pclm — Channel length modulation
pscbe1 pscbe2 — Substrate current induced body effect
pdiblc1 — Coefficient of drain-induced barrier lowering
dsub — Drain-induced barrier lowering effect in a sub-threshold region.
delta — Effective drain voltage smoothing

Drain-source resistance parameters

rdsw, — Zero bias lightly doped drain resistance per unit width
rdswmin — rdsw at high V_{GS}
prwg — Gate-effect coefficient for Rds
prwb — Body-bias coefficient for Rds

Charge and capacitance parameters

CGBO — Gate-to-body overlap capacitance per unit channel length.
CGSO — Source-gate overlap capacitance per unit channel width
CGDO — Drain-gate overlap capacitance per unit channel width
DLC — Channel-length offset parameter for CV model
DWC — Channel-width offset parameter for CV model
NOFF, VOFFCV — CV parameter describing the channel charge characteristics (V_{gsteff}) from sub-threshold to strong inversion.

Chapter 3

LDMOS DC model

In this chapter process of creating a DC compact model of LDMOS structure is presented. In such approach the device unity is preserved trough a set of self-consistent and continious expressions, which allows to predict and reproduce the specific device behaviour. Large amount of parameters is used to create accurate model in all regimes of operations: from weak to strong invesion, in linear and saturation region [12].

For the purpose of this project, an LDMOS transistor structure with fixed-length n-type channel has been chosen with work operational area up to 60 V. BSIM4 approach, which was described in the second chapter is used to create a I-V model.

The approximate cross-section of the tested device is represented in figure 3.1. The difference between one and that was stated in first chapter (1.2), is that the one has configuration of two gates, which are arranged symmetrically with respect to the drain. This structure, though, may have bigger amount of fingers, but that would not be considered in this work.

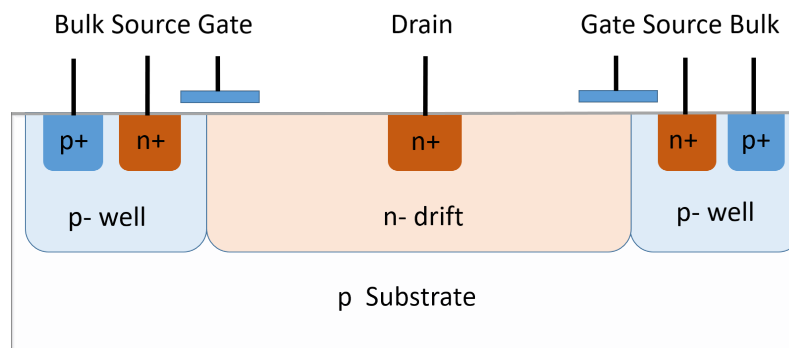

Fig. 3.1: Cross-section of chosen N-type LDMOS transistor

3.1 DC measurement

Measurements were held at the ON Semiconductor laboratory on Agilent 41501B semiconductor characterization probe. All of them were held at constant room temperature, 27 $°C$. It should be noted that the measuring device is sensitive up to the units of pA, thus measured data below $1 \cdot 10^{-12}$ A are considered as unreliable.

Shielded coaxial cables and protected from outer interference microscope were used for characterization measurement.

The die was chosen close to the wafer's center , thus it can have higher probability to be a ”golden” one. The main purpose of that procedure was to avoid abnormal or defective structure .

A simplified measurement diagram is shown in fig. 3.2. SMU stands for source measure unit and as follows from its name it can bias voltage and measure current depending on the test-case.

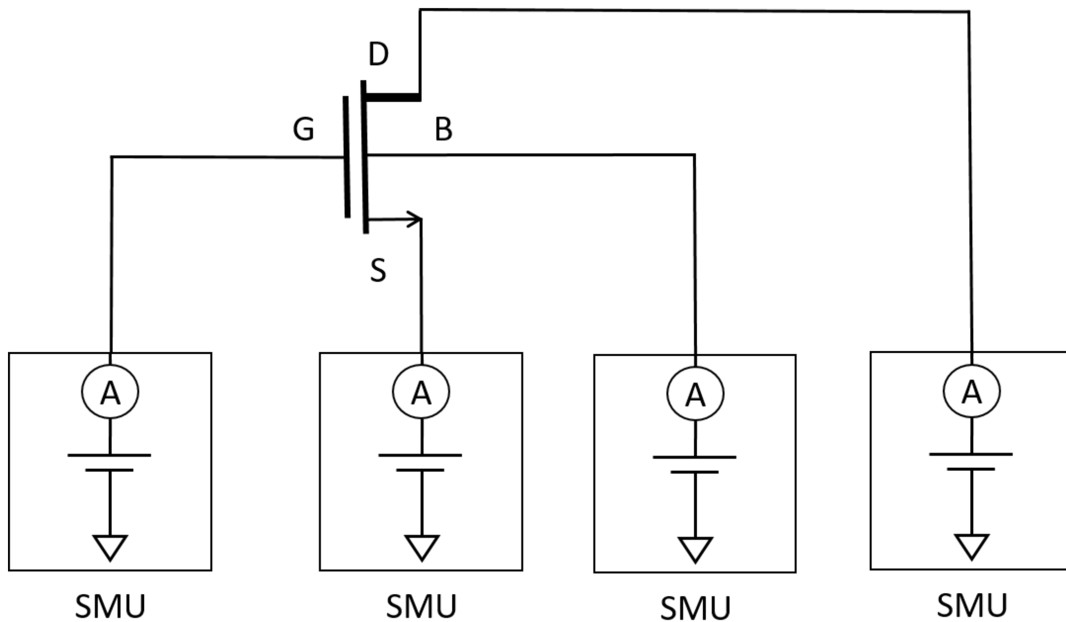

Fig. 3.2: Measurement concept of N-LDMOS

3.1.1 DC Tests

A brief description of applied I-V tests is written in this subsection.

I_D-V_G Low

The output of this test brings us a graph showing the dependence of drain current on gate voltage at low V_{DS}, which is usually described as transfer characteristics. This test is particularly important in a characterization of a MOS transistor. It is a starting point of fitting device characteristics, which affects all other behavior. Thereby the basis of threshold modeling and mobility parameters is built.

The derivative of the drain current with respect to the gate voltage as the result produces the graph of g_m dependence on the gate voltage.
Following biases have been used in the test

For constant $V_{DS} = 0{,}1$ V

V_{GS} linear swept from 0 to 3,6 V with 0,02 V step.

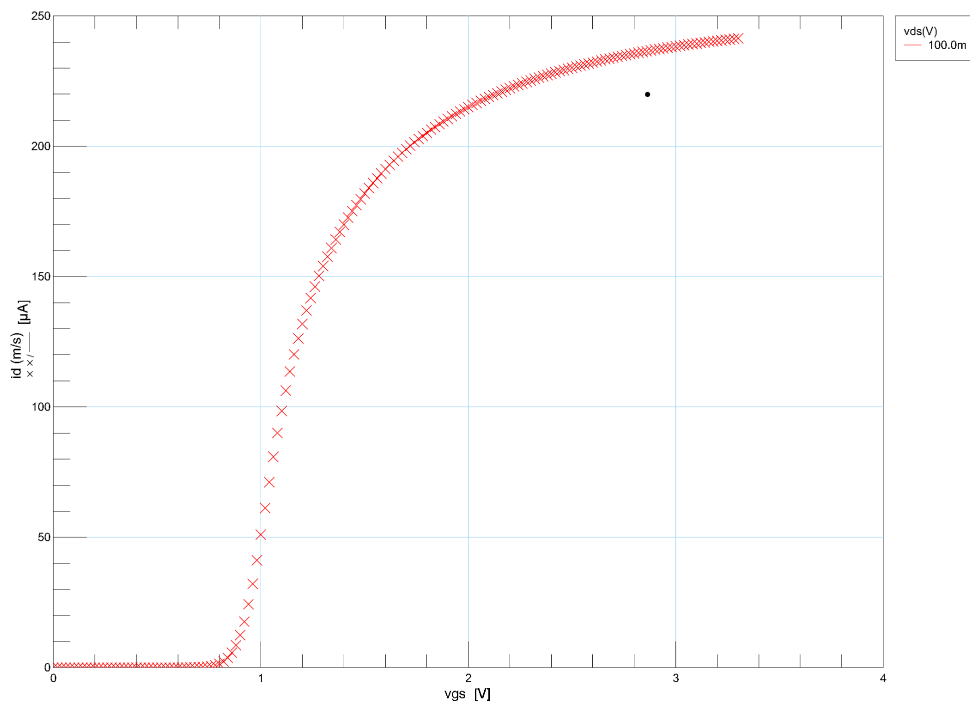

Fig. 3.3: I_D-V_G — transfer characteristics at low $V_{DS} = 0{,}1$ V

I_D-V_G High

The test output represents the dependence of drain current on higher gate voltages. It is an extension of previously mentioned test I_D-V_G low. The derivative of the drain current with respect to the gate voltage at several drain voltages as the result produces a graph of g_m dependence on the gate voltage.
Following biases have been used in the test

For several V_{DS}: 0,5; 1; 2; 5 V

V_{GS} linear swept from 0 to 3,6 V with 0,02 V step.

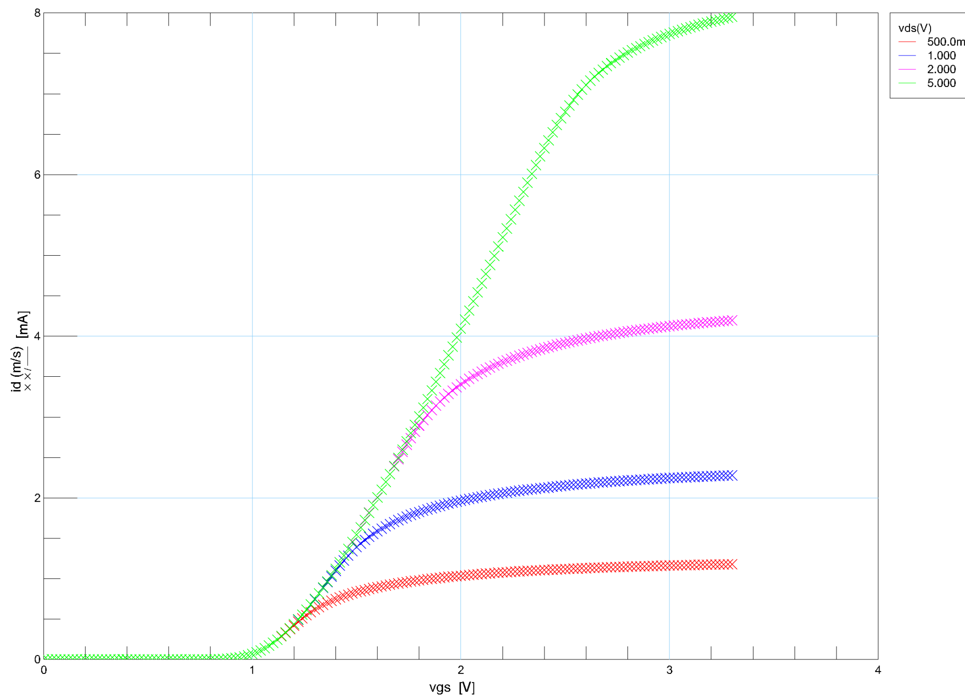

Fig. 3.4: I_D-V_G — transfer characteristics at higher V_{DS}

I_D-V_D Saturation

Dependence of a particular drain current for a particular drain voltage at a particular gate voltage also called output characteristics. The test is repeated for several V_{GS} biases. The derivative of the drain current regarding the drain voltage as the result produces the graph showing a dependence of output conductance on drain voltage, which will help us to fit output resistance.
Following biases have been used in the test

For several V_{GS} 0,9; 1; 1,1; 1,2; 1,3; 1,4; 1,5 V

V_{DS} linear swept from 0 to 35 V with 0,5 V step.

I_D-V_D Linear region

Linear region is an important part of the output characteristics curve. Because of precise requirements in the switching applications, this area should be very well fitted.
Following biases have been used in the test

For several V_{GS} : from 1 to 3 V with 0,2 V step

V_{DS} linear swept from 0 to 3 V with 0,05 V step.

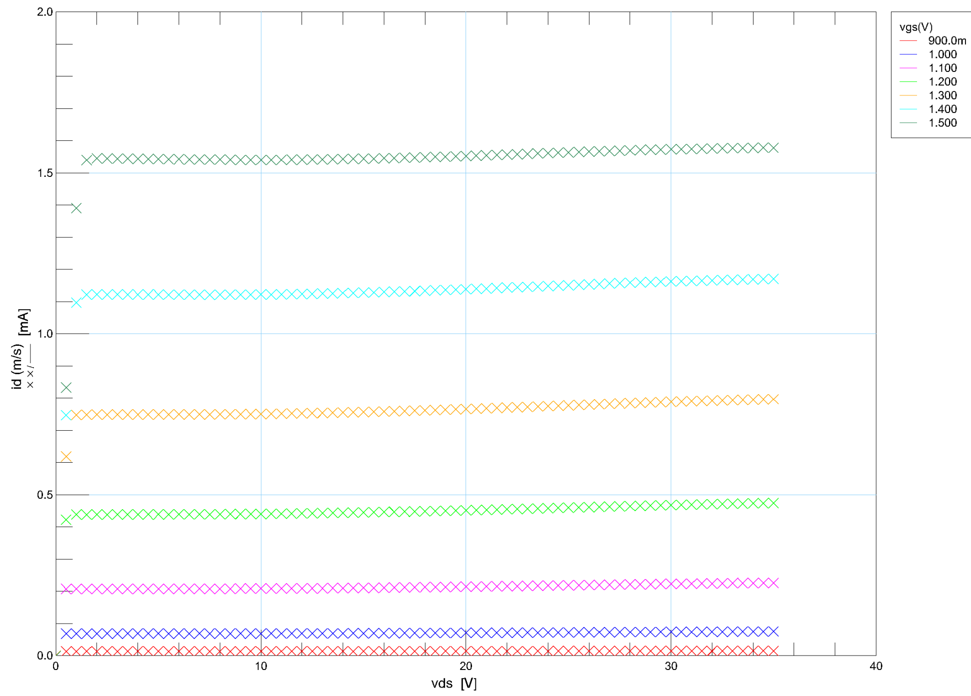

Fig. 3.5: Output characteristics measured data — I_D-V_D Saturation

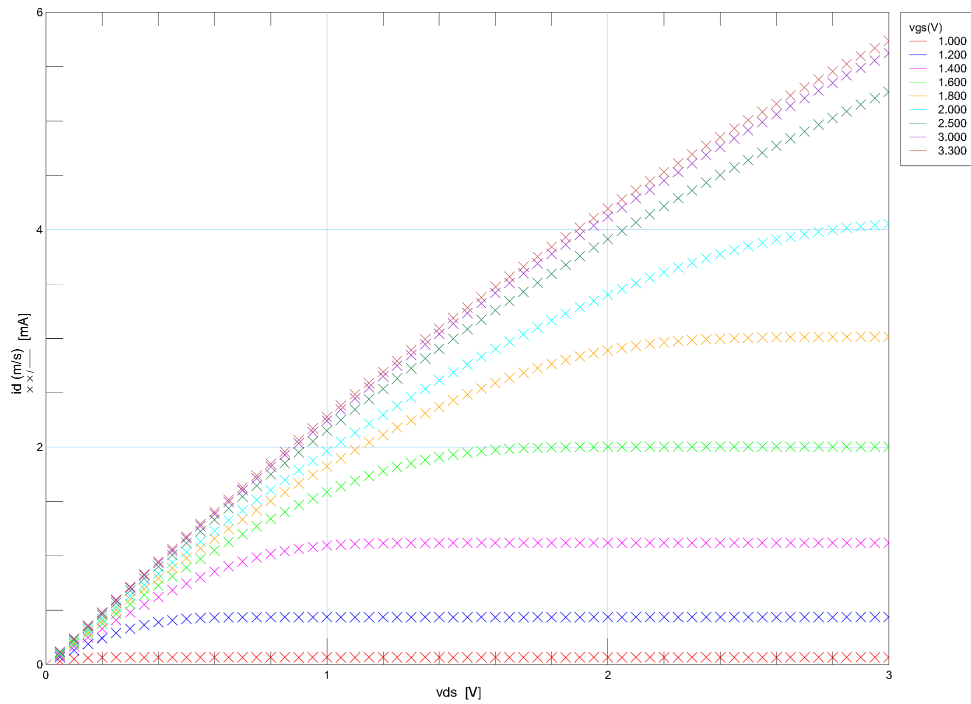

Fig. 3.6: Output characteristics measured data in linear region — I_D-V_D linear

3.2 DC parameters extraction

The process of extraction starts with an overview of technological parameters. It is necessary to know the device architecture, oxide thickness, the number of gates NG, type of channel and geometries: Wg and Lg. After that, we can proceed to the next fundamental step in building a model. A bare BSIM4 model just with technological parameters is shown in figure 3.7. Measured data are represented as squares or cross-shaped points, simulated data as a bold line; thus it will be thereon if otherwise is not stated.

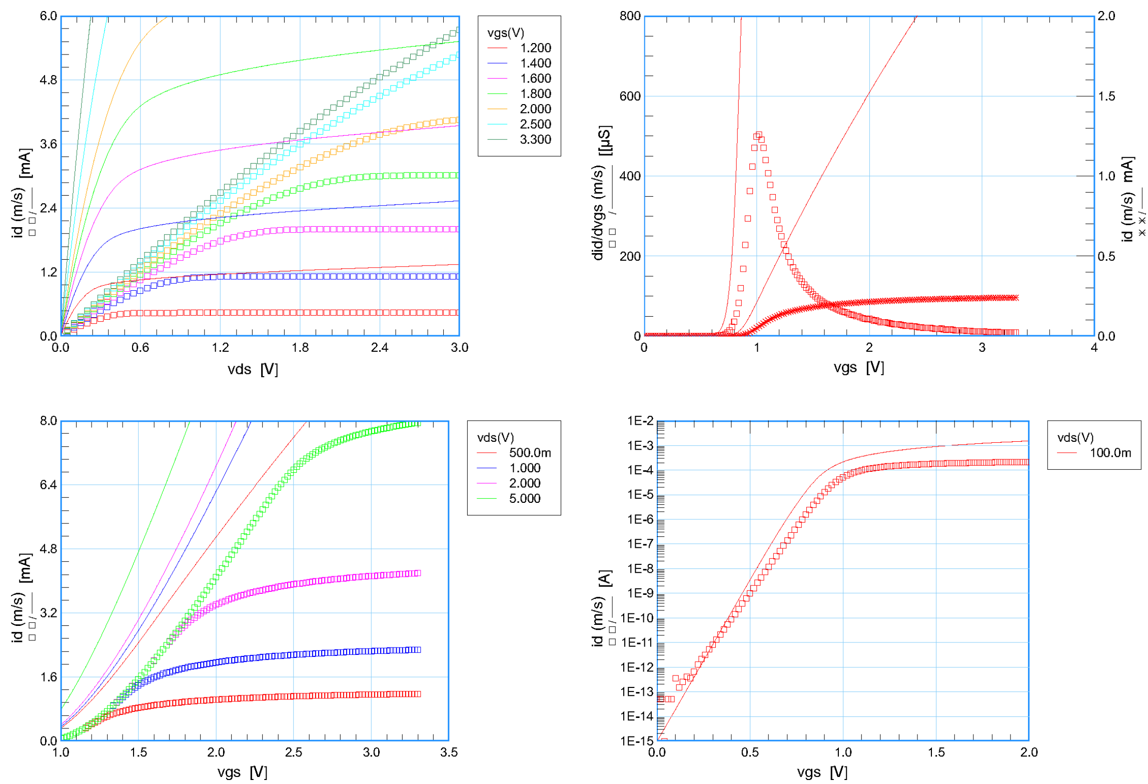

Fig. 3.7: BSIM4 model, basic parameters only

3.2.1 Transfer characteristic tuning on low Drain-Source Voltage

The starting point of the modeling process is to tune the transfer characteristics on low V_{DS}. Hereon the particular gate voltage is 0,1 V. The best we will fit this characteristic, the better responce will we get on the others.

Threshold and Mobility fitting

The basic parameter for the start of tuning is Vth0. The best feedback upon tuning of the parameter will be received on this transfer characteristics with drain current in logarithmic scale. After the threshold is tuned with Vth0, mobility parameters are taking place. U0 and Ua will form the shape of g_m-V_G graph. U0 moves the peak level of this graph while ua corrects a level of peak and its lowering part.

Rdsw and N-factor fitting

After having mobility and threshold fitted we can proceed to drain resistance and N-factor fitting. Changing of N-factor will adjust the angle of the rising slope of a transfer function in logarithmic scale, along with that we can see changes in the position of the g_m-VGS peak. Rdsw is used to push down the whole characteristics and it has a major impact on the position of the g_m-V_G tail.

Body-effect modeling

Body effect is the last step of fitting the transfer characteristics on low V_{DS}. Best responce could be achieved if we focus on g_m-V_G and I_D-V_G in logarithmic scale. First will help to adjust mobility peaks, for their growth trend with higher bulk voltage correction parameter Uc is used, and second will let us adjust the threshold changes via k3b. The total look of these curves depends on previous modeling steps.

Complet body-effect model vs measured data is presented in figure 3.2.1.

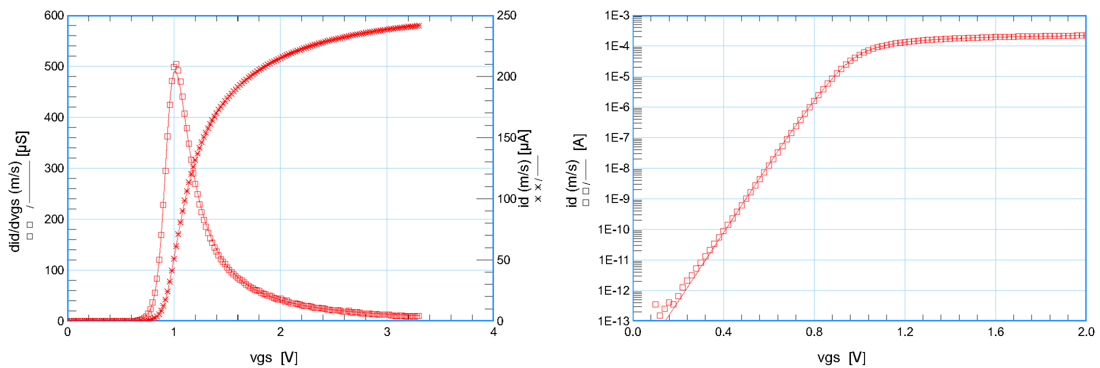

Fig. 3.8: Fitted transfer characteristics on low V_{DS}

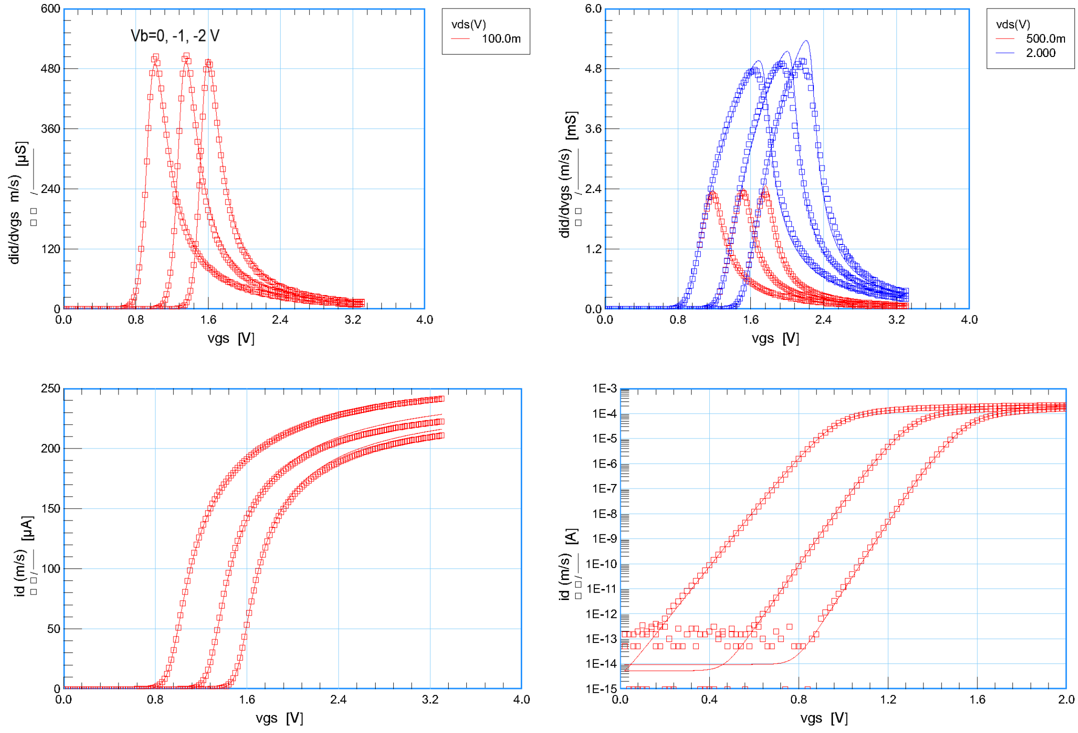

Fig. 3.9: Body effect modeled on I_D-V_G-Low

3.2.2 Fitting the output characteristics

After complete and tuned transfer characteristic on low VDS we to focus attention at the output characteristics of the N-LDMOS. Fitted I_D-V_G on low VDS is not enough for the accurate I_D-V_D.

For tuning of I_D-V_D, both linear and saturation region, we have used parameters such as a0, ags, a1, a2. They are defining levels of each drain current, in dependence on a particular gate voltage. To offset the all the curves Vsat has been used. As well we have had to remove the rising tale of the output characteristics, a sign of impact ionization in conventional MOSFET.

As well with that PCLM (*channel length modulation*), PDIBL (*drain-induced barrier lowering*) and SCBE (*substrate current induced body-effect*) parameters were used to improve the saturation curve accuracy. The working area of each parameter type is shown in figure 3.10.

3.2.3 Fitting the transfer characteristics and transconductivity

Parameters that were used to fit the output characteristics have made an impact on the look of transfer characteristics on higher drain voltages. The rising slope of g_m-V_G characteristics was over-linearized and peaks were too uplifted. But at the

same time, those changes had not such an impact on I_D-V_G. Hence mobility fitting on higher gate voltages should be very careful if we are not to destroy the I_D-V_G low appearance.

Fitting the transfer was the most complex step of DC model. It included tuning of the sub-threshold (K1 and K2), mobility, drain-resistance, short channel effect (DVT0, LPE0), MINV, Voff, and Nfactor parameters. To create the best fit in g_m-V_G and I_D-V_G characteristics on higher drain voltages a compromise with low I_D-V_G has been made. And because of changes into the sub-threshold region, we must have observed a threshold on the logarithmic graph of I_D-V_G and tune it as well.

3.2.4 R$_{out}$ and R$_{DSon}$ fitting

The output resistance of the device was fitted on the output conductivity graph, which is the byproduct of I_D-V_D derivation. The main purpose was to fit Rout behavior on lower gate voltages. Difficulty lies in representing the changing "knee" correctly on the graph and the levels of its constant saturation behavior.

For those purposes, we have used PCLM, PSCBE, dsub, pdits, pdiblc1, delta, and pvag. Good fit of Rout behavior made output characteristics(I_D-V_D saturation) and On-resistance look better as well.

However, the R_{DSon} was not only adjusted with mentioned parameters, but with triode parameters as well, which are U0, Ua, Ub mobilities and resistances Rdw, prwg, prwb. At the same time this interference made an impact on I_D-V_G low characteristic appearance. Therefore counterbalancing the effects of triode parameters was necessary.

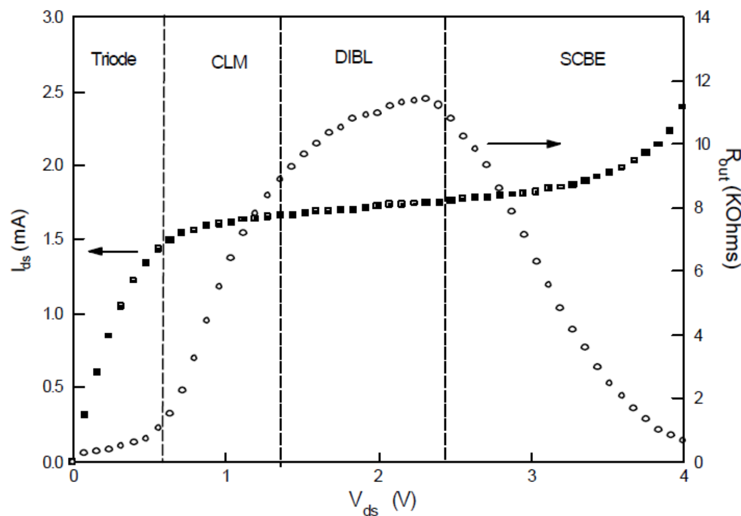

Fig. 3.10: Indication of BSIM parameters use for I_D-V_D and R_{out} fitting [19]

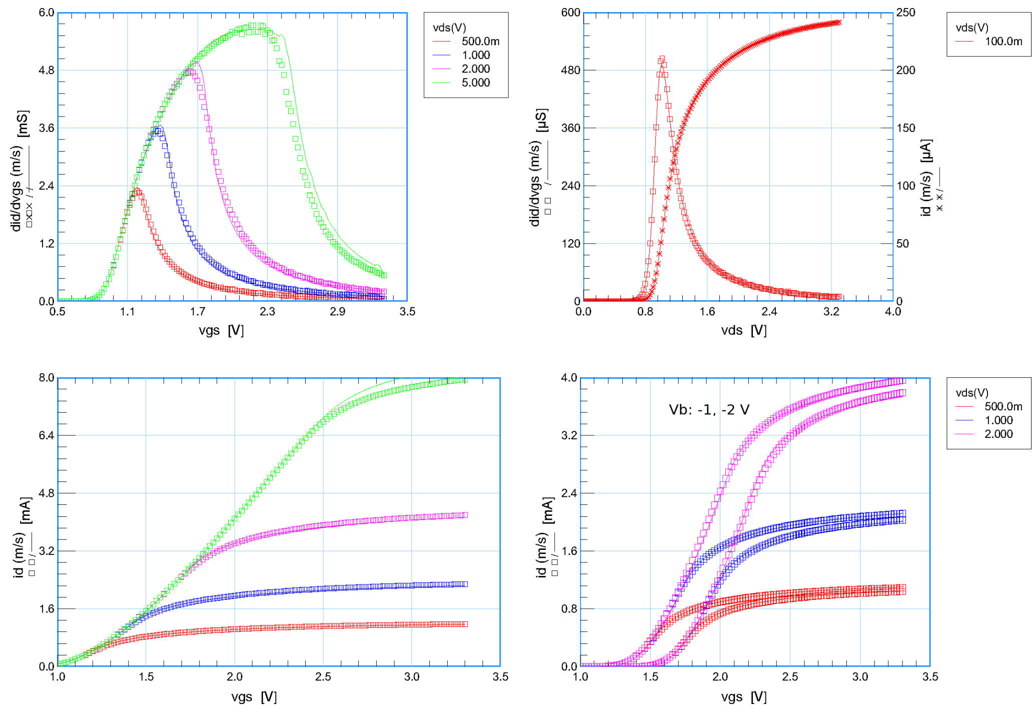

Fig. 3.11: Fitted I_D-V_G

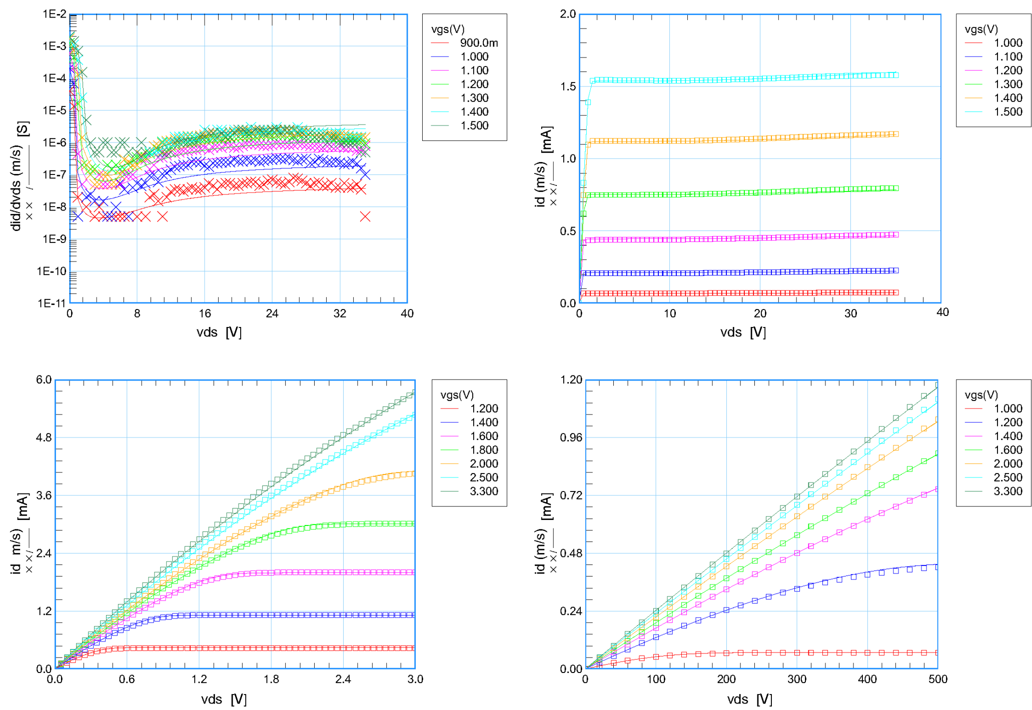

Fig. 3.12: Output conductance and I_D-V_D fitted

3.3 Scaling of the DC model

Device width has a significant effect on the device characteristics. The characteristics of a MOS transistor change with the device dimensions reduced. LDMOS as well as MOSFET characteristics degrade with the reduction in its physical dimension. Main changes are applied to threshold voltage and subthreshold swing. Threshold voltage decreases and subthreshold swing increases because of two-dimensional electrostatic charge sharing between the gate and the source-drain regions [22].

In particular N-LDMOS the channel length remained constant and the only changing parameter was width. Thus four different geometries with channel width of 3, 5, 10 and 20 μm were used for characterization of the DC model scaling.

The following figures (3.13, 3.14, 3.15) provide scaled characteristics of the DC model from previous step.

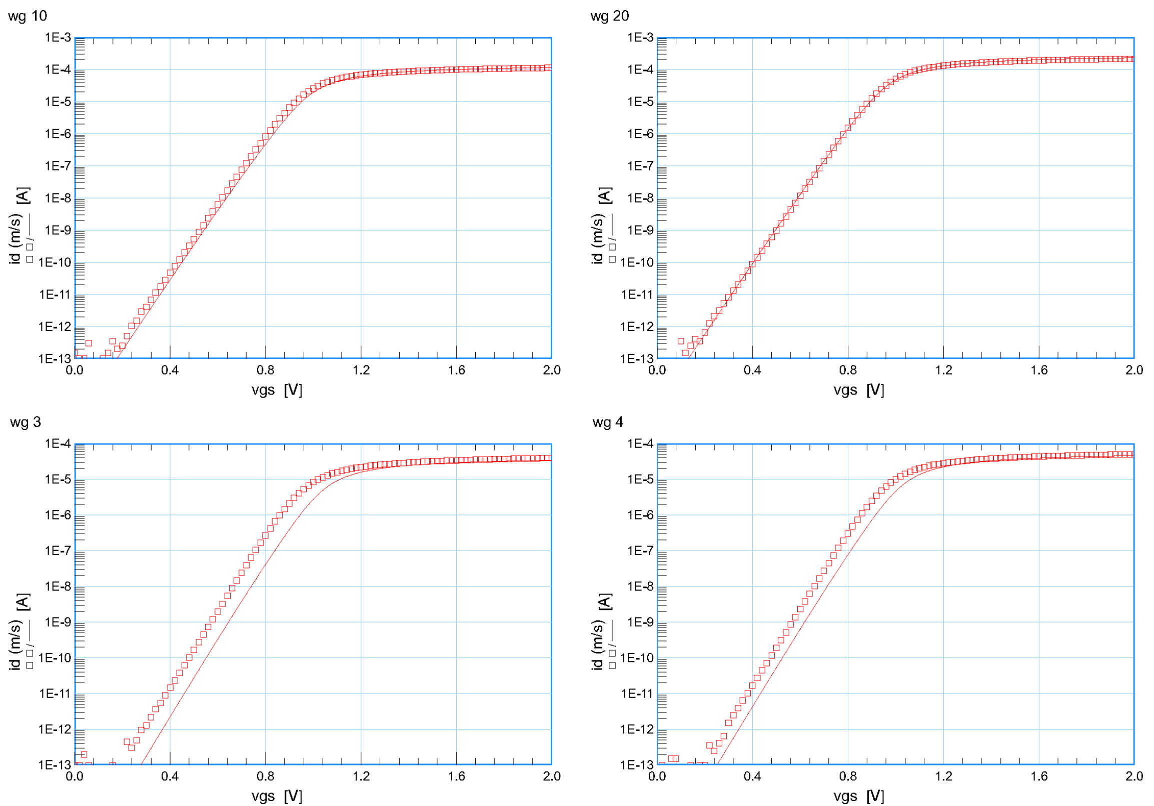

Fig. 3.13: Threshold shift due to the channel width change

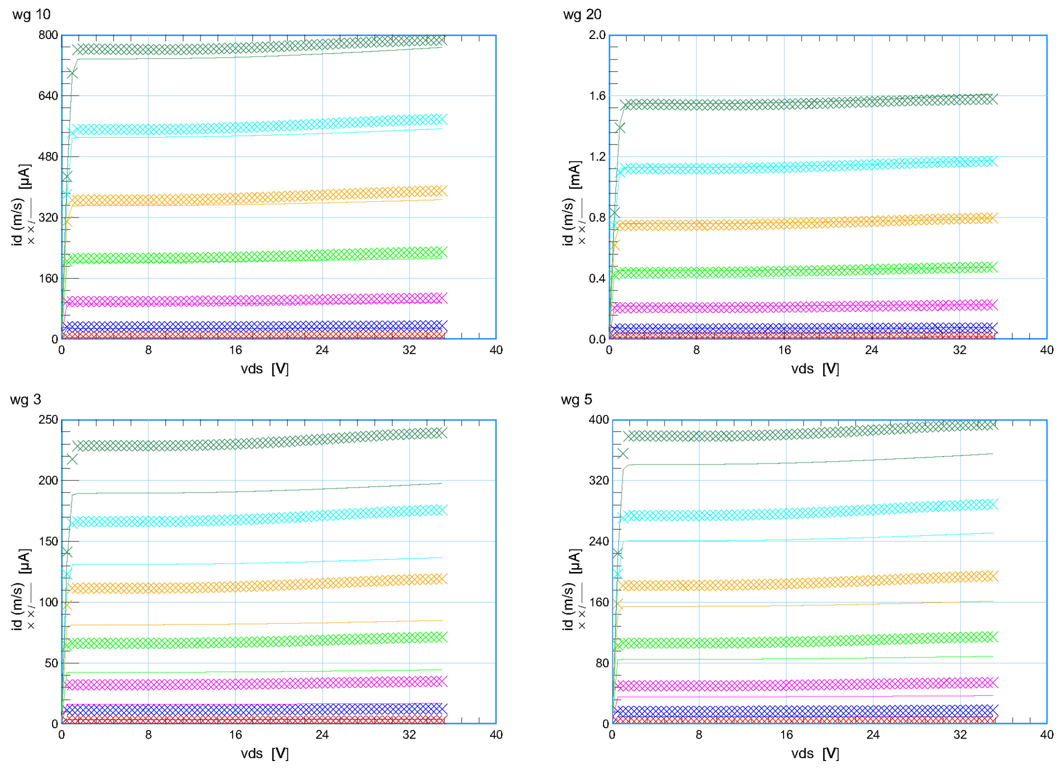

Fig. 3.14: Channel width change impact on I_D-V_D *Saturation*

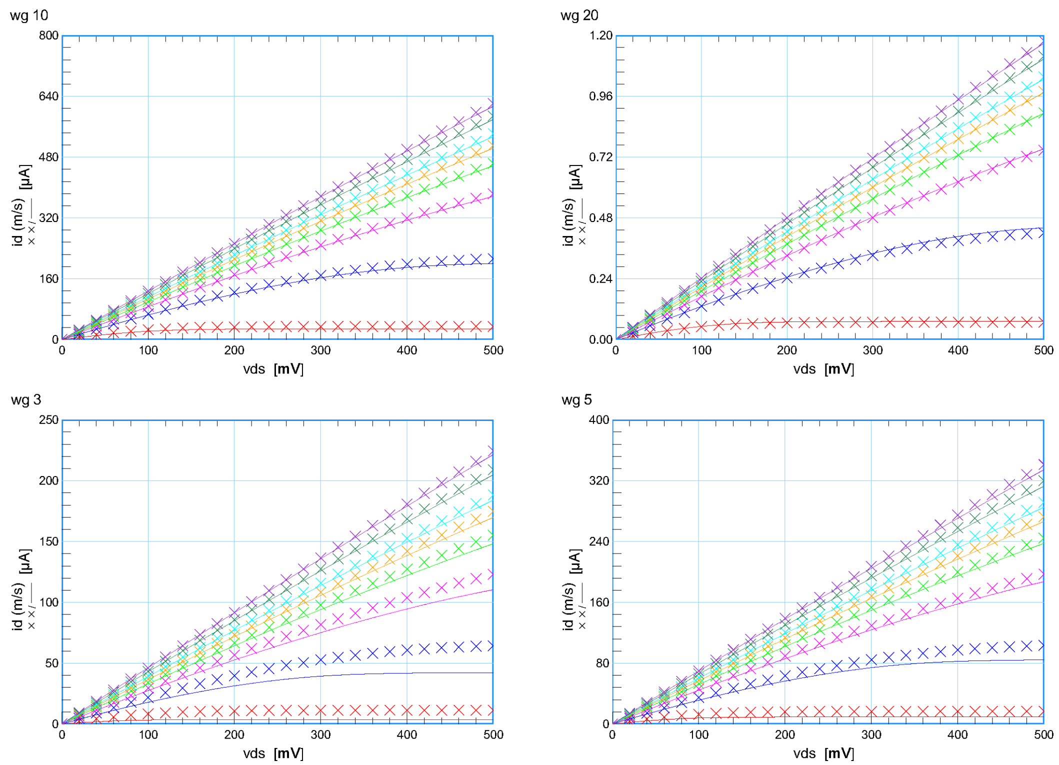

Fig. 3.15: Channel width change impact on R_{DSON}

3.3.1 Modeling of the narrow width effect on threshold

On the other hand it has been found that threshold voltage increases as the channel width decreases. The "normal" narrow width effect is explained by the contribution of charges in the depletion layer region or in the edge of the field implant region. With the decreasing width of the device, these charges have bigger impact so the total depletion region charge becomes greater, which leads to an Vth increase.

BSIM approach has several tools to represent this Vth shift due to change of width and takes an empirical approach to account for the overall narrow width effects (both normal and reverse narrow width effects). These are special parameters for channel geometry change and binning parameters with prefix w. Almost every BSIM parameter has its w or l scaling counterpart. However their utilization was unnecessary in our case.

Three fitting parameters K3, K3B, and W0 are used in model to scale Vth. For small channel lengths, which is the natural case of LDMOS, BSIM introduces addition parameters: DVT0W, DVT1W and DVT2W which are extracted from experimental data [7].

3.3.2 Width-dependency in the drift resistance implementation

The next possible option how to improve characteristics on different geometries is to implement width dependency into the outer R_{drift} equation. After having fitted threshold voltage shift, drain resistance is the key to the rest of the characteristics. As it can be seen in fig. 3.15 simulated R_{DSON} is higher for smaller W_g, thus its impact should be reduced on smaller structures.

For that implementation RDSW parameter from previous section is used. The following equation was implemented. As channel width decreases the drain resistance is less susceptible to increase.

$$R_{DSWext} = \frac{R_{DSW}}{W_g - \ correction} \tag{3.1}$$

Following figures (3.16, 3.17, 3.18, 3.19) display the results of a DC model scaling.

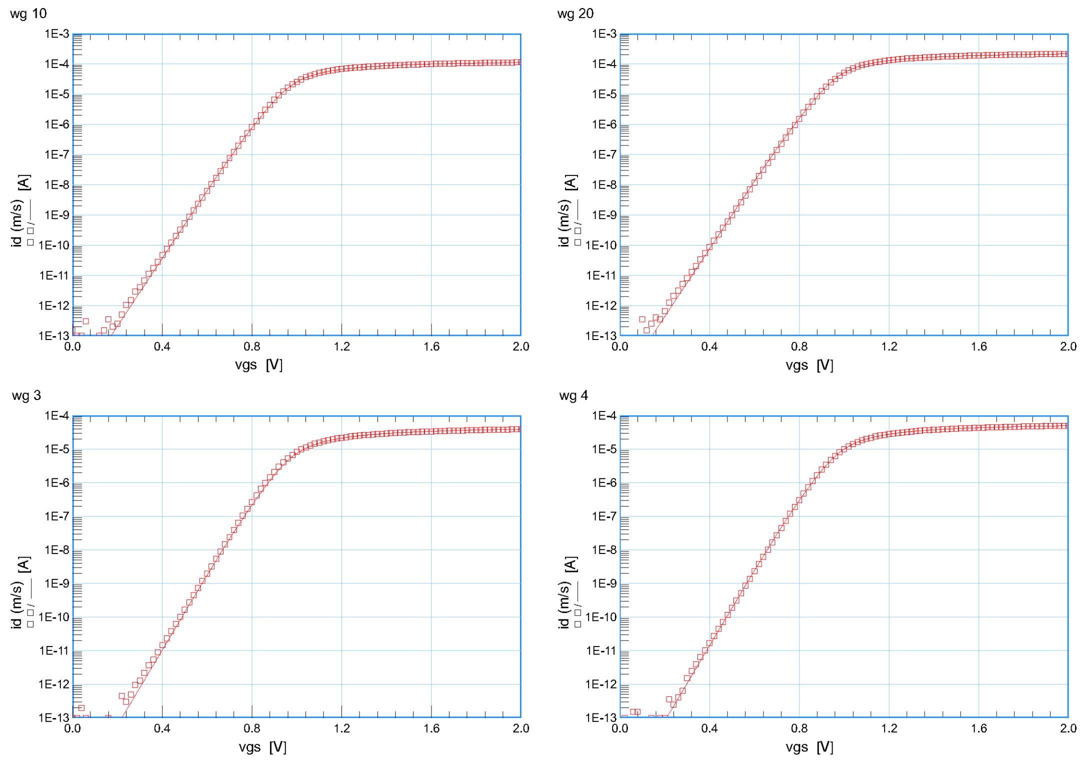

Fig. 3.16: Threshold model including scaling parameters

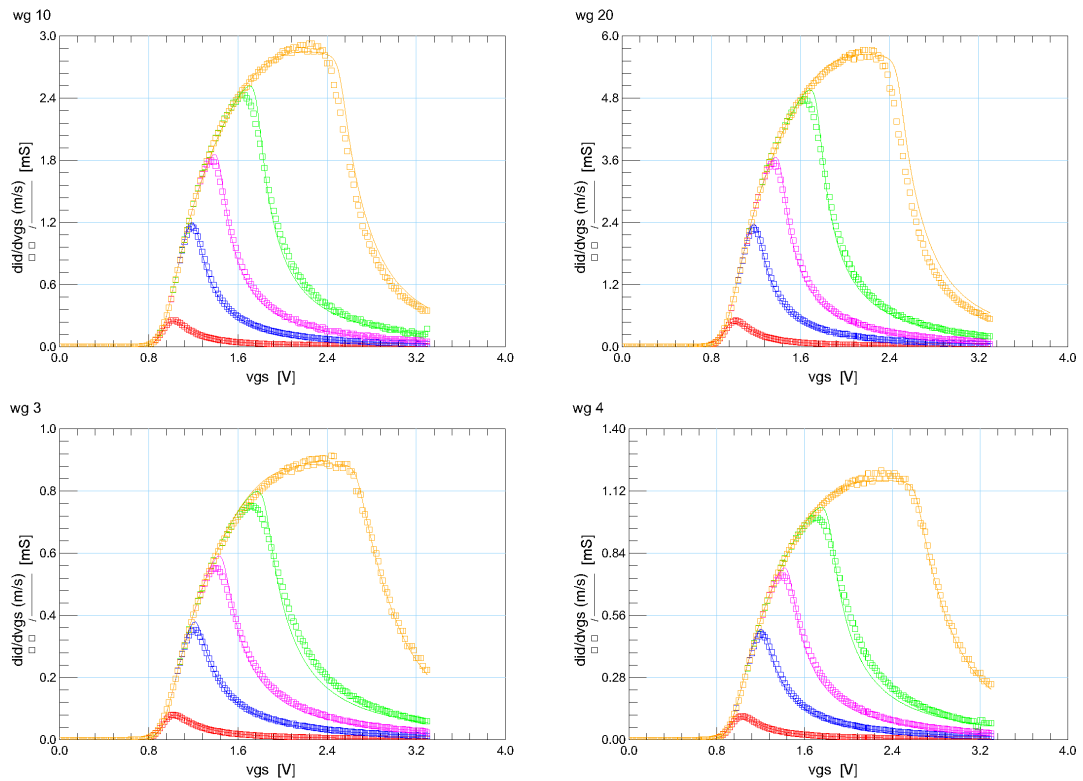

Fig. 3.17: g_M-V_G high model with implemented scaling parameters

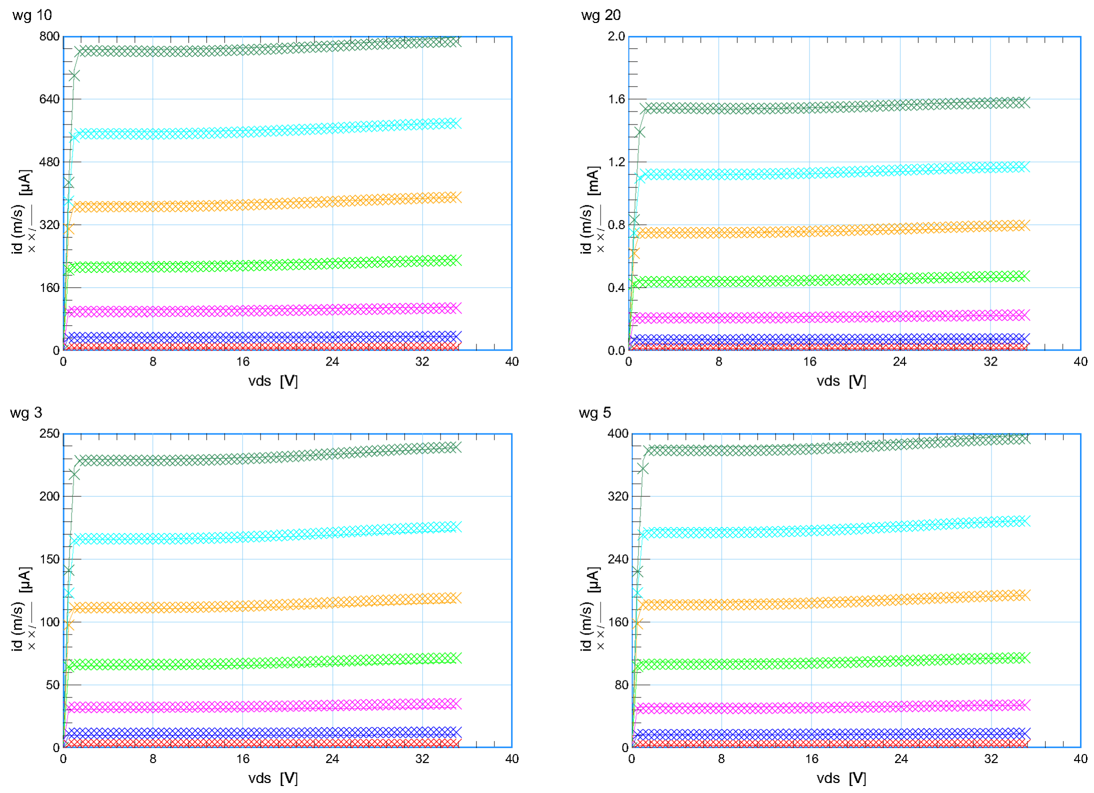

Fig. 3.18: I_D-V_D *Saturation* with implemented scaling parameters

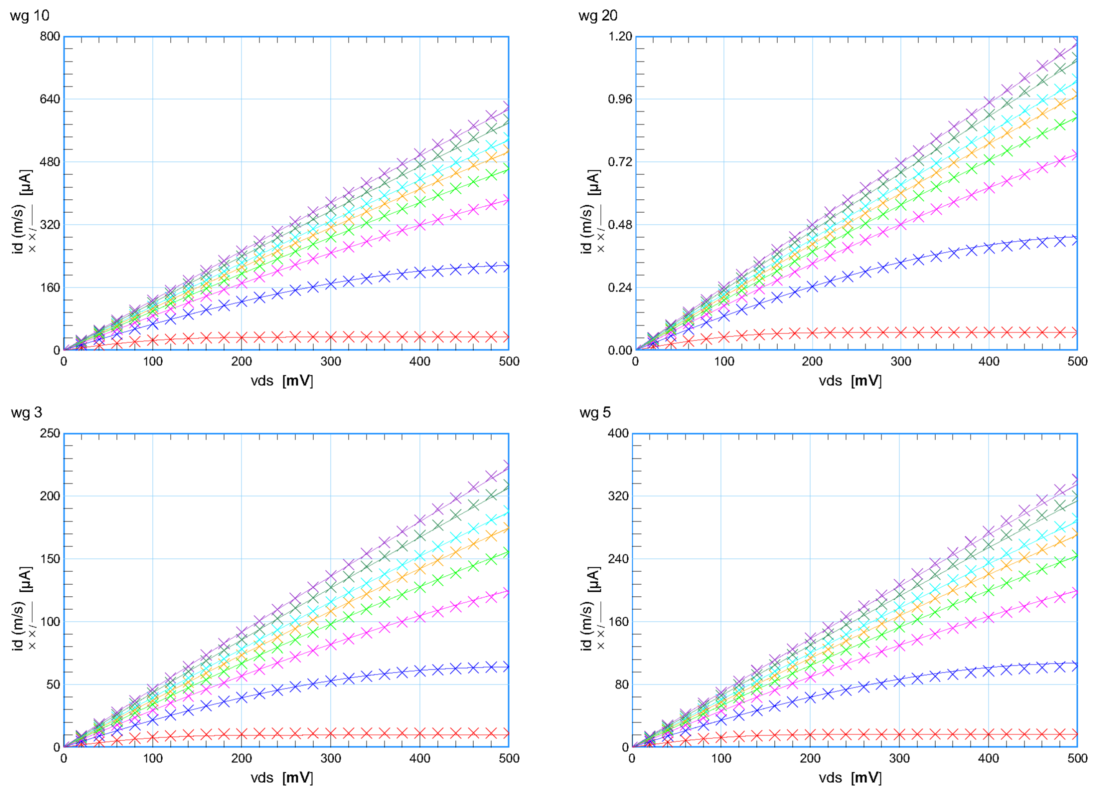

Fig. 3.19: R_{DSON} with implemented width scaling parameters

3.4 Result

The result model parameters based on all previous steps are stated in table 3.1. The RMS error of simulated model versus measured data:

of output characteristics is 12 %,
of On-Resistance is $\leq$ 1 %,
of transfer characteristics on higher V_{DS} is 13 %,
of I_D-V_G low is 1,4 %.

Parameter	Value	Parameter	Value	Parameter	Value
vth0	0,88	wint	$5 \cdot 10^{-8}$	dsub	0,25
k1	0,86	keta	-0,02	minv	$35 \cdot 10^{-4}$
k2	-0,025	vsat	$2,6 \cdot 10^{6}$	pclm	1,736
k3	10	u0	0,0366	pdiblc1	$1,2 \cdot 10^{-8}$
k3b	14	ua	$36,89 \cdot 10^{-16}$	pdiblc2	$4,5 \cdot 10^{-6}$
w0	$1,25 \cdot 10^{-5}$	uc	$5 \cdot 10^{-16}$	drout	$5 \cdot 10^{-3}$
lpeb	$1,87 \cdot 10^{-8}$	eu	1,701	pscbe1	$6,1 \cdot 10^{10}$
dvt0	$2 \cdot 10^{-2}$	nfactor	1,8	pscbe2	$4,1 \cdot 10^{-5}$
dvt1	$6 \cdot 10^{-2}$	a0	-0,13	delta	0,01
dvt2	-0,1	ags	-0,5	pdits	$1 \cdot 10^{-3}$
dvtp0	$2 \cdot 10^{-7}$	vtl	$5,6 \cdot 10^{4}$	rdw	$10,3 \cdot 10^{3}$
dvt1w	6,124	voff	-0,123	prwg	0,05
dvt2w	-0,029	dwg	$-1 \cdot 10^{-7}$	prwb	-0,028
lint	$7,5 \cdot 10^{-8}$	dwb	$1,4 \cdot 10^{-7}$	alpha0	$1,46 \cdot 10^{-9}$

Tab. 3.1: Optimized set of BSIM4 parameters for N-LDMOS DC model

Chapter 4

Capacitance model

In previous chapters we have discussed DC model approaches and characteristics. However real circuit applications of an LDMOS might be dealing with time-varying voltages and currents. Incoming alternating, pulsating or variable signal is affected by device's capacitance, and thus, the output is a result of this capacitive effect.

Capacitance of LDMOS is an important parameter, which influences the input and output of an enclosed device, has significant impact on high frequency performance and switching applications. [23].

Parasitic capacitance is formed due to the overlapping of different layers in semiconductor device during fabrication [6].

Capacitance models of high-voltage devices are made of two parts. First is large signal charge-based model, which is BSIM in our case, and second is equivalent circuit for small signal operation, representing layout of the device [12].

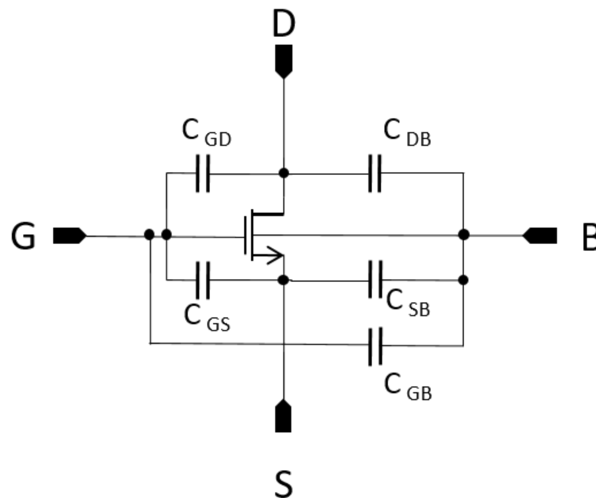

Fig. 4.1: LDMOS capacitances

4.1 Measurement of CV characteristics

Measurements were made at the ON semiconductor laboratory on precision LCR-meter Agilent E4980A. Following scheme in fig. 4.1 represents 4-wire capacitance measurement of the device. H and L stands for HIGH and LOW test terminals; more specificly: H_{CUR} — High current, H_{POT} — High potential, L_{POT} — Low potential, L_{CUR} — Low current; DUT stands for device under test.

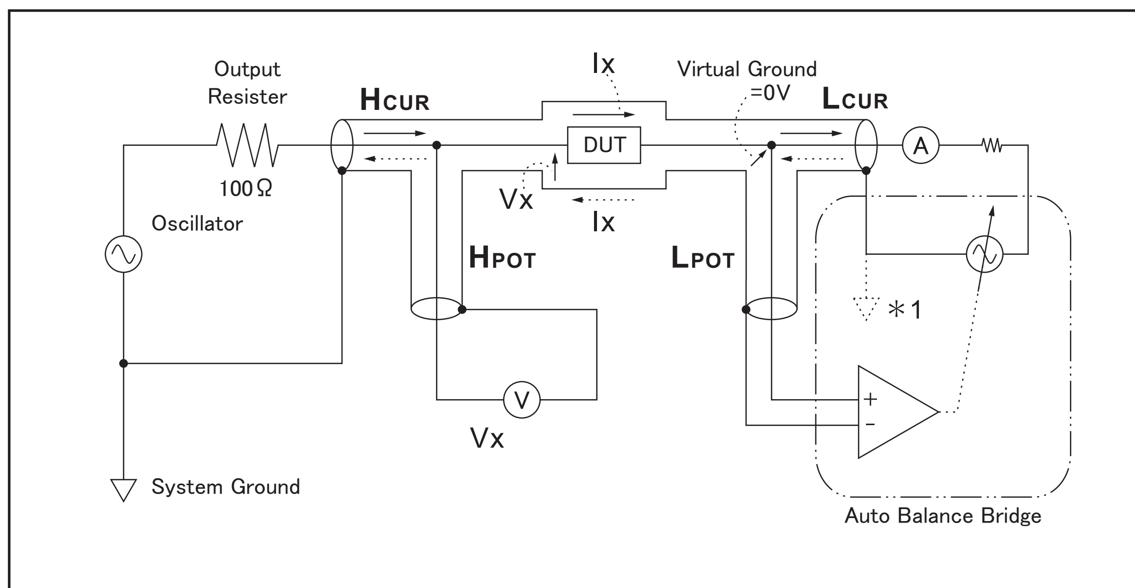

Fig. 4.2: Four-terminal pair capacitance measurement principle [24]

The following sections contain short description of the measured Capacitance-Voltage characteristics, their graphs and connection diagrams.

4.1.1 Gate oxide capacitance measurement

For the CV tests related with this chapter, which are stated in this part, the same bias was used:

Vg sweep from -3,6 to 3,6 V with 0,1 V step.

AC signal properties: frequency 100 kHz, amplitude 0,05 V.

Gate Drain

Cgd is called the feedback capacitance or the reverse transfer capacitance, which is created between the gate and the drain region. This parameter greatly affects switching speed, and the effect of the capacitance is amplified by the transistor gain, therefore an accurate model is essential.

High test terminal is connected to the gate and low to the drain.

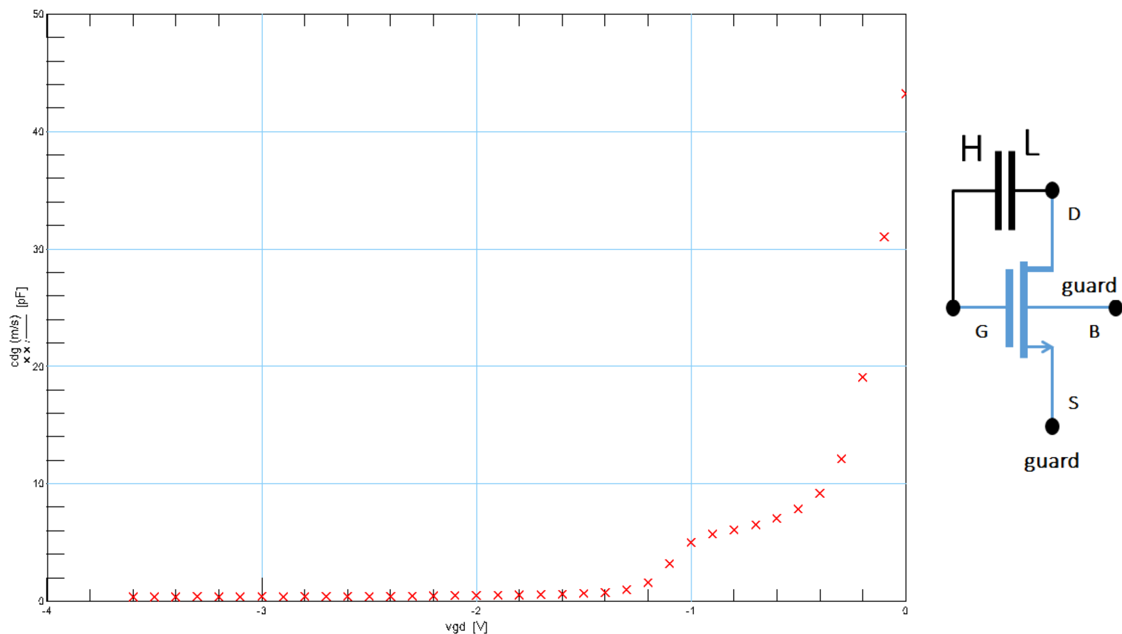

Fig. 4.3: Gate-Drain capacitance versus V_G and measurement diagram

Gate Drain Source

Cgds is the capacitance between gate and drain-source region. Extension of previous measurement in which the drain and the source terminals are shorted to each other. Source part of this capacitance represents the inversion region of total CV LDMOS profiling.

Gate Bulk

C_{GB} is bulk versus gate capacitance, represents accumulation region. It is to be expected that C_{GB} is zero in strong inversion since the inversion layer in the channel from the drain to the source shields the gate from the bulk and prevents any response of the gate charge to a change in the substrate bias, V_{BS}. This is approximately true in the strong inversion case. However, C_{GB} can not be considered zero in the weak inversion and accumulation regions [7].

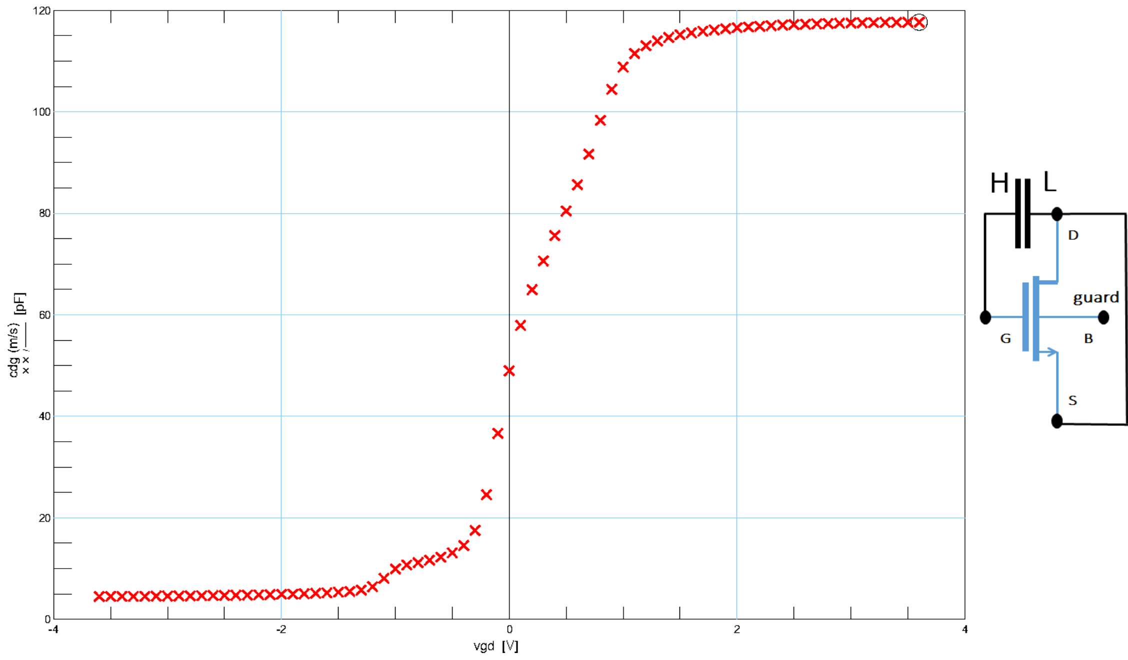

Fig. 4.4: Gate-Drain Source capacitance versus V_{GD} and measurement diagram

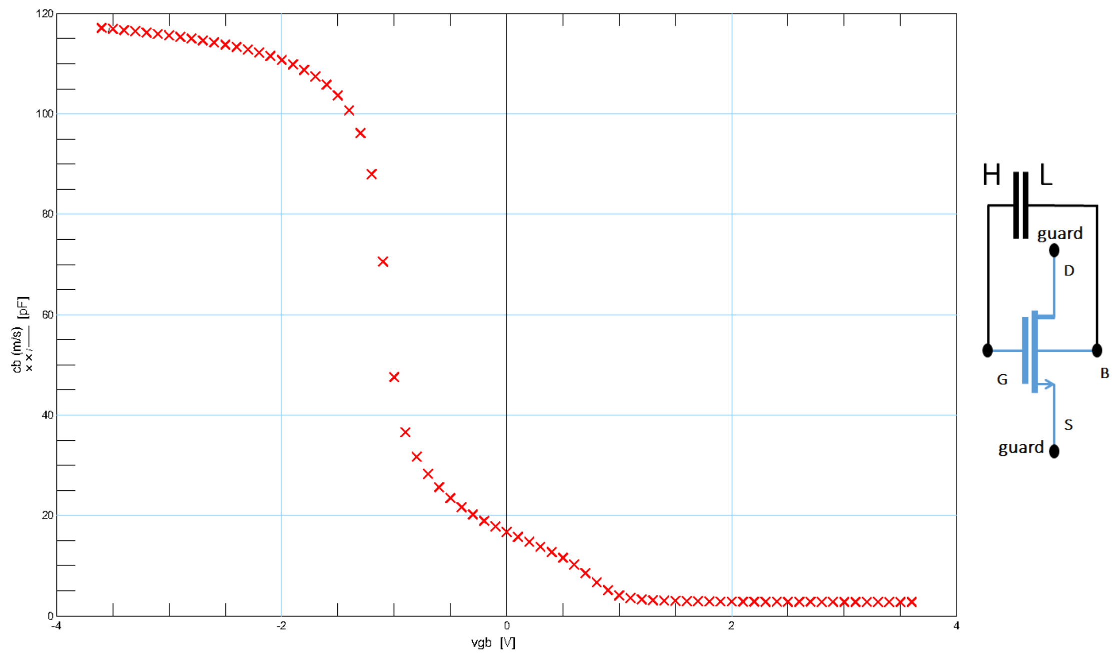

Fig. 4.5: Gate-Bulk capacitance versus V_G and measurement scheme

Gate versus Drain-Bulk-Source

Total gate capacitance versus gate voltage from accumulation through strong inversion regions. It is also called the quasi-static C-V characteristic. This characteristic mainly depends on gate oxide thickness.

For less noise and better quality of the output graph the bias polarity was reverted, thus C_{GDSB} became C_{DSBG}, as the result of that characteristics is flipped vertically. The validity of this statement was observed empirically, insofar as data measured the first way were blurred by noise and unusable. In the test drain, bulk and source are shorted and biased from -3,6 to 3,6 V with 0,1 V step.

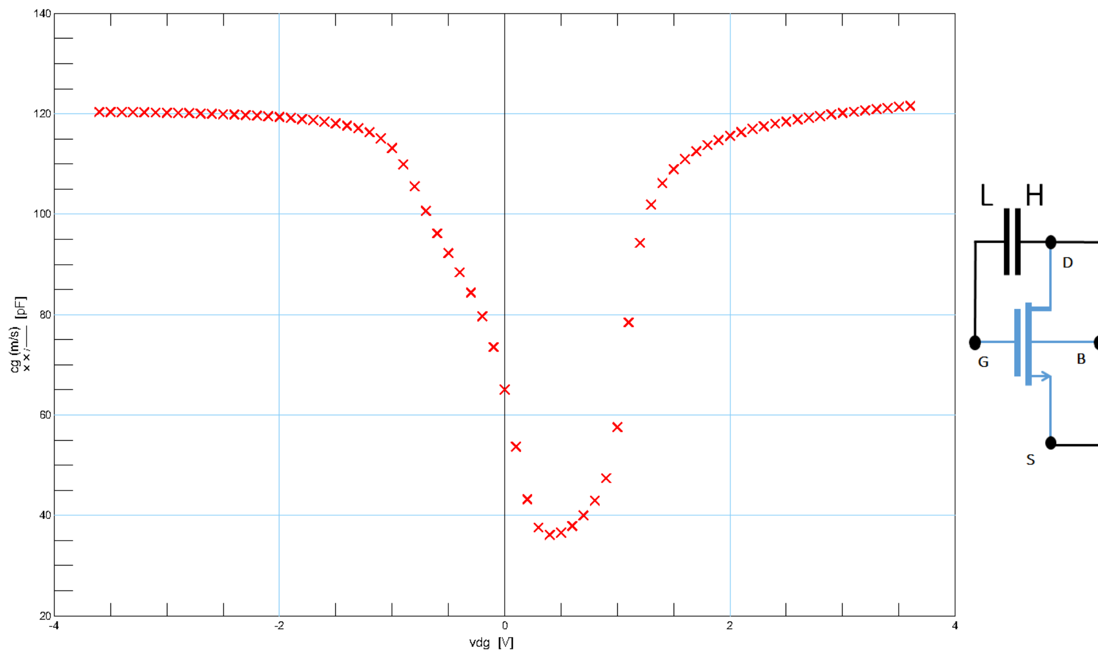

Fig. 4.6: Drain Source Bulk-Gate capacitance versus V_{DSB} and measurement diagram

4.1.2 Junction capacitance measurement

These capacitances are formed by a PN junctions, and the C-V characteristics are like diode ones. Increasing the reverse bias voltage across the PN junction therefore decreases the diode capacitance.

Bulk drain

At the drain region a drain-to bulk junction capacitance is presented. Drain voltage linear swept from 0 to 40V with 1V step.

Bulk Source

At the source region a source-to bulk junction capacitance is presented. Source voltage linear swept from 0 to 3V with 0,1V step.

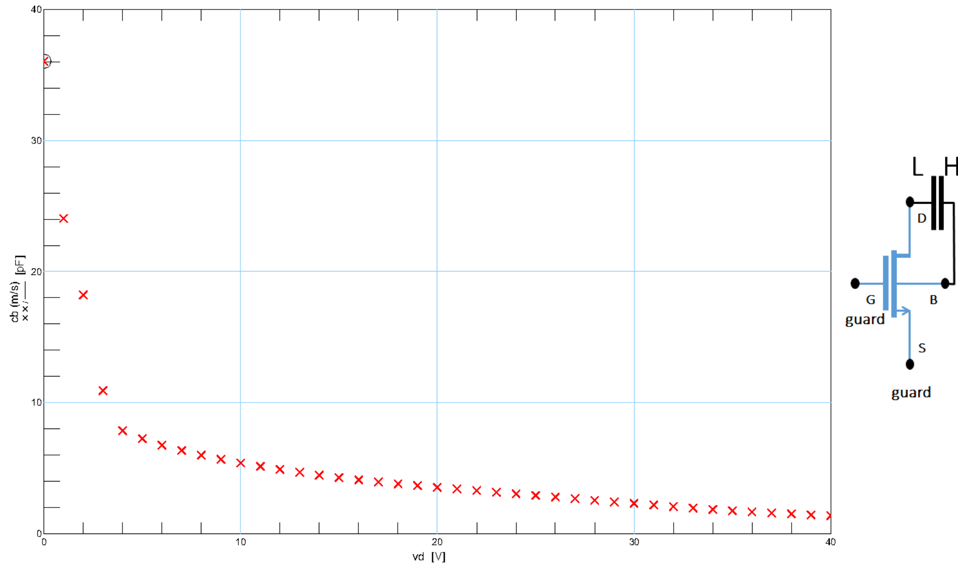

Fig. 4.7: Bulk-Drain capacitance versus V_D and its measurement diagram

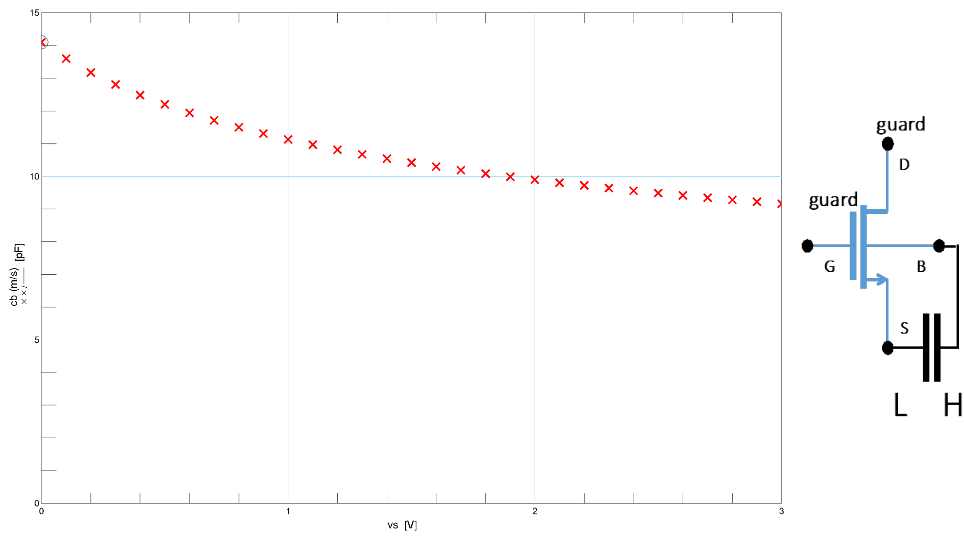

Fig. 4.8: Bulk-Source capacitance versus V_S and measurement diagram

4.2 Modeling process

Capacitance model is Sub-circuit implementation of two MOSFETs and diodes. Basic BSIM FET represents large-signal model, shortened MOSCAP with opposite channel type is used to revert depletion and inversion of specific LDMOS C-V profiling. Diodes are being used to represent pn junction capacitances CBS and CBD.

These extra connected components have no impact on IV characteristics of the device.

It is suggested to start capacitance model optimization from the largest device architecture, therefore an LDMOS with 150 um channel width has been chosen. It is required to postpone parasitics and tolerances of a small structure [7].

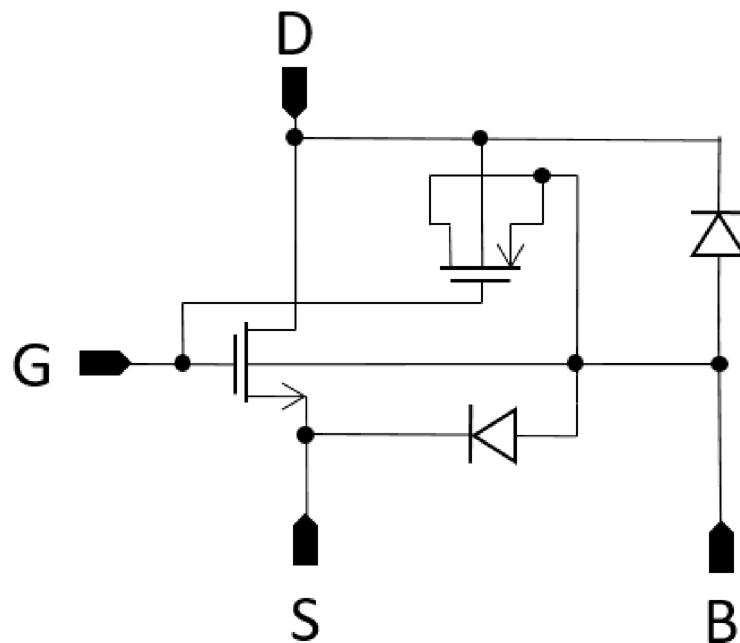

Fig. 4.9: Capacitance macro model

4.2.1 Gate capacitances fitting

Technological parameters such as oxide thickness, Ng, Wg remain the same for the MOSCAP as for the main MOS. Integrity of the IV characteristics is reached by non-interference in DC parameters of the BSIM MOSFET.

The starting point of capacitance characterization is Vth0, threshold voltage of shortened MOSCAP. This device of opposite channel type, compensate the unusual for MOS rotation of the depletion pit. By changing the threshold voltage of it, we can adjust the depletion region position and shape. As well as that we can optimize levels of inversion and accumulation capacitance by changing the DLC parameter, responsible for effective length of the MOSCAP channel. Voffcv and Noff are used to change the angle of the rising or falling slope of Cdsbg.

After receiving satisfying total gate capacitance fit we can proceed in adjusting the overlap capacitances. By changing CGDO, CGSO and CGBO, for drain, source and bulk overlap respectively, we can obtain good conformity of the model with measured data for Cgb CGDS and CGD.

Results of these characterization steps are presented below. Figure 4.10 displays state before C-V modeling and implementing of the macro-model, in figure 4.11 gate capacitance tuning was completed.

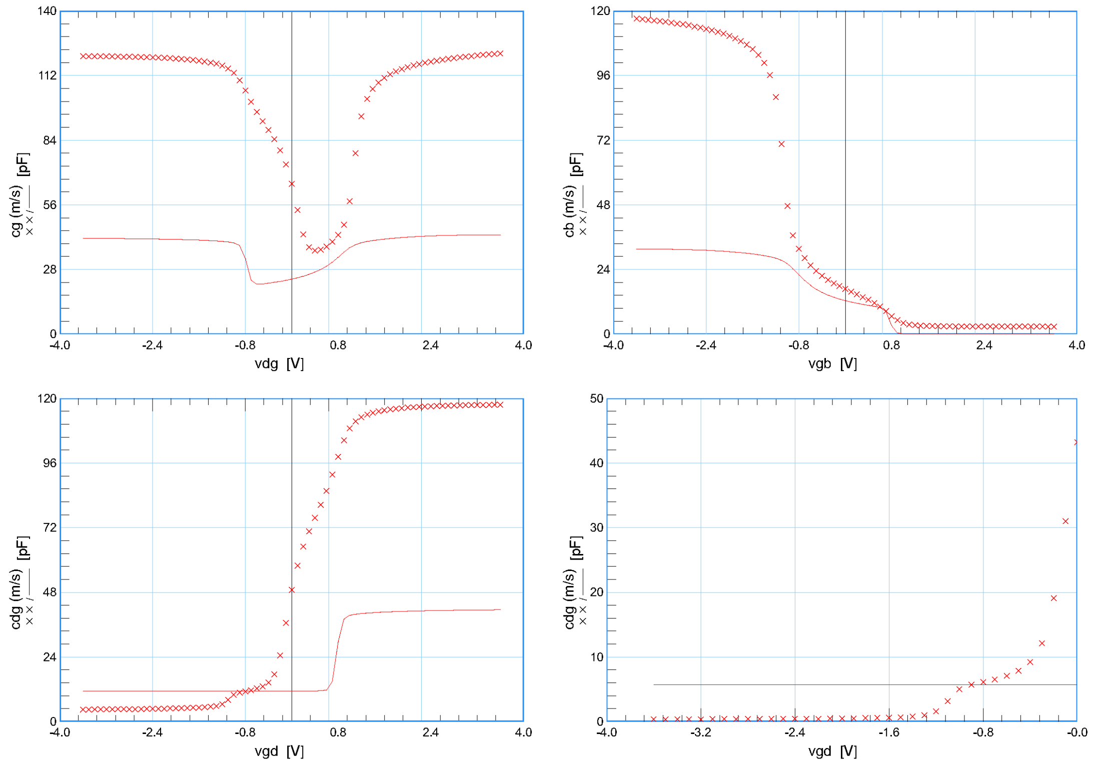

Fig. 4.10: Gate capacitances with DC parameters set

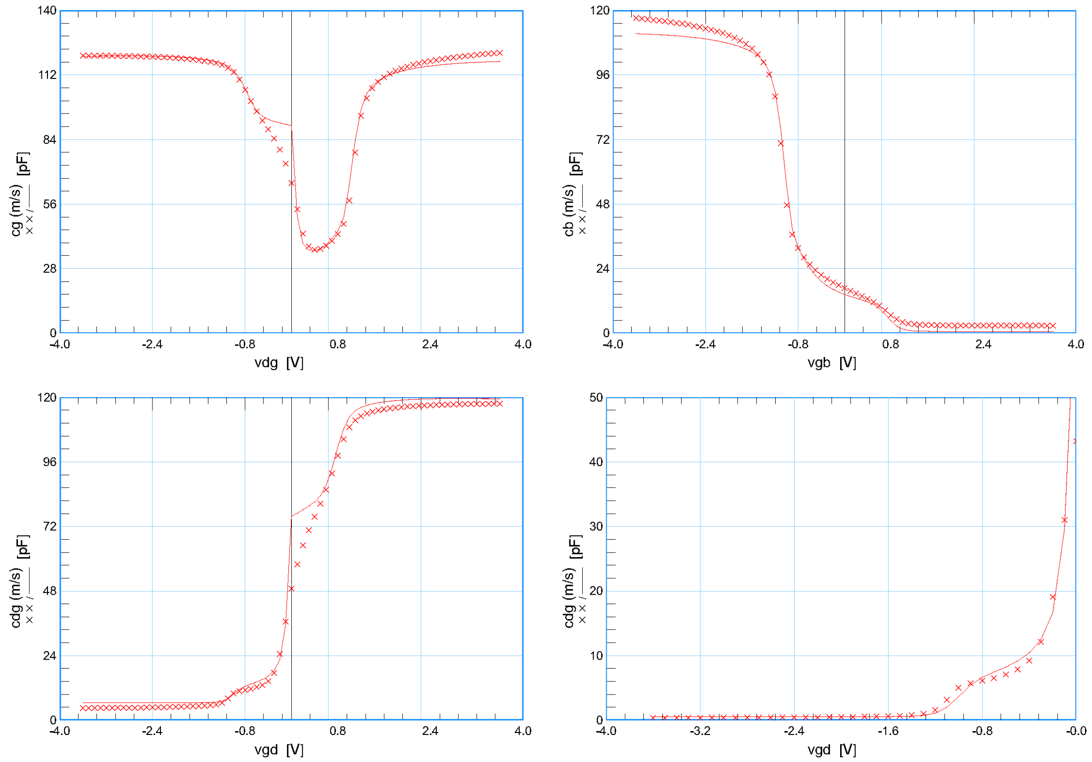

Fig. 4.11: Gate capacitances after modeling

4.2.2 Junction capacitances modeling

Unfortunaty basic BSIM is not capable to represent precisely junction capacitances scaling. Bulk-Drain and Bulk-Source p-n interfaces are having small capacitive value, however creating impact on behavior of bulk-driven applications.

For proper representation of junctions capacitance two diodes are added into macro-model. The best fit is achieved by producing certain capacitance trend. Therefore their tuning is the last step of capacitance characterization process.

Three parameters are used to control the C-V junctions curves. Cj models the fundamental level of capacitance in pn junctions. In most cases it can be substracted from device layout, perimeter and area capacitance. In our case this parameter was fitted empirically. Next option is to use Mj and Vj to fit the slopes of characteristics. As the result of combining these three parameters correct representation of junction capacitance was obtained (fig. 4.13).

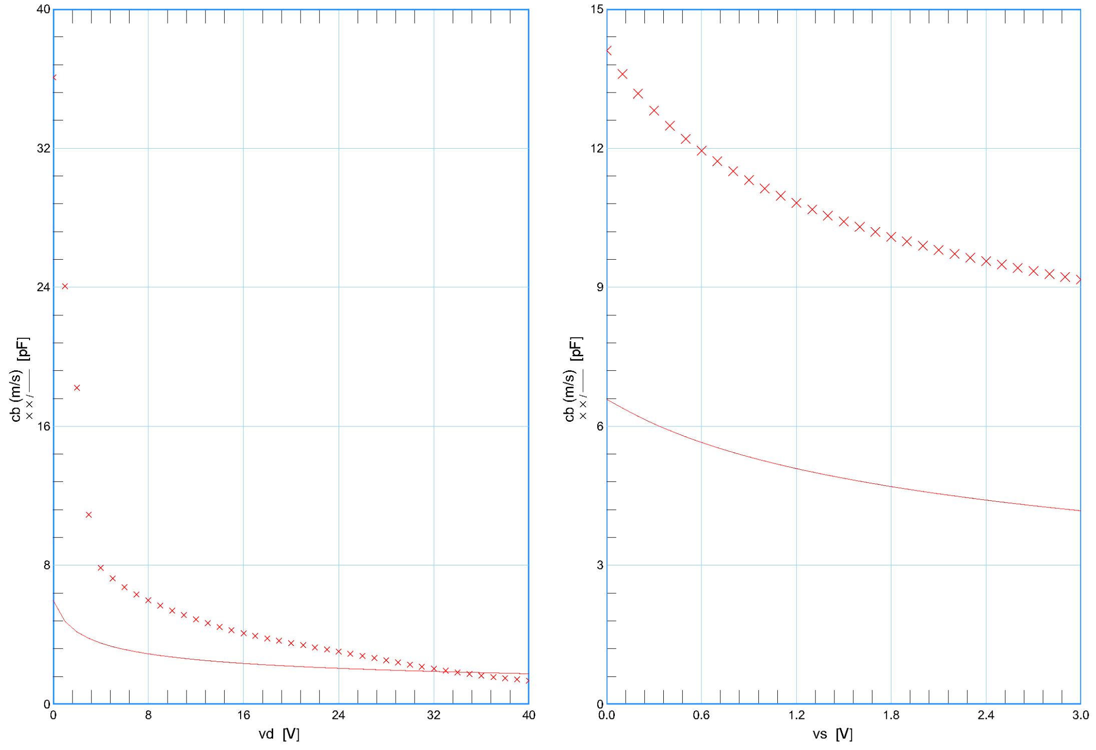

Fig. 4.12: C_{BD} and C_{BS} simulated with parameters from previous step

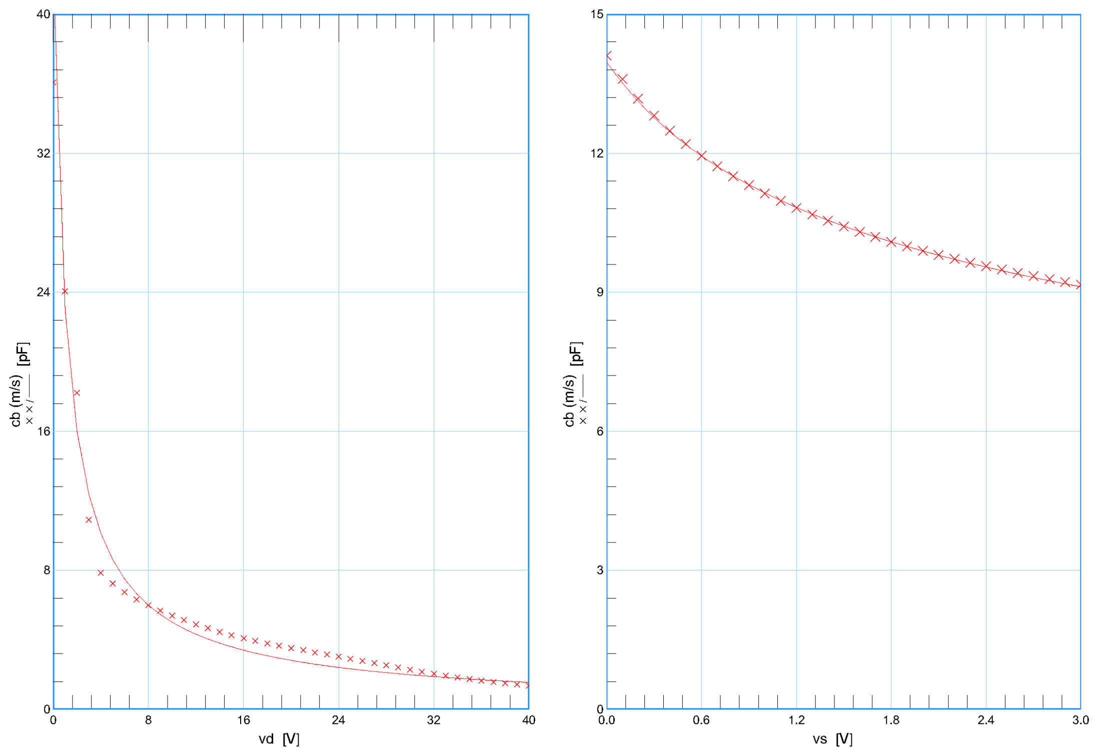

Fig. 4.13: C_{BD} and C_{BS} model fit simulated

4.3 Scaling of CV model

In most of the cases properly scalable DC model ensures fit of the capacitance model as well. Although in some cases some adjustment has to be made. Width-dependence binning parameters along with narrow width effect of the shortened MOS may assure good model fit with simulated data.

For capacitance scaling model 150, 20 and 3 μm channel width architectures have been used. Therefore having DC model precisely scalable only shift of the threshold voltage of shortened MOS was needed to imply. Thus only k3 parameter was involved. Result of that step is shown in figure below. Since the improvement was not so significant only after-state is presented.

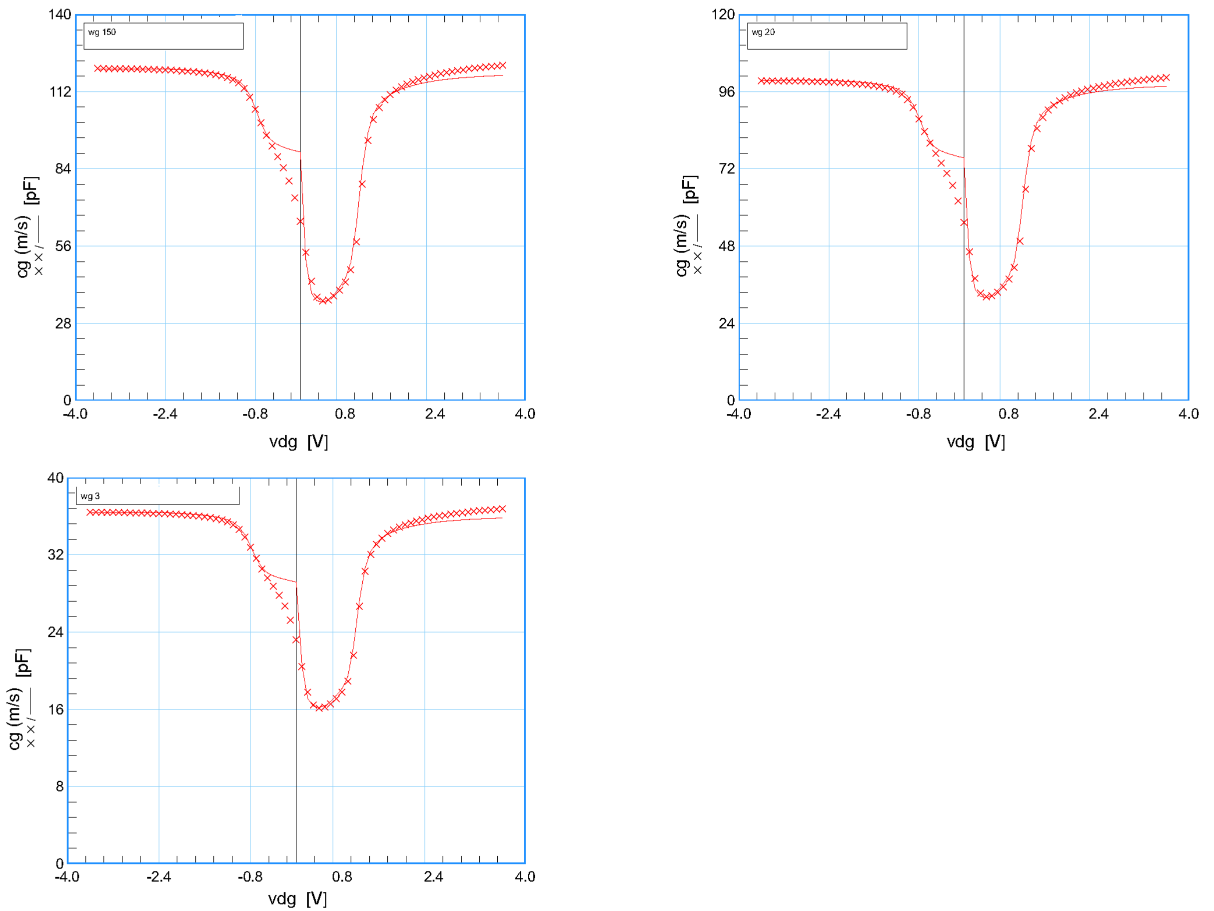

Fig. 4.14: C_{DSBG} simulated after implemented width dependence for 150, 20 and 3 μm channel width

4.4 Result

The result capacitance model parameters based on all previous steps are stated in table 4.4.

The RMS error of model in C-V profile is 9,88 %, of Bulk-Source and Bulk-Drain junctions 0,66 % and 1,5 % respectively.

Shortened MOS		**Main MOS**		**BS diode**	
Parameter	*Value*	*Parameter*	*Value*	*Parameter*	*Value*
Vth0	-1	Vth0	from DC	cj	$2{,}45 \cdot 10^{-15}$
Voffcv	$20 \cdot 10^{-3}$	Voffcv	-0,17	vj	0,8
Noff	2,6	Noff	2,5	mj	0,28
dlc	$-1{,}8 \cdot 10^{-7}$	dlc	-	**BD diode**	
dwc	$5{,}5 \cdot 10^{-10}$	dwc	$6{,}12 \cdot 10^{-10}$	*Parameter*	*Value*
k1	0,17	k1	from DC	cj	$1{,}7 \cdot 10^{-14}$
k2	0	k2	from DC	vj	1,19
k3	10	CGSO	$5{,}2 \cdot 10^{-10}$	mj	0,88
CGBO	$1{,}67 \cdot 10^{-10}$	CGBO	$1{,}3 \cdot 10^{-8}$		

Tab. 4.1: Optimized set of parameters for N-LDMOS capacitance model

Chapter 5

Conclusion

In this bachelor thesis, the results of measurements and modeling of LDMOS structure are presented. The technical information and the investigated devices have been kindly provided by ON Semiconductor Brno Design Center.

The first chapter of this work was meant to introduce HV power transistor device — LDMOS. In this part, physical differences compared to a conventional MOSFET device are presented. Several anomalous effects of LDMOS structure, which are not present in conventional MOSFET, such as quasi-saturation, self-healing effect, Kirk and kink effects has been studied and reported.

Onward, in the second chapter, we have described several modeling approaches for such a structure. Among those are EKV, Lumped-Charge methodology, BSIM, and HiSIM. Thus we had chosen the fourth generation BSIM model — BSIM4. In particular for its better accuracy, physical basis and frequent use in the semiconductor industry. Thereafter we gave the description of the most important parameters of that model that are used in the last part of this work.

In chapter 3, we described the characterization and modeling process of N-type LDMOS starting from a test case to a complete BSIM model of the device. Thus, at the beginning of the third chapter, we have prepared a background for the further modeling by measuring DC characteristics at the ON Semiconductor laboratory. Afterward, the parameters extraction was made. Important steps of modeling DC behavior of LDMOS transistor were marked. Finally, the BSIM4 model for a fixed geometry LDMOS structure with n-type channel has been created. In addition channel width scaling of the model was implemented into model. The satisfying results including a complete set of BSIM4 parameters and model representation compared to measured data are given in the last part of the chapter.

In the fourth chapter complete capacitance model of the LDMOS was created. Measured tests and connection diagrams were given. Gate capacitances and there-

after junction ones were fitted using sub-circuit implementation and BSIM parameter set. Bulk-source and bulk drain capacitances were fitted via diodes representing *p*-*n* junctions for better scaling properties. The RMS errors of C-V profile model was below 10 %, of junction capacitances 0,66 and 1,5 % for C_{BS} and C_{BD}. Scaling of the total C-V profiling on LDMOS with several channel widths was complete by modeling narrow width effect in shortened MOSCAP.

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List of symbols, physical constants and abbreviations

BJT	Bipolar Junction Transistor
BSIM	Berkeley Short-channel IGFET Model
CMOS	Complimentary MOS
C-V	Capacitance-Voltage
DC	Direct current
g_m	Transconductance, [S]
HiSIM	Hiroshima-university STARC IGFET Model
HV	High-Voltage
Id	Drain current, [A]
Is	Source current, [A]
I-V	Current-Voltage
JFET	Junction gate Field-Effect Transistor
LC	Lumped-Charge
LDMOS	Lateral double-Diffused Metal Oxide Semiconductor
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field-effect Tranzistor
Rds	Drain-Source resistance, [Ω]
RMS	Root Mean Square
SPICE	Simulation Program with Integrated Circuit Emphasis
VBS, VB	Bulk-Source voltage, [V]
VDMOS	Vertical Double Diffused MOS
VDS, VD	Drain-Source voltage, [V]
VGS, VG	Gate-Source voltage, [V]
VTH	Threshold voltage, [V]