



# General View on Fractional-Order All-Pass Filters Using Generalized Current Conveyors

HERENCSÁR, N.

Proceedings of the 2020 43rd International Conference on Telecommunications and Signal Processing (TSP), pp. 689-693

eISBN: 978-1-7281-6376-5

ISSN: 2157-023X

DOI: https://doi.org/10.1109/TSP49548.2020.9163482

Accepted manuscript

©2020 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works. HERENCSÁR, N., "General View on Fractional-Order All-Pass Filters Using Generalized Current Conveyors", 43rd International Conference on Telecommunications and Signal Processing (TSP), 2020. DOI: 10.1109/TSP49548.2020.9163482. Final version is available at <a href="https://ieeexplore.ieee.org/document/9163482">https://ieeexplore.ieee.org/document/9163482</a>

## General View on Fractional-Order All-Pass Filters Using Generalized Current Conveyors

Norbert Herencsar
Dept. of Telecommunications
Brno University of Technology
Technicka 12, 616 00 Brno, Czech Republic
Email: herencsn@feec.vutbr.cz

Abstract—The paper presents a general structure for realizing current-mode (CM) fractional-order all-pass filters (FOAPFs) using generalized first-kind five-port current conveyors (GCC5s). The proposed circuit topology employs two GCC5s and minimum number of passive components, i.e., one resistor and one fractional-order capacitor, both in grounded form. A total of eight CM FOAPFs using second-generation current conveyor are derived, which are capable of providing simultaneously both inverting and non-inverting current-outputs from high impedance terminals. A theoretical study of a variant created using universal current conveyor is provided, which verify the concept of the proposed circuit topology.

Index Terms—all-pass filter; APF; current-mode; fractionalorder filter; generalized first-kind five-port current conveyor; GCC5; universal current conveyor; UCC

#### I. INTRODUCTION

Current conveyors (CCs) have proved to be one of the most versatile active building blocks (ABBs) in circuit theory and have received considerable attention in realizing wide variety of circuit solutions [1], [2]. These include first-order filters, biquadratic filters, impedance simulators (including inductor simulators and capacitance multipliers), chaotic circuits, proportional-integral-derivative controllers, sinusoidal oscillators, precision rectifiers and non-linear circuits for squaring, square-rooting and vector summation. The motivation of this paper is to extend the knowledge about current-mode (CM) fractional-order all-pass filters (FOAPFs) and propose a new general topology using a generalized first-kind five-port current conveyor (GCC5) [3] and minimum passive components. All-pass filters are very important circuits for many analog signal processing applications. These are generally used in phase equalization and for introducing a frequency dependent delay while keeping the amplitude of the input signal constant over the desired frequency range [4]-[51]. The proposed circuit topology employs two GCC5s and only two passive components, namely one virtually grounded resistor and one virtually grounded capacitor. Both the passive components are grounded and the use of grounded capacitor makes the circuit suitable for monolithic integration. Limiting our study to second-generation current conveyor designs only, a total of eight FOAPFs have been derived from the topology. All variants are capable of simultaneously providing two explicit

Research described in this paper was financed by the Czech Science Foundation under grant no. 19-24585S.

current outputs from high impedance terminals and thus can realize both inverting and non-inverting APFs without any change of the circuit configuration. A theoretical study of the selected variant created using universal current conveyor (UCC) [52] has been included to verify the concept of the proposed circuit.

#### II. CIRCUIT DESCRIPTION

#### A. The Generalized Current Conveyor (GCC)

In the general design of frequency filters and oscillators with CCs it is of advantage to use the classical generalized current conveyor (GCC). Using the GCC, authors in [3] introduced new classification for CCs. In their viewpoint, the classification of CCs by generations is not suitable. For example, the thirdgeneration CC differs from the first-generation CC by the sign of one port current only and the term 'second-generation' does not in fact denotes a development stage but a certain property. According to this classification, the number of input ports X specifies the conveyor order, the number of all auxiliary ports Y determines the conveyor kind, and the number of output ports Z to which an independent current  $i_X$ is conveyed classifies the conveyor class. This classification has not undertaken yet, however, some of defined novel types of GCCs could be still expanded in the future. One of them is the generalized first-kind five-port current conveyor (GCC5) [3], which schematic symbol is shown in Fig. 1.

Relations between the individual terminals of the GCC5 can be described by the following matrix equation:

$$\begin{bmatrix} v_{X} \\ i_{Y} \\ i_{Z1} \\ i_{Z2} \\ i_{Z3} \end{bmatrix} = \begin{bmatrix} 0 & a & 0 & 0 & 0 \\ b & 0 & 0 & 0 & 0 \\ d_{1} & 0 & 0 & 0 & 0 \\ d_{2} & 0 & 0 & 0 & 0 \\ d_{3} & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{X} \\ v_{Y} \\ v_{Z1} \\ v_{Z2} \\ v_{Z3} \end{bmatrix}, \tag{1}$$

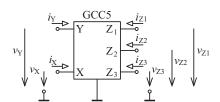


Fig. 1. Generalized first-kind five-port current conveyor

where  $a, b, d_1, d_2, d_3$  are the conveyance coefficients of the GCC5 that can be substituted by the values:  $a \in \{-1, +1\}$ ,  $b \in \{-1, 0, +1\}$ , and  $d_i \in \{-1, +1\}$  for i = 1, 2, 3. If in (1) a = +1, we consider a conventional (non-inverting) CC, while a = -1 characterizes an inverting current conveyor (ICC) [2]. With b = +1 the first-generation current conveyor (CCI or ICCI) [2] can be realized. Similarly, the second-generation CC (CCII or ICCII) [2] can be realized, if the b = 0 and the third-generation CC (CCIII or ICCIII) [2], when b = -1. Eventually, when  $d_i = +1$  we speak about a positive current conveyor, which is denoted by the "+" sign following the schematic symbol (e.g. ICCIII+), when  $d_i = -1$ , we consider the negative current conveyor, which is denoted by the "-" sign (e.g. CCI-). In general, the GCC5 represents 24 different types of multiple-output CCs of different generations.

#### B. The Universal Current Conveyor (UCC)

As it was mentioned above, the GCC5 is just a general tool for the initial filter design. For further implementation and simulation of the selected filter topology proposed in the first step using GCC5s, the universal current conveyor (UCC) [52] can be used. In 2000, the UCC was designed and developed using the CMOS 0.35  $\mu$ m technology under the designation UCC-N1B 0520 and produced in cooperation with ON Semiconductor Czech Republic, Ltd. It is an eight-port active element that schematic symbol is shown in Fig. 2. Analogous to differential difference current conveyor (DDCC) [2] or to differential difference complementary current conveyor (DDCCC) [2], the UCC has three high-impedance voltage inputs Y (one differencing - Y2, and two additive - Y1, and Y<sub>3</sub>), one low impedance input X, and four current outputs  $(Z_{1+},\ Z_{1-},\ Z_{2+},\ Z_{2-}).$  Outputs  $Z_{1-},\ Z_{2-}$  are inverse to outputs  $Z_{1+}$  and  $Z_{2+}$ .

Relations between the individual terminals of UCC can be described by the following hybrid matrix:

where  $\beta_k = 1 - \varepsilon_{vk}$  and  $\alpha_j = 1 - \varepsilon_{ij}$  (k = 1, 2, 3 and j = 1, 2, 3, 4) are the non-ideal voltage and current gains, respectively, and  $\varepsilon_{vk}$  ( $|\varepsilon_{vk}| \ll 1$ ) denote voltage tracking

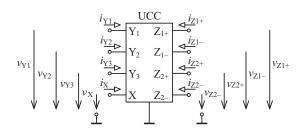


Fig. 2. Schematic symbol of universal current conveyor

errors and  $\varepsilon_{ij}$  ( $|\varepsilon_{ij}| \ll 1$ ) denote current tracking errors of the UCC, respectively.

By connecting or grounding suitable terminals of the UCC, it helps to realize different generations and types of current conveyors with single low impedance current input X [52]. Moreover, as it is mentioned above, the UCC can be also used for realization of 24 different types of multiple-output CCs of different generations, defined by the GCC5 (excluding those 12 that have three plus or three minus outputs Z). The multiple-output current follower (MO-CF) [53] can be also realized by the UCC when only current input X and all four current outputs Z are used, while voltage inputs are connected to the ground. Implementation of the balancedoutput operational transconductance amplifier (BOTA) using UCC is another option [54]. In this case, voltage inputs  $Y_1$ and Y2) are used and admittance GK is connected to current input X in order to represent transconductance  $g_m$ . Terminals  $Z_{1+}$  and  $Z_{1-}$  are used as current outputs.

## III. GENERAL VIEW ON CM FOAPFS AND DERIVED CIRCUITS

The proposed general CM FOAPF using two GCC5s, grounded resistor, and grounded fractional-order capacitor (FoC) [5], [12], [55] with pseudo-capacitance  $C_{\alpha}$  (0 <  $\alpha$  < 1) of impedance  $Z_{C_{\alpha}}(s)=1/C_{\alpha}s^{\alpha}$  is shown in Fig. 3.

Routine analysis yields to current transfer functions (TFs) that can be expressed in following general forms:

$$T_{1}(s) = \frac{I_{o1}}{I_{in}} = \frac{a_{2}d_{23}s^{\alpha}C_{\alpha} + a_{1}d_{12}G}{a_{2}s^{\alpha}C_{\alpha}(b_{2} + d_{21}) + a_{1}G(b_{1} + d_{11})} = \frac{a_{2}d_{23}s^{\alpha}C_{\alpha}R + a_{1}d_{12}}{a_{2}s^{\alpha}C_{\alpha}R(b_{2} + d_{21}) + a_{1}(b_{1} + d_{11})}, (3)$$

$$T_{2}(s) = \frac{I_{o2}}{I_{in}} = \frac{a_{2}d_{22}s^{\alpha}C_{\alpha} + a_{1}d_{13}G}{a_{2}s^{\alpha}C_{\alpha}(b_{2} + d_{21}) + a_{1}G(b_{1} + d_{11})} = \frac{a_{2}d_{22}s^{\alpha}C_{\alpha}R + a_{1}d_{13}}{a_{2}s^{\alpha}C_{\alpha}R(b_{2} + d_{21}) + a_{1}(b_{1} + d_{11})}. (4)$$

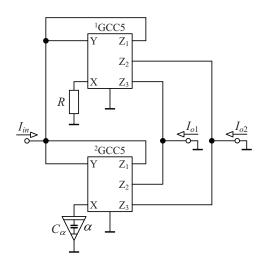


Fig. 3. Proposed general current-mode all-pass filter

TABLE I CONVEYANCE COEFFICIENTS OF GCC5s

Variant no.	<sup>1</sup> GCC5				<sup>2</sup> GCC5			
	$a_1$	$d_{11}$	$d_{12}$	$d_{13}$	$a_2$	$d_{21}$	$d_{22}$	$d_{23}$
#1	1	1	1	-1	1	1	1	-1
#2	1	1	1	-1	-1	-1	-1	1
#3	1	-1	-1	1	1	-1	-1	1
#4	1	-1	-1	1	-1	1	1	-1
#5	-1	1	1	-1	1	-1	-1	1
#6	-1	1	1	-1	-1	1	1	-1
#7	-1	-1	-1	1	1	1	1	-1
#8	-1	-1	-1	1	-1	-1	-1	1

To obtain an inverting and a non-inverting all-pass filter in the same configuration the following conditions must be fulfilled in (3) and (4):

$$b_1 = b_2 = 0, (5)$$

$$a_1 a_2 d_{11} d_{21} = 1,$$
  $d_{21} d_{22} = 1,$   $d_{21} d_{23} = -1,$  (6)

$$d_{11}d_{12} = 1, d_{11}d_{13} = -1. (7)$$

From (5) it is evident that in this work only the second-generation CCs are considered. Eight different variants satisfy conditions (5)–(7) and conveyance coefficients of GCC5s are given in Table III. In all eight cases both inverting (3) and non-inverting (4) CM APFs can be realized with the same circuit topology.

## IV. THE DESIGN EXAMPLE AND ITS CONCEPTUAL VERIFICATION

The variant #7 using ideal UCCs ( $\beta_k = 1$  and  $\alpha_j = 1$  for k = 1, 2, 3 and j = 1, 2, 3, 4) is shown in Fig. 4. Current TFs of the circuit are given as follows:

$$T_1(s) = \frac{I_{o1}}{I_{in}} = -\frac{s^{\alpha}C_{\alpha} - G}{s^{\alpha}C_{\alpha} + G} = -\frac{s^{\alpha}C_{\alpha}R - 1}{s^{\alpha}C_{\alpha}R + 1},$$
 (8)

$$T_2(s) = \frac{I_{o2}}{I_{in}} = \frac{s^{\alpha}C_{\alpha} - G}{s^{\alpha}C_{\alpha} + G} = \frac{s^{\alpha}C_{\alpha}R - 1}{s^{\alpha}C_{\alpha}R + 1}.$$
 (9)

As it is seen from these equations, both inverting (8) and non-inverting (9) types of CM FOAPF can be realized with the same circuit topology. The magnitude characteristic of both type CM FOAPFs can be expressed after replacing the  $s^{\alpha}$  by  $\omega^{\alpha}[\cos\left(\frac{\alpha\pi}{2}\right)+j\sin\left(\frac{\alpha\pi}{2}\right)]$  as:

$$|T_1(j\omega)| = |T_2(j\omega)| =$$

$$= \sqrt{\frac{\omega^{2\alpha} C_{\alpha}^2 R^2 - 2C_{\alpha} R \omega^{\alpha} \cos\left(\frac{\alpha\pi}{2}\right) + 1}{\omega^{2\alpha} C_{\alpha}^2 R^2 + 2C_{\alpha} R \omega^{\alpha} \cos\left(\frac{\alpha\pi}{2}\right) + 1}}, \quad (10)$$

while the phase responses of the filter are given as:

$$\angle T_1(j\omega) = \\
= \angle \frac{\left[1 - C_\alpha R\omega^\alpha \cos\left(\frac{\alpha\pi}{2}\right)\right] + jC_\alpha R\omega^\alpha \sin\left(\frac{\alpha\pi}{2}\right)}{\left[1 + C_\alpha R\omega^\alpha \cos\left(\frac{\alpha\pi}{2}\right)\right] + jC_\alpha R\omega^\alpha \sin\left(\frac{\alpha\pi}{2}\right)}, (11)$$

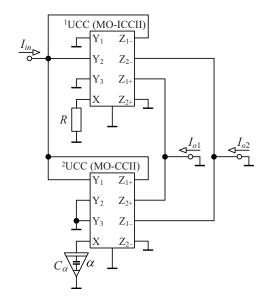


Fig. 4. Proposed inverting and non-inverting current-mode APF using UCCs: variant #7

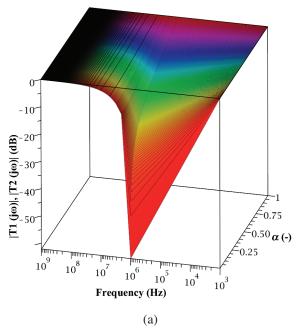
$$\angle T_2(j\omega) = \\
= \angle \frac{\left[C_\alpha R\omega^\alpha \cos\left(\frac{\alpha\pi}{2}\right) - 1\right] + jC_\alpha R\omega^\alpha \sin\left(\frac{\alpha\pi}{2}\right)}{\left[C_\alpha R\omega^\alpha \cos\left(\frac{\alpha\pi}{2}\right) + 1\right] + jC_\alpha R\omega^\alpha \sin\left(\frac{\alpha\pi}{2}\right)}. (12)$$

Hence, the phase (11) and (12) of current TFs alter from  $0^{\circ}$  to  $-180^{\circ}$  and  $180^{\circ}$  to  $0^{\circ}$ , respectively, while  $\omega$  changes from  $0{\to}\infty$ . Finally, the resulting pole  $(\omega_{\mathrm{p},\alpha})$  and zero  $(\omega_{\mathrm{z},\alpha})$  frequencies are evaluated. The resulted expressions are:

$$\omega_{\mathrm{p},\alpha} = \left\{ \frac{\left[ -\cos\left(\frac{\alpha\pi}{2}\right) - \sqrt{\cos\left(\frac{\alpha\pi}{2}\right)^2 - 1} \right]}{C_{\alpha}R} \right\}^{\alpha^{-1}}, \quad (13)$$

$$\omega_{z,\alpha} = \left\{ \frac{\left[ \cos\left(\frac{\alpha\pi}{2}\right) - \sqrt{\cos\left(\frac{\alpha\pi}{2}\right)^2 - 1} \right]}{C_{\alpha}R} \right\}^{\alpha^{-1}}.$$
 (14)

To verify the theoretical study, the proposed all-pass filter has been numerically validated. From above analysis it is evident that first-order APF exists only at  $\alpha=1$ . However, both magnitude and phase responses are dependent on value of  $\alpha$ . MAPLE plot given in Fig. 5(a) shows the effect of FoC order in range  $\alpha=\{0$  to  $1\}$  on magnitude responses of the filter. Subsequently, the effect of  $\alpha=\{0.25,0.5,0.75\}$  of FoC (that having the same impedance  $@f_{\rm p,z}=1$  MHz and  $\mp 90^{\circ}$  phase shifts) on phase responses vs. first-order responses are depicted in Fig. 5(b). Here, resistor and capacitor values used are as follows  $R=10~{\rm k}\Omega,~C_{0.25}=2~\mu{\rm F}\cdot{\rm sec}^{-0.75},~C_{0.5}=39.9~{\rm nF}\cdot{\rm sec}^{-0.5},~C_{0.75}=796.1~{\rm pF}\cdot{\rm sec}^{-0.25},~{\rm and}~C_1=15.9~{\rm pF},~{\rm respectively}.$ 



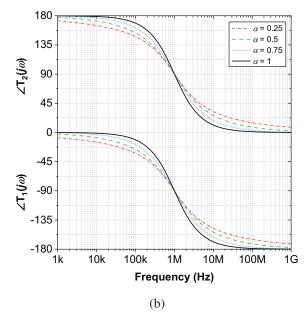


Fig. 5. FOAPF (a) magnitude and (b) phase responses for different  $\alpha$ .

#### V. CONCLUSION

The paper presents a general design of CM FOAPFs using GCC5s. The circuit topology is versatile and a total of eight variants have been derived from the general topology; all of which are capable of simultaneously realizing both inverting and non-inverting all-pass filtering functions. The variant #1 is same as that in [4]. Considering only ICCII-based topologies (variants #6 and #8) our literature survey has showed that no such CM APF exists in the open literature. A theoretical study of the selected variant #7 created using universal current conveyors has been included to verify its concept. It is expected that the used general design methodology is of wider use to the circuit designers and researchers in the field and such a technique is further used for designs of biquad filters and sinusoidal oscillators. Future works will be focused on following this direction.

#### REFERENCES

- G. Ferri and N. C. Guerrini, Low-Voltage Low-Power CMOS Current Conveyors. Springer US, 2003. ISBN 978-1-4020-7486-8
- [2] R. Senani, D. Bhaskar, and A. Singh, Current Conveyors: Variants, Applications and Hardware Implementations. Springer International Publishing, 2015. ISBN 978-3-319-08683-5
- [3] J. Cajka, T. Dostal, and K. Vrba, "General view on current conveyors," International Journal of Circuit Theory and Applications, vol. 32, no. 3, pp. 133–138, 2004. doi: 10.1002/cta.271
- [4] I. Khan, P. Beg, and M. Ahmed, "First order current mode filters and multiphase sinusoidal oscillators using CMOS MOCCIIs," *Arabian Journal for Science and Engineering*, vol. 32, no. 2 C, pp. 119–126, 2007.
- [5] A. Radwan, A. Soliman, and A. Elwakil, "First-order filters generalized to the fractional domain," *Journal of Circuits, Systems and Computers*, vol. 17, no. 1, pp. 55–66, 2008. doi: 10.1142/S0218126608004162
- [6] D. Biolek and V. Biolkova, "First-order voltage-mode all-pass filter employing one active element and one grounded capacitor," *Analog Integrated Circuits and Signal Processing*, vol. 65, no. 1, pp. 123–129, 2010. doi: 10.1007/s10470-009-9435-2

- [7] B. Metin, E. Arslan, N. Herencsar, and O. Cicekoglu, "Voltage-mode MOS-only all-pass filter," in *Proceedings of the 2011 34th International Conference on Telecommunications and Signal Processing (TSP)*, Budapest, Hungary, 2011, pp. 317–318. doi: 10.1109/TSP.2011.6043718
- [8] P. Beg, M. Siddiqi, and M. Ansari, "Multi output filter and four phase sinusoidal oscillator using CMOS DX-MOCCII," *International Journal of Electronics*, vol. 98, no. 9, pp. 1185–1198, 2011. doi: 10.1080/00207217.2011.582451
- [9] B. Metin, N. Herencsar, and K. Pal, "Supplementary first-order all-pass filters with two grounded passive elements using FDCCII," *Radioengi*neering, vol. 20, no. 2, pp. 433–437, 2011.
- [10] N. Pandey and S. Paul, "Single CDTA-based current mode all-pass filter and its applications," *Journal of Electrical and Computer Engineering*, 2011. doi: 10.1155/2011/897631
- [11] S. Maheshwari and B. Chaturvedi, "High-input low-output impedance all-pass filters using one active element," *IET Circuits, Devices and Sys*tems, vol. 6, no. 2, pp. 103–110, 2012. doi: 10.1049/iet-cds.2011.0213
- [12] B. Maundy, A. Elwakil, and S. Gift, "On the realization of multiphase oscillators using fractional-order allpass filters," *Circuits, Systems, and Signal Processing*, vol. 31, no. 1, pp. 3–17, 2012. doi: 10.1007/s00034-010-9235-z
- [13] B. Metin, N. Herencsar, and K. Vrba, "A CMOS DCCII with a grounded capacitor based cascadable all-pass filter application," *Radioengineering*, vol. 21, no. 2, pp. 718–724, 2012.
- [14] S. Minaei and E. Yuce, "High input impedance NMOS-based phase shifter with minimum number of passive elements," *Circuits, Systems, and Signal Processing*, vol. 31, no. 1, pp. 51–60, 2012. doi: 10.1007/s00034-011-9290-0
- [15] E. Yuce and S. Minaei, "Derivation of low-power first-order low-pass, high-pass and all-pass filters," *Analog Integrated Circuits and Signal Processing*, vol. 70, no. 1, pp. 151–156, 2012. doi: 10.1007/s10470-011-9689-3
- [16] N. Herencsar, J. Koton, and K. Vrba, "Low-voltage CMOS-RC fully cascadable transadmittance-mode all-pass filter," in *Proceedings of the 2013 36th International Conference on Telecommunications and Signal Processing (TSP)*, Rome, Italy, 2013, pp. 385–388. doi: 10.1109/TSP.2013.6613959
- [17] N. Herencsar, J. Koton, K. Vrba, and O. Cicekoglu, "New current-mode all-pass filter with grounded capacitor based on gain-variable CCIII," in *Proceedings of the 2013 IEEE AFRICON Conference*, Pointe-Aux-Piments, Mauritius, 2013, pp. 1–4. doi: 10.1109/AFR-CON.2013.6757657
- [18] S. Iqbal, C. Psychalinos, and N. Parveen, "First-order allpass filter using

- multi-input OTA," International Journal of Electronics, vol. 100, no. 10, pp. 1373–1382, 2013. doi: 10.1080/00207217.2012.743088
- [19] S. Maheshwari, J. Mohan, and D. Chauhan, "Novel voltage-mode cascadable all-pass sections employing grounded passive components," *Journal of Circuits, Systems and Computers*, vol. 22, no. 1, 2013. doi: 10.1142/S021812661250065X
- [20] N. Herencsar, S. Minaei, J. Koton, E. Yuce, and K. Vrba, "New resistorless and electronically tunable realization of dual-output VM all-pass filter using VDIBA," *Analog Integrated Circuits and Signal Processing*, vol. 74, no. 1, pp. 141–154, 2013. doi: 10.1007/s10470-012-9936-2
- [21] L. Safari, S. Minaei, and E. Yuce, "CMOS first-order current-mode all-pass filter with electronic tuning capability and its applications," *Journal of Circuits, Systems and Computers*, vol. 22, no. 3, 2013. doi: 10.1142/S0218126613500072
- [22] B. Metin, N. Herencsar, and O. Cicekoglu, "A low-voltage electronically tunable MOSFET-C voltage-mode first-order all-pass filter design," *Radioengineering*, vol. 22, no. 4, pp. 985–994, 2013.
- [23] E. Yuce, S. Minaei, N. Herencsar, and J. Koton, "Realization of first-order current-mode filters with low number of MOS transistors," *Journal of Circuits, Systems and Computers*, vol. 22, no. 1, 2013. doi: 10.1142/S0218126612500715
- [24] N. Herencsar, J. Koton, K. Vrba, and O. Cicekoglu, "Low-voltage fully cascadable resistorless transadmittance-mode all-pass filter," in Proceedings of the 2014 IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS), College Station, TX, USA, 2014, pp. 185–188. doi: 10.1109/MWSCAS.2014.6908383
- [25] J.-W. Horng, C.-M. Wu, and N. Herencsar, "Fully differential first-order allpass filters using a DDCC," *Indian Journal of Engineering and Materials Sciences*, vol. 21, no. 4, pp. 345–350, 2014.
- [26] J. Mohan and S. Maheshwari, "Additional high-input low-output impedance voltage-mode all-pass sections," *Journal of Circuits, Systems and Computers*, vol. 23, no. 6, 2014. doi: 10.1142/S0218126614500777
- [27] E. Yuce, S. Minaei, and N. Herencsar, "Grounded voltage controlled positive resistor with ultra low power consumption," *Elektronika ir Elektrotechnika*, vol. 20, no. 7, pp. 45–50, 2014. doi: 10.5755/j01.eee.20.7.8023
- [28] N. Herencsar, S. Minaei, J. Koton, and K. Vrba, "Voltage-mode all-pass filter design using simple CMOS transconductor: Non-ideal case study," in *Proceedings of the 2015 38th International Conference on Telecommunications and Signal Processing (TSP)*, Prague, Czech Republic, 2015, pp. 677–681. doi: 10.1109/TSP.2015.7296349
- [29] N. Herencsar, J. Koton, K. Vrba, S. Minaei, and I. C. Goknar, "Voltage-mode all-pass filter passive scheme based on floating negative resistor and grounded capacitor," in *Proceedings of the 2015 European Conference on Circuit Theory and Design (ECCTD)*, Trondheim, Norway, 2015, pp. 1–4. doi: 10.1109/ECCTD.2015.7300056
- [30] S. Maheshwari and D. Agrawal, "High performance voltage-mode tunable all-pass section," *Journal of Circuits, Systems and Computers*, vol. 24, no. 6, 2015. doi: 10.1142/S0218126615500802
- [31] D. Mitic, G. Jovanovic, M. Stojcev, and D. Antic, "Phase-synchroniser based on gm-C all-pass filter chain with sliding mode control," *Interna*tional Journal of Electronics, vol. 102, no. 3, pp. 362–375, 2015. doi: 10.1080/00207217.2014.896421
- [32] E. Tlelo-Cuautle, L. De La Fraga, K. Phanrattanachai, and K. Pitak-suttayaprot, "CDCTA and OTA realizations of a multi-phase sinusoidal oscillator," *IETE Technical Review*, vol. 32, no. 6, pp. 497–504, 2015. doi: 10.1080/02564602.2015.1043149
- [33] N. Herencsar, J. Koton, M. Sagbas, and U. E. Ayten, "New tunable resistorless CM first-order filter based on single CBTA and grounded capacitor," in *Proceedings of the 2016 IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Abu Dhabi, UAE, 2016, pp. 1–4. doi: 10.1109/MWSCAS.2016.7870064
- [34] E. Arslan, K. Pal, N. Herencsar, and B. Metin, "Design of novel CMOS DCCII with reduced parasitics and its all-pass filter applications," *Elektronika ir Elektrotechnika*, vol. 22, no. 6, pp. 46–50, 2016. doi: 10.5755/j01.eie.22.6.17222
- [35] R. Nandi, K. Mathur, and S. Pattanayak, "Single-CFA first-order all-pass filter," *IEICE Electronics Express*, vol. 13, no. 4, 2016. doi: 10.1587/elex.13.20151039
- [36] H. Yildiz, A. Toker, S. Kilinc, and S. Ozoguz, "Low frequency active only filters with small chip area," *Analog Integrated Circuits and Signal Processing*, vol. 89, no. 3, pp. 739–747, 2016. doi: 10.1007/s10470-016-0777-2

- [37] R. Nandi, K. Mathur, and S. Pattanayak, "Electronically tunable allpass filter: Linear VCO design," *IEICE Electronics Express*, vol. 13, no. 6, 2016. doi: 10.1587/elex.13.20160059
- [38] E. Yuce and S. Minaei, "A first-order fully cascadable current-mode universal filter composed of dual output CCIIs and a grounded capacitor," *Journal of Circuits, Systems and Computers*, vol. 25, no. 5, 2016. doi: 10.1142/S0218126616500420
- [39] N. Herencsar, J. Koton, and P. Hanak, "Universal voltage conveyor and its novel dual-output fully-cascadable VM APF application," *Applied Sciences*, vol. 7, no. 3, 2017. doi: 10.3390/APP7030307
- [40] S. Maheshwari and D. Agrawal, "Cascadable and tunable analog building blocks using EX-CCCII," *Journal of Circuits, Systems and Computers*, vol. 26, no. 6, 2017. doi: 10.1142/S0218126617500931
- [41] P. Thitimahatthanagusol, C. Saetiaw, T. Thosdeekoraphat, C. Thongsopa, and S. Summart, "CCCIIs-based first-order all-pass filter and quadrature oscillators," *Journal of Circuits, Systems and Computers*, vol. 26, no. 6, 2017. doi: 10.1142/S0218126617500943
- [42] Y. Chen and W. Li, "Compact and broadband variable true-time delay line with DLL-based delay-time control," *Circuits, Systems, and Signal Processing*, vol. 37, no. 3, pp. 1007–1027, 2018. doi: 10.1007/s00034-017-0594-6
- [43] N. Herencsar, J. Koton, A. Lahiri, U. Ayten, and M. Sagbas, "Resistorless current-mode first-order all-pass filter with electronic tuning employing low-voltage CBTA and grounded capacitor," *Journal of Circuits, Systems and Computers*, vol. 27, no. 2, 2018. doi: 10.1142/S0218126618500317
- [44] D. Ozenli, A. Yesil, E. Arslan, and H. Kuntman, "Novel first order current mode MOS-C phase shifters," *Elektronika ir Elektrotechnika*, vol. 24, no. 1, pp. 31–35, 2018. doi: 10.5755/j01.eie.24.1.20157
- [45] S. Aghazadeh, H. Martinez, and A. Saberkari, "5GHz CMOS all-pass filter-based true time delay cell," *Electronics*, vol. 8, no. 1, 2019. doi: 10.3390/electronics8010016
- [46] D. Agrawal and S. Maheshwari, "An active-C current-mode universal first-order filter and oscillator," *Journal of Circuits, Systems and Computers*, vol. 28, no. 13, 2019. doi: 10.1142/S0218126619502190
- [47] M. Masud, A. A'ain, I. Khan, and N. Husin, "Design of voltage mode electronically tunable first order all pass filter in ±0.7 V 16 nm CNFET technology," *Electronics*, vol. 8, no. 1, 2019. doi: 10.3390/electronics8010005
- [48] M. Masud, A. A'ain, I. Khan, and N. Shaikh-Husin, "A CNTFET-C first order all pass filter," *Analog Integrated Circuits and Signal Processing*, vol. 100, no. 2, pp. 257–268, 2019. doi: 10.1007/s10470-018-1361-8
- [49] B. Metin, N. Herencsar, V. Kledrowetz, and O. Cicekoglu, "MOS-only voltage-mode all-pass filter core suitable for IC design," AEU International Journal of Electronics and Communications, vol. 110, 2019. doi: 10.1016/j.aeue.2019.152834
- [50] M. Faseehuddin, J. Sampe, S. Shireen, and S. Md Ali, "Minimum component all pass filters using a new versatile active element," *Jour*nal of Circuits, Systems and Computers, vol. 29, no. 5, 2020. doi: 10.1142/S0218126620500784
- [51] B. Maundy, A. Elwakil, L. Belostotski, and N. Herencsar, "Single transistor RC-only second-order allpass filters," *International Journal* of Circuit Theory and Applications, vol. 48, no. 2, pp. 162–169, 2020. doi: 10.1002/cta.2721
- [52] D. Becvar, K. Vrba, V. Zeman, and V. Musil, "Novel universal active block: A universal current conveyor," in *Proceedings of the* 2000 IEEE International Symposium on Circuits and Systems (IS-CAS), Geneva, Switzerland, 2000, pp. III–471–III–474. doi: 10.1109/IS-CAS.2000.856099
- [53] J. Jerabek and K. Vrba, "SIMO type low-input and high-output impedance current-mode universal filter employing three universal current conveyors," AEU - International Journal of Electronics and Communications, vol. 64, no. 6, pp. 588–593, Jun 2010. doi: 10.1016/j.aeue.2009.03.002
- [54] N. Herencsar and K. Vrba, "Current conveyors-based circuits using novel transformation method," *IEICE Electronics Express*, vol. 4, no. 21, pp. 650–656, 2007. doi: 10.1587/elex.4.650
- [55] M. D. Ortigueira, "An introduction to the fractional continuoustime linear systems: the 21st century systems," *IEEE Circuits and Systems Magazine*, vol. 8, no. 3, pp. 19–26, Third 2008. doi: 10.1109/MCAS.2008.928419