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MOS-Only Voltage-Mode All-Pass Filter Core Suitable for IC Design

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ABSTRACT

In this paper, an area efficient CMOS first-order voltage-mode (VM) all-pass filter (APF) is proposed. The introduced resistorless MOS-only core circuit consists of three transistors only. For the design three transconductances and one gate-to-source capacitance of MOS transistors are sufficient instead of external passive resistors and capacitors, while the full implementation of the VM APF consists of 12 MOS transistors and one grounded capacitor only. Hence, the proposed circuit exhibits important features such as simplicity, permitting reduced chip area when integrated and wide operating frequency range compared to classical analog counterparts that require active elements employing large number of transistors. The theoretical results are in detail verified by numerous post-layout simulations using Cadence IC6 Spectre analog design environment. In the design, medium V_{th} transistors with 1.8 V supply voltage were used and modeled by the TSMC 180 nm CMOS process parameters available in EUROPRACTICE IC Service design kit. The post-layout simulated pole frequency of the VM APF is 4.825 MHz, the implemented layout including metal-insulator-metal on-chip capacitor occupies an area of 31.1 μm×39.5 μm, while the total power consumption of the filter is found to be only 92.57 μW.

1. Introduction

Recently, there is growing demand for analog filter structures circuits [1]–[30] operated with low-voltage and with capabilities of higher frequency of operation [31]. Most conventional analogue building blocks (ABBs) based on Op-Amps, Current Conveyors, etc. may remain inadequate for applications beyond tens of megahertz frequency range or may require advanced ABB with larger number of transistors. For higher frequencies, g_m-RL [20], or g_m-C [21] type filters can be preferred. In the most of the publications in the literature active component count is a comparison parameter in analog filter designs. This is understandable since it directly gives an idea about power consumption and chip area. However, in many recent papers about circuits with reduced chip area and power consumption, MOSFET-only analog design approach attracts growing attention [19], [22]–[30].

In MOSFET-only design approach only metal-oxide-semiconductor (MOS) transistors operating in the saturation region are used instead of generic active elements. Moreover, instead of passive resistors, the transconductance (g_m) parameter of MOS is used to obtain resistive (or conductive) dimension for analog circuit design. In other words, the small-signal model of the MOS transistor with its transconductance and gate-to-source capacitance (C_{gs}) is very suitable for designing high performance active circuits. Such applications are therefore expected to exhibit important features such as reduced number of transistors, simplicity, reduced chip area, and wide operating frequency range compared to classical analog circuits that employ standard ABBs.

In this study, an easily integrable area efficient CMOS first-order voltage-mode (VM) all-pass filter (APF) is proposed. All-pass filters are widely used as phase equalizers where they shift the phase of an input signal without altering its amplitude. Table 1 provides a fair performance comparison of proposed VM APF to state-of-the-art VM APFs [1]–[21] based on relevant criterion. The basic core topology of the proposed filter employs only 3 MOS transistors operating in saturation mode. In addition, the on-chip implemented VM APF containing an additional biasing circuitry and inverting output voltage level shifter employs in total 12 transistors and a single grounded capacitor. Therefore, it was very favorable in Cadence IC6 Spectre analog design environment from the integrated circuit implementation point of view.

2. Circuit Description

The proposed first-order VM APF core circuit is shown in Fig. 1. Assuming that size of the transistor M_2 is large enough such that its gate-to-source capacitance is at least an order of magnitude greater than the C_{gs} of M_1 and M_3 with the matching condition of

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Table 1
Comparison of previously published state-of-the-art first-order all-pass filters.

Ref.	Operation mode	No. and ABB type[b]	No. of transistors	No. of $R/C/L$ (gr. or float.)	No passive/ active matching constraints	Technology	Power supplies (V)	f_{p_sim} (Hz)	Power consumption (W)	Area of designed layout/ fabricated APF on-chip
[1]	Voltage-mode	1 CCII–	–	1 float.; 2 gr./1 float./0	no	–	–	–	–	NA
[2][a]	Voltage-mode	1 CCII–	NA	2 gr./1 float./0	no	D[d]	–	1 k	–	NA
[3][a]	Voltage-mode	1 FTFN	17	2 gr./1 float./0	no	TÜBİTAK YITAL 3 μm CMOS[d]	±5	159 k	–	NA
[4][a]	Voltage-mode	1 CCII+	NA	2 float./1 float./0	no	D[d]	±12	159 k	–	NA
[5][a]	Voltage-mode	1 CCII–	NA	1 float.; 1 gr./1 float./0	no	D[e]	±12	1 k	–	NA
[6][a]	Voltage-mode	2 CCII+	NA	2 gr./2 gr./0	no	D[e]	±12	15.9 k	–	NA
[7]	Voltage-mode	1 DO-CCII	23[c]	2 float./1 gr./0	no	TSMC 350 nm CMOS[d]	±1.5	1 M	–	NA
[8]	Voltage-mode	1 MCCII–	21[c]	2 float./1 gr./0	no	TSMC 350 nm CMOS[d]	±2.5	1 M	–	NA
[9][a]	Voltage-mode	1 FD-Op-Amp	NA	1 float./1 float./0	yes	D[e]	±5	33.9 k	–	NA
[10]	Voltage-mode	1 VD-DIBA	NA	0/1 gr./0	yes	D[e]	±5	316 k	–	NA
[11]	Voltage-mode	1 VDIBA	6[c]	0/1 float./0	yes	TSMC 180 nm CMOS[d]	±0.9	9.44 M	10.5 m	NA
[12][a]	Voltage-mode	2 OTA, 1 DVB	34[c]	0/1 gr./0	no	TSMC 180 nm CMOS[d]	±0.9	1.658 M	–	NA
[13]	Voltage-mode	2 Subtractors	20	1 float./1 gr./0	yes	IBM 130 nm CMOS[d]	±0.75	6.37 M	1.77 m	NA
[14]	Voltage-mode	MOS-RC circuit	6	1 float./1 gr./0	yes	350 nm CMOS[f]	3.3	1.59 M	–	NA
[15]	Current-mode	MOS-C circuit	10	0/1 float./0	no	40 nm CMOS[d]	±1.25	512 k	980 μ	NA
[16][a]	Voltage-mode	2 IVB	5	0/1 float./0	yes	TSMC 180 nm CMOS[d]	±0.9	3.18 M	–	NA
[17][a]	Current-mode	BJT-C circuit	6[c]	0/1 gr./0	yes	PR100N (PNP) & NP100N (NPN)[d]	1.5	159 k	169 μ	NA
[18]	Current-mode	2 DO-CF	10	0/1 gr./0	yes	TSMC 180 nm CMOS[d]	±0.9	2.99 M	266 μ	NA
[19][a]	Voltage-mode	MOS-only circuit	4[c]	0/0/0	no	TSMC 350 nm CMOS[g1]	1.65	150 M	–	NA
[20]	Current-mode	MOS-RL circuit	3	1 float./0/1 gr.	no	IBM 130 nm CMOS[g2]	1.5	8.74 G	19 m	186 μm×125 μm
[21][a]	Current-mode	MOS-C circuit	8	0/1 float./0	no	TSMC 180 nm CMOS[d]	1.8	9.4 M	760 μ	NA
This work (core circuit in Fig. 1)	Voltage-mode	MOS-only circuit	3[c]	0/0/0	no	–	–	–	–	NA
This work (full circuit in Fig. 4)	Voltage-mode	MOS-C circuit	12	0/1 gr./0	no	TSMC 180 nm CMOS[g2]	1.8	4.825 M	92.57 μ	31.1 μm×39.5 μm

Note:
–: Not mentioned; NA: Not applicable; D: Discrete IC(s) used: [2], [4], [6] AD844; [9] LMH6550; [10] OPA860 & AD8130
[a] Considered circuit: [2] Fig. 1; [3] Fig. 2(a); [4] Fig. 2(a); [5] Fig. 1; [6] Fig. 1(a); [9] Fig. 3; [12] Fig. 1; [16] Fig. 2; [17] Fig. 4; [19] Fig. 3(a); [21] Fig. 3(a)
[b] Refer Appendix for nomenclature of the ABBs
[c] Ideal current source(s) used
[d] OrCAD PSpice simulation results
[e] Experimental measurement results
[f] HSPICE simulation results
[g] Cadence IC6 Spectre simulation results: [1]pre-layout; [2]post-layout

transconductance gains of $2g_{m3} = g_{m2}$, routine analysis yields the following transfer function (TF):

$$T(s) = \frac{V_{OUT}}{V_{IN}} = \frac{-g_{m1} + sC_{gs2}}{g_{m1} + sC_{gs2}}, \tag{1}$$

where g_{mn} and C_{gsn} represent the transconductances and gate-to-source capacitances of the n-th transistor, respectively. In this circuit C_{gs2} can directly be used as the filter's capacitor if a high frequency operation is desired, but it can be shunted by a metal-insulator-metal (MIM) on-chip capacitor to improve linearity and as remedy against tolerances of gate-to-source capacitance. From (1), the phase response and the pole (ω_p) and zero (ω_z) frequencies of the filter can be respectively calculated as:

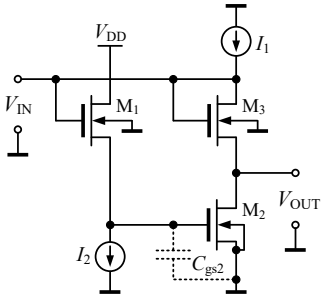

Figure 1: The proposed first-order voltage-mode all-pass filter core circuit.

$$\varphi(\omega) = 180^\circ - 2\tan^{-1}\left(\frac{\omega C_{gs2}}{g_{m1}}\right), \tag{2}$$

and

$$\omega_p = \omega_z = \frac{g_{m1}}{C_{gs2}}. \tag{3}$$

Hence, from (2) it can be seen that the proposed VM APF can provide phase shifting between 180° (at $\omega = 0$) to 0° (at $\omega = \infty$). The pole and zero frequency sensitivities of the proposed APF core are given as:

$$S_{g_{m1}}^{\omega_p,\omega_z} = -S_{C_{gs2}}^{\omega_p,\omega_z} = 1, \tag{4}$$

which are not higher than unity in magnitude.

3. Non-Ideal Analysis and Compensation for Non-Ideal Effects

MOS transistor small-signal ac model including dominant parasitic elements is shown in Fig. 2. From a signal point of view it behaves as a voltage-controlled current source, which accepts a signal v_{gs} between gate and source and provides a current $g_m v_{gs}$ at the drain terminal. The input resistance of this controlled source is very high, ideally infinite, while the output resistance that is looking into the drain is also high.

The proposed first-order VM APF core circuit including main parasitics is shown in Fig. 3. The following mathematical analysis is only focused on the effect of channel-length modulation, which is modeled by output resistance r_o of MOSFETs. Therefore, the body effect is ignored due to simplicity and other parasitic capacitances can also be neglected since they are either in parallel with C_{gs2} or their value can be too small compared to C_{gs2}. Indicating the output resistances of MOS transistors as $r_{on} = 1/g_{dsn}$ for $n = (1, 2, 3)$ and considering $C' = C + C_{gs2}$, where C is a MIM on-chip capacitor used in the implemented filter, the TF in (1) turns to (for $2g_{m3} = g_{m2}$):

$$T'(s) = \frac{V_{OUT}}{V_{IN}} = \\ = \frac{\left[\begin{array}{l} g_{ds3}\left(g_{m1} + g_{ds1}\right) + \\ \quad + g_{m3}\left(g_{ds1} - g_{m1}\right) + sC'\left(g_{m3} + g_{ds3}\right) \end{array}\right]}{\left(g_{m3} + g_{ds2} + g_{ds3}\right)\left(g_{m1} + g_{ds1} + sC'\right)}. \tag{5}$$

For the compensation of undesired g_{ds} parasitics, TF (5) was recalculated for the matching condition of $kg_{m3} = g_{m2}$ instead of $2g_{m3} = g_{m2}$ to obtain:

$$T''(s) = \frac{V_{OUT}}{V_{IN}} = \\ = \frac{\left\{\begin{array}{l} g_{m3}\left[g_{m1}(1-k) + g_{ds1}\right] + \\ \quad + g_{ds3}\left(g_{m1} + g_{ds1}\right) + sC'\left(g_{m3} + g_{ds3}\right) \end{array}\right\}}{\left(g_{m3} + g_{ds2} + g_{ds3}\right)\left(g_{m1} + g_{ds1} + sC'\right)}. \tag{6}$$

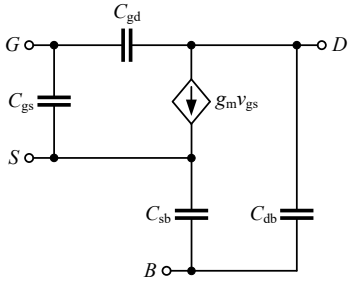

Figure 2: Simplified small-signal ac model of a MOS transistor.

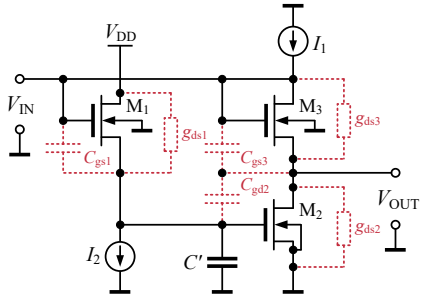

Figure 3: The proposed first-order VM APF core circuit including main parasitic elements.

From (6) we can find a $k = g_{m2}/g_{m3}$ value as given below that will preserve the all-pass response:

$$k = \frac{2\left(g_{m1} + g_{ds1}\right)\left(g_{m3} + g_{ds3}\right)}{g_{m1}g_{m3}}. \tag{7}$$

Using k in (6), the following TF can be obtained:

$$T'''(s) = \frac{V_{OUT}}{V_{IN}} = \\ = -\frac{\left(g_{m3} + g_{ds3}\right)\left(g_{m1} + g_{ds1} - sC'\right)}{\left(g_{m3} + g_{ds2} + g_{ds3}\right)\left(g_{m1} + g_{ds1} + sC'\right)}. \tag{8}$$

Note that here the APF response is preserved with a slightly modified gain and phase responses. However, for the slight deviation in the phase response due to g_{ds1}, phase compensation is easily possible by decreasing g_{m1} by an amount of g_{ds1}.

4. Simulation Results

To verify the theoretical study, the behavior of the designed first-order VM APF with full implementation shown in Fig. 4 has been verified by simulations in Cadence IC6 Spectre analog design environment. In the structure, transistors M_1–M_3 represent the initial core filter shown in Fig. 1 and M_4–M_{10} realize the bias current sources I_1, I_2. In addition, transistors M_{11} and M_{12} operate as an inverting voltage level shifter, which is very favorable sub-circuit for low-voltage operation since it employs only two NMOS transistors between its rails. It can be clearly seen that the first presented circuit shown in Fig. 1 has an offset voltage problem at the output. This offset voltage can be defined as $V_{OUT} = V_{IN} - V_{gs3}$ in Fig. 1. Therefore, in the full implementation, M_{11} and M_{12} transistors are added to the design to eliminate the output offset voltage. Therefore, the offset voltage can be calculated as follows: $V_{OUT} = -(V_{IN} - V_{gs1} + V_{gd11})$. DC power sup-

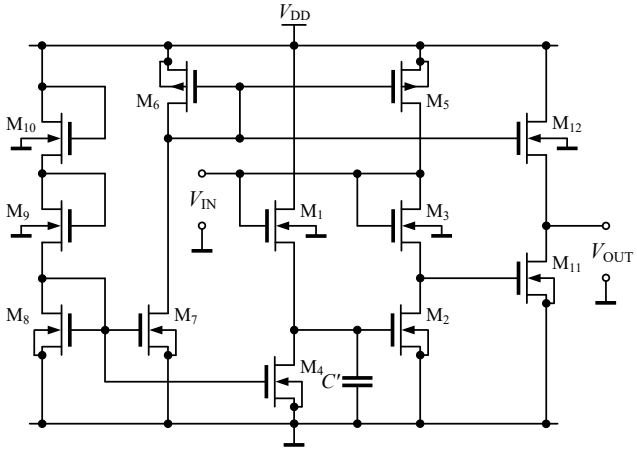

Figure 4: Full implementation of the proposed first-order VM APF core circuit.

Table 2
Aspect ratios of MOSFETs in implemented first-order VM APF shown in Fig. 4.

PMOS Transistors	W (μm) / L (μm)
M_5	20.2 / 1
M_6	4 / 1
NMOS Transistors	**W (μm) / L (μm)**
M_1	3 / 1
M_2	76 / 5.6
M_3	2.3 / 1.15
M_4, M_8	3.5 / 0.5
M_7	3.5 / 1.1
M_9, M_{10}	1.4 / 2
M_{11}	32 / 1
M_{12}	3 / 2.9

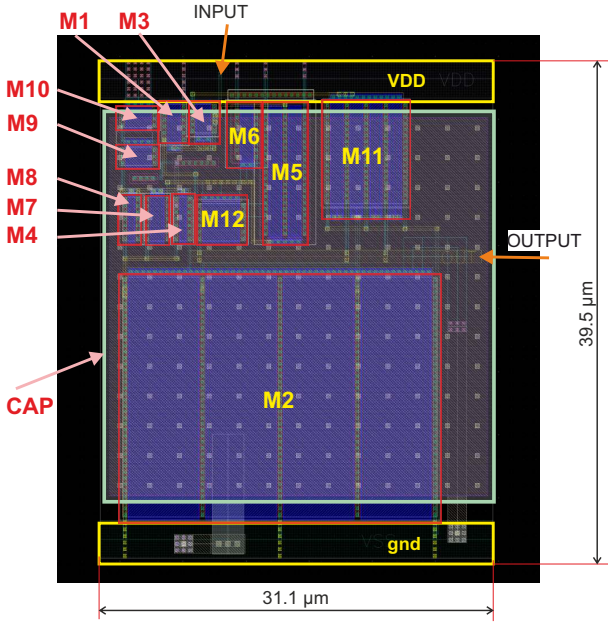

Figure 5: Layout of the designed first-order VM APF shown in Fig. 4.

ply voltage was set equal to V_{DD} = 1.8 V, all transistors with recommended minimal length 300 nm are of medium V_{th}, which were modeled by the TSMC 180 nm CMOS process parameters available in EUROPRACTICE IC Service design kit. The aspect ratios of transistors are listed in Table 2. Note that the W/L ratio of the transistor M_2 should be selected sufficiently high to reach significantly greater C_{gs} than other parasitics in the circuit. The corresponding layout with proper labeling and dimension 31.1 μm×39.5 μm is depicted in Fig. 5. During design DRC (design rule check) and ERC (electrical rule check) have been successfully performed. The total power consumption of the designed filter is found to be 92.57 μW.

First of all, the performance of the filter was tested by AC analyses. Fig. 6 shows the ideal, pre-layout, and post-layout (extraction settings: distributed resistors, distributed capacitors, coupling capacitors, no inductance) simulated gain and phase responses of the first-order VM APF and corresponding zoom in pole frequency region as inset. In simulations the value of the capacitor C has been selected as 1.79 pF. Note that this MIM capacitor (in layout labeled as CAP) appears parallel with C_{gs2} parasitic capacitance of the transistor M_2, which value is equal to 2.18 pF. Theoret-

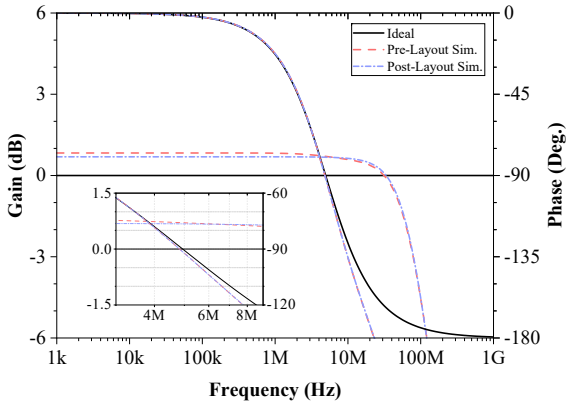

Figure 6: Ideal, pre-layout, and post-layout simulated gain and phase responses of the first-order VM APF and corresponding zoom in pole frequency region as inset.

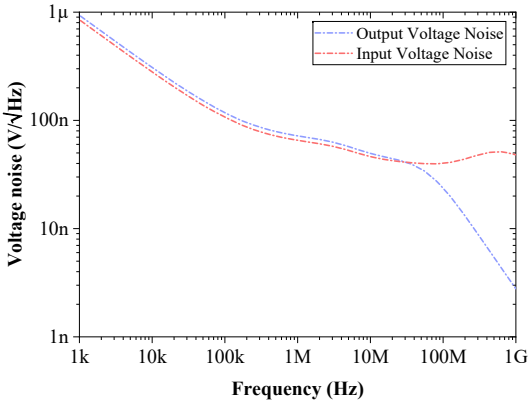

Figure 7: Post-layout simulated output and equivalent input noise variations vs. frequency.

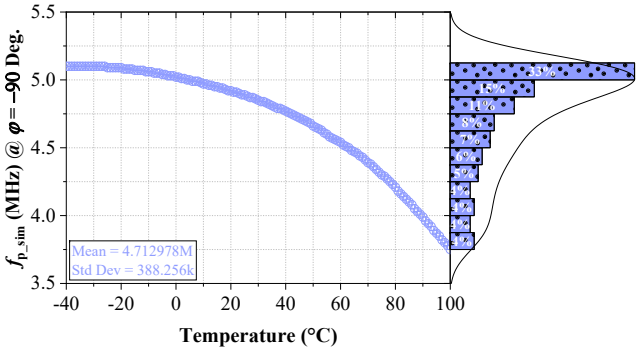

Figure 8: Post-layout simulated temperature dependence of pole frequency and corresponding histogram.

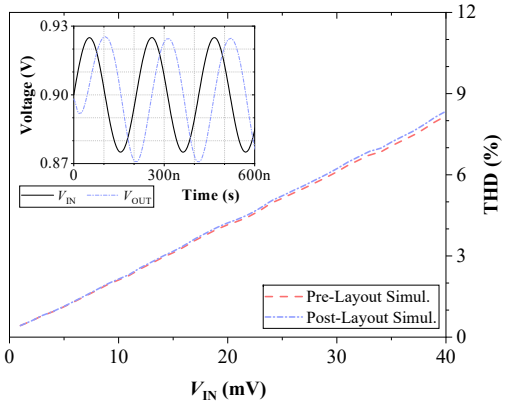

Figure 9: THD variation of the proposed first-order VM APF against applied input voltages at 4.825 MHz and post-layout simulated example of time-domain response with applied input voltage with amplitude of 25 mV as inset.

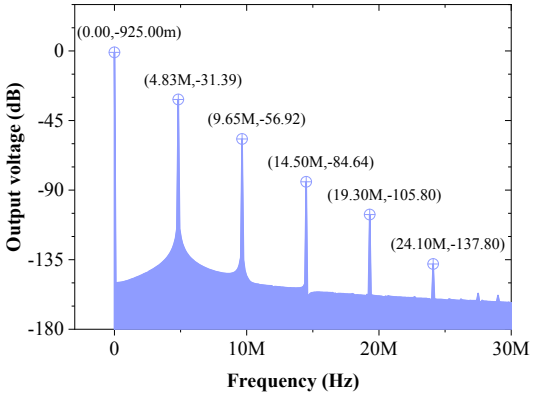

Figure 10: Post-layout simulated FFT spectrum of the proposed first-order VM APF.

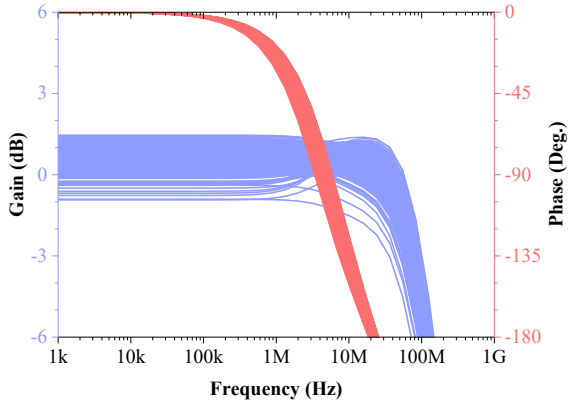

Figure 11: Monte Carlo statistical analysis: Post-layout simulated gain and phase responses change due to variation of process, mismatch, transistors, and capacitor.

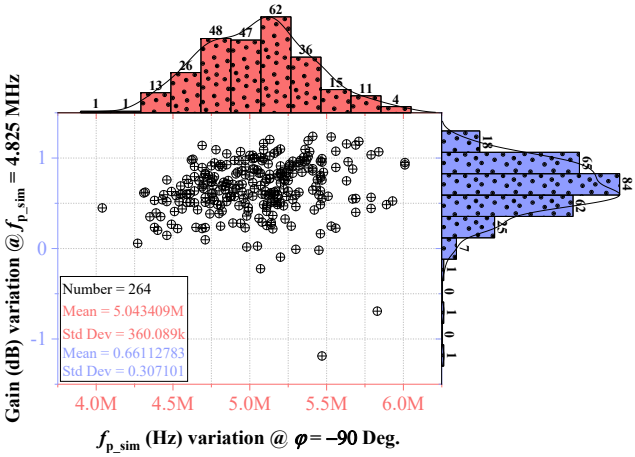

Figure 12: Evaluation of Monte Carlo statistical analysis results shown in Fig. 11: Variations of the pole frequency at -90° vs. variations of the gain of VM APF at simulated pole frequency 4.825 MHz.

ically, therefore, its total value equal to $C' \approx 3.97$ pF should be taken into account. Hence, the -90° phase shift is at pole frequency $f_{p\_sim} \cong 4.825$ MHz, which is close to the ideal f_{p_theor} equal to 4.94 MHz. The gain response for the output is flat far beyond the pole frequency in large frequency range. The obtained pre-layout and post-layout simulated gains at f_{p_sim} are equal to 0.71 dB and 0.68 dB, respectively. The gain roll-off and discrepancy against theoretical gain 0 dB can be mainly attributed to non-unity gain of the inverting voltage level shifter sub-circuit. The output and equivalent input noise variations against frequency have also been simulated, as it is shown in Fig. 7. The equivalent output/input noises at post-layout simulated pole frequency are found as 57.7 nV/$\sqrt{\text{Hz}}$ and 53.2 nV/$\sqrt{\text{Hz}}$, respectively. The effect of temperature on f_{p_sim} of the proposed APF at $\varphi = -90^\circ$ was examined in range $T \in \{-40; +100\}^\circ$C and the post-layout simulation results with corresponding statistical evaluation are depicted in Fig. 8.

To illustrate the time-domain performance, transient analysis is performed to evaluate the voltage swing capability and phase errors of the filter. The pre-layout and post-layout simulated total harmonic distortion (THD) variations with respect to amplitude of the applied sinusoidal input voltage at f_{p_sim} are depicted in Fig. 9. As an example, post-layout simulated time-domain result is shown as inset in which a sine-wave input of 25 mV amplitude was applied to the filter and it yields THD value of 5.2%. Moreover, the corresponding FFT spectrum of the output signal is shown in Fig. 10.

Finally, in order to evaluate the potential vary of the proposed filter parameters due to tolerances incurred from manufacturing processes, Monte Carlo statistical analysis is performed with default setting for process, mismatch, transistors, and MIM capacitor tolerances and 264 runs. Note that manufacturing processes may affect the value of each MOS, however, vary in value of M_2 is the most critical for the proposed VM APF. Therefore, potential change of g_{m2} is during filter implementation reduced by precise design of bias circuitry (proper settings of transistors M_9 and

M_{10}) and especially thanks to use of medium V_{th} transistors. Fig. 11 shows the post-layout simulated gain and phase responses of the proposed APF. Histograms in Fig. 12 demonstrate the variations of the pole frequency at $-90°$ with mean value 5.043 MHz and variations of the gain of APF at simulated pole frequency $f_{p\_sim} \cong 4.825$ MHz with mean value 0.66 dB, respectively.

Computed Cadence IC6 Spectre post-layout simulation results are in good agreement with theory and confirm the feasibility of the proposed circuit for on-chip fabrication.

5. Conclusion

In this brief, a simple first-order voltage-mode all-pass filter with reduced complexity designed with MOS-only technique is presented. The circuit has a potential to be used as an intermediate block in analog design applications. In particular, in this work the VM APF is implemented using medium V_{th} transistors supplied with 1.8 V voltage and modeled by the TSMC 180 nm CMOS process parameters available in EUROPRACTICE IC Service design kit. The functionality of the circuit is verified in detail with numerous post-layout simulations. The simulated pole frequency of the implemented VM APF is 4.825 MHz and its layout occupies an area of 31.1 μm×39.5 μm. The total power consumption is found to be only 92.57 μW. Depending on the selected sub-nanometer integrated circuit technology and the capacitor value, the circuit can operate in GHz frequency region.

Appendix

This section provides full nomenclature of the mentioned ABBs in Table 1 in alphabetical order.

CCII+ (–):	Plus-Type (Minus-Type) Second-Generation Current Conveyor
DO-CCII:	Dual-Output Second-Generation Current Conveyor
DO-CF:	Dual-Output Current Follower
DVB:	Differential Voltage Buffer
DV-VB:	Differential-Voltage Voltage Buffer
FD-Op-Amp:	Fully-Differential Operational Amplifier
FTFN:	Four-Terminal Floating Nullor
IVB:	Inverting Voltage Buffer
MCCII–:	Minus-Type Modified Second-Generation Current Conveyor
OTA:	Operational Transconductance Amplifier
VD-DIBA:	Voltage Differencing-Differential Input Buffered Amplifier
VDIBA:	Voltage Differencing Inverting Buffered Amplifier

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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