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Abstract—**This paper deals with a voltage-mode integer- and fractional-order oscillator design providing compact and simple CMOS structure. The proposed circuit consists of only one grounded/floating capacitor, one grounded/floating resistor, and one high-performance and versatile active element so-called voltage differencing inverting buffered amplifier (VDIBA), employing only six transistors. Compared with the corresponding already introduced fractional-order oscillators, it offers the benefit of low transistor count. In addition, it offers the well-known advantages of fractional-order oscillators about the capability for achieving very low and high oscillation frequencies with reasonable component values. The design parameters of the proposed oscillator can be electronically adjusted via change of order of the fractional-order capacitor and/or by means of bias current of the internal transconductance of the VDIBA. Theoretical results are verified by SPICE simulations using TSMC 0.18 μm level-7 LO EPI SCN018 CMOS process parameters with ±0.9 V supply voltages.**

Keywords—fractional calculus; fractional-order capacitor; fractional-order oscillator; MOS-RC oscillator; operational transconductance amplifier; voltage differencing inverting buffered amplifier; Valsa structure; VDIBA

I. INTRODUCTION

In the last years, the study of fractional-order oscillators started to be one of the main fundamental topics in fractional-order dynamic systems. This originated from the fact that extremely low and high frequencies of oscillation are possible through such structures [1], [2]. Many classical fractional-order oscillators were presented using conventional op-amps or its equivalent macromodels [3]. Although the aforementioned solutions could be implemented using commercially available discrete-component ICs, from the integration point of view they suffer from the increased transistor count that they are required for implementing the active cells [4]–[6]. In general, fractional-order oscillators offer: (i) independent tuning of the frequency and condition of oscillation, (ii) extremely low and high frequency of oscillation (FO) than its integer-order counterpart, (iii) requirement for capacitances with reasonable values, (iv) possibility for achieving different frequency of oscillation/start-up condition (CO) by only changing the order/capacitance values. The design of fractional-order oscillators requires fractional-order elements, e.g. fractional-order capacitors (FOCs) or fractional-order inductors. The impedance response of these fractional-order elements can be emulated via discrete element realizations [7]–[9]. On the other hand, the internal CMOS structures of analog building blocks (ABBs) are composed of excessive number of transistors.

TABLE I. COMPARATIVE STUDY OF FRACTIONAL-ORDER OSCILLATORS.

Ref.	No. of ABBs	No. of trans.	No. of $R / C / L$	Orders	Power supplies
[1]	-	1 BJT	1 gr. / 2 gr. / 1 fl.	-	-
[2]	1 opamp	-	3 fl.; 2 gr. / 1 fl.; 1 gr. / -	1.8	-
[3]	1 opamp	-	2 fl.; 2 gr. / 1 fl.; 1 gr. / -	1.31	-
[4]	-	20 CMOS	1fl. / 1 fl.; 1 gr. / -	1; 1.5; 2	±1.65 V
[5]	-	12 CMOS	1fl. / 1 fl.; 1 gr. / -	1; 1.2; 2	±1 V
[6]	-	22 CMOS	2 fl.; 1 gr. / 2 gr. / 1 fl.	2.75	±1 V
Our	1 VDIBA	6 CMOS	1 fl.; 1 gr. / 1 fl.; 1 gr. / -	1; 1.5; 2	±0.9 V

Nowadays the most attractive 'voltage differencing' device is the voltage differencing inverting buffered amplifier (VDIBA) [10]–[14], which has the simplest internal structure and it is easy to implement by commercially available ICs. The output stage of VDIBA is formed by two NMOS-based unity-gain inverting voltage buffer (VB), hence, there is no need of a more complex difference amplifier at its second stage. Therefore, the aim of this paper is to introduce low-transistor count, simple fractional-order oscillator design as well as its integer-order counterpart based on one VDIBA, two resistors, and two FOCs. In brief, the paper is organized as follows: Section II describes preliminary considerations of a VDIBA and design parameters of integer- and fractional-order oscillators. Simulation results of FOC computed via three branches Valsa RC structure and optimized using the genetic algorithm method with IEC 60063 compliant commercially available RC kit values [7] along with frequency and time domain behavior of the fractional-order oscillator are shown in Section III, while the last section concludes the paper.

II. CIRCUIT DESCRIPTION

A. Voltage Differencing Inverting Buffered Amplifier

The VDIBA is a recently introduced four-terminal active device [10]–[14], which circuit symbol is shown in Fig. 1. It is formed by a pair of high-impedance voltage inputs $v+$ and $v-$, a high-impedance current output z, and low-impedance voltage output $w-$. From implementation point of view, its input stage consists of differential-input single-output operational transconductance amplifier (OTA), which converts the input voltage to output current that flows out at the z
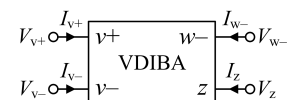

Fig. 1. Circuit symbol of VDIBA.

(6)

$$R_1 = -\frac{2\omega^\beta R_2 C_\beta \cos\left(\frac{\beta\pi}{2}\right)}{\omega^{\alpha+\beta} R_2 C_\alpha C_\beta \cos\left[\frac{(\alpha+\beta)\pi}{2}\right] + \omega^\alpha C_\alpha \cos\left(\frac{\alpha\pi}{2}\right) + \omega^\beta C_\beta \sin\left(\frac{\beta\pi}{2}\right) - \omega^\beta g_m R_2 C_\beta \cos\left(\frac{\beta\pi}{2}\right)},$$

FO: $\omega^{\alpha+\beta} R_2 C_\alpha C_\beta \left[\cos\left(\frac{(\alpha+\beta)\pi}{2}\right) + R_2 \cos\left(\frac{(\alpha+\beta)\pi}{2}\right) - 2\omega^\beta R_2 C_\beta \sin\left(\frac{\alpha\pi}{2}\right) - 2\sin\left(\frac{(\alpha-\beta)\pi}{2}\right)\right] = 0.$ (7)

terminal, and the output stage is unity-gain inverting voltage buffer. Using standard notation, the relationship between port currents and voltages of a VDIBA can be described by the following hybrid matrix:

$$\begin{bmatrix} I_{v+} \\ I_{v-} \\ I_z \\ V_{w-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & -1 & 0 \end{bmatrix} \begin{bmatrix} V_{v+} \\ V_{v-} \\ V_z \\ I_{w-} \end{bmatrix}. \quad (1)$$

The VDIBA is attractive for low transistor count, resistorless, and/or electronically controllable circuit applications since it contains OTA whose g_m can be electronically controllable via DC bias current.

B. Integer-Order Oscillator Design

The proposed voltage-mode oscillator with a single VDIBA, two resistors, and two capacitors, is shown in Fig. 2. Assuming that both capacitors C_i ($i = 1, 2$) are conventional (i.e. integer-order) ideal elements with capacitance C_1, C_2 and the used ABB is also ideal, i.e. for sake of simplicity not taking into account parasitic effects, the characteristic equation (CE) of this oscillator is as follows:

CE: $s^2 R_1 R_2 C_1 C_2 +$
$\qquad + s\left(R_1 C_1 + R_1 C_2 + 2R_2 C_2 - g_m R_1 R_2 C_2\right) +$ (2)
$\qquad + g_m R_2 + 1 = 0.$

According to (2), the oscillation starts-up condition (CO) will be:

CO: $R_1 \leq \dfrac{2R_2 C_2}{g_m R_2 C_2 - C_1 - C_2},$ (3)

while the frequency of oscillation (FO) is:

FO: $\omega_0 = \sqrt{\dfrac{1 + g_m R_2}{R_1 R_2 C_1 C_2}}.$ (4)
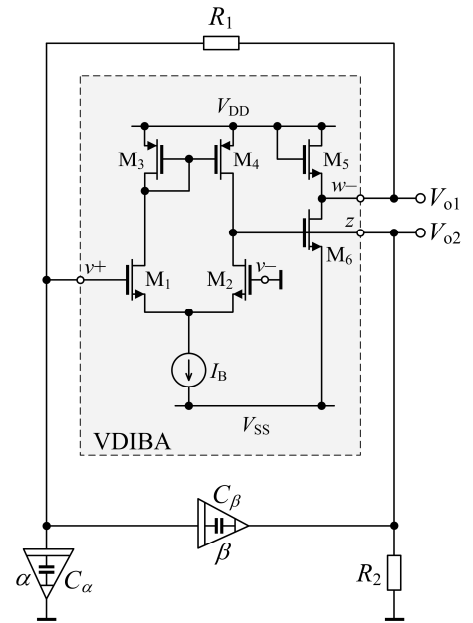

Fig. 2.   The proposed single VDIBA-based voltage-mode oscillator.

C. Fractional-Order Oscillator Design

The CE of the fractional-order system with FOCs (C_α, C_β) of impedances $Z_\alpha(s) = 1/(s^\alpha C_\alpha)$, $Z_\beta(s) = 1/(s^\beta C_\beta)$, can be described as:

CE: $s^{\alpha+\beta} R_1 R_2 C_\alpha C_\beta +$
$\qquad + s^\beta \left[R_1 C_\beta + 2R_2 C_\beta - g_m R_1 R_2 C_\beta\right] + s^\alpha R_1 C_\alpha +$ (5)
$\qquad + g_m R_2 + 1 = 0.$

By solving (5), the CO and FO of fractional-order oscillator can be obtained as (6) and (7), respectively. Note that setting $\alpha = \beta = 1$ in the expressions in (5)–(7), then the expressions in (2)–(4) are derived.
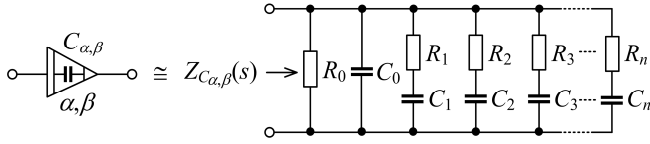
Fig. 3. Valsa RC network emulating behavior of fractional-order capacitor.

| VDIBA	
Transistors	*W/L (μm)/(μm)*
M_1–M_4	18/1.08
M_5, M_6	54/0.18
Parameter	*Value*
Bias current I_B (μA)	100
Transconductance gain g_m (μA/V)	598
Voltage gain V_w/V_z (β_o)	0.922
$f_{-3\,dB}$ @ g_m (MHz)	226.32
$f_{-3\,dB}$ @ V_w/V_z (GHz)	51.93
DC linearity V_{v+}; V_{v-} (mV)	±200
DC linearity V_w/V_z (mV)	$-0.9 \rightarrow +0.5$
Power consumption (mW)	10.5
Area (μm²)	97.2

TABLE III.   STANDARD EIA-96 COMPLIANT COMPONENT VALUES USED IN RC NETWORK DEPICTED IN FIG. 3 FOR $C_{0.5}$ = 37.3 nF·s$^{-0.5}$ IN FREQUENCY RANGE OF 1 MHZ–100 MHZ.

| Components	Values via Valsa Approximation
R_0 (Ω) / C_0 (F)	24 k / 0.5 p
R_1 (Ω) / C_1 (F)	11 k / 8 p
R_2 (Ω) / C_2 (F)	4.7 k / 2.5 p
R_3 (Ω) / C_3 (F)	1.6 k / 1 p
Total resistance (Ω) / capacitance (F)	
41.3 k / 12 p	
Spread of resistance / capacitance	
15 / 16	
Average / max. phase angle deviation (deg.)	
1.02 / 1.38	
|Relative phase error| (%)	
3.07	

III. SIMULATION RESULTS

The behavior of VDIBA shown in CMOS implementation of the proposed voltage-mode integer- and fractional-order oscillators has been verified by SPICE simulations. In the design, transistors are modeled by the TSMC 0.18 μm level-7 LO EPI SCN018 CMOS process. In simulations, the DC power supply voltages equal to $+V_{DD} = -V_{SS} = 0.9$ V. The aspect ratios of CMOS transistors in structures and their main parameters obtained with AC and DC analyses are listed in Table II.

In order to verify the workability of the three branches Valsa RC network structure [7] giving FOC behavior shown in Fig. 3, the phase, magnitude, pseudo-capacitance responses and relative phase error analysis are given in Fig. 4 within the frequency range of 1 MHz–100 MHz, while computed corresponding RC values are listed in Table III. As it can be seen in Fig. 4(b), in the constant phase zone the maximum relative phase error is 3.07% and corresponding absolute phase angle deviation about 1.38 degree. Next, as the first case, the performance of the proposed integer-order oscillator ($\alpha = \beta = 1$) was evaluated. In this case, both capacitances have
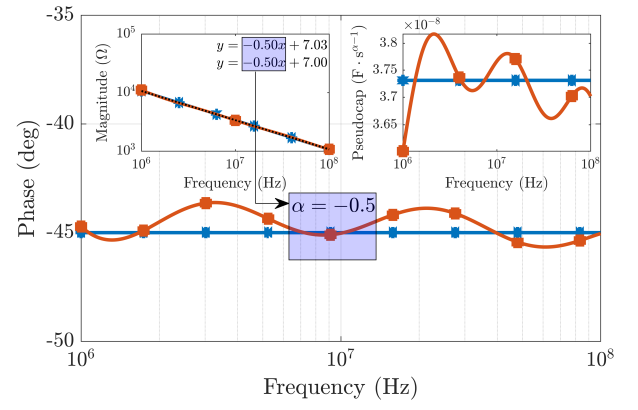
(a)
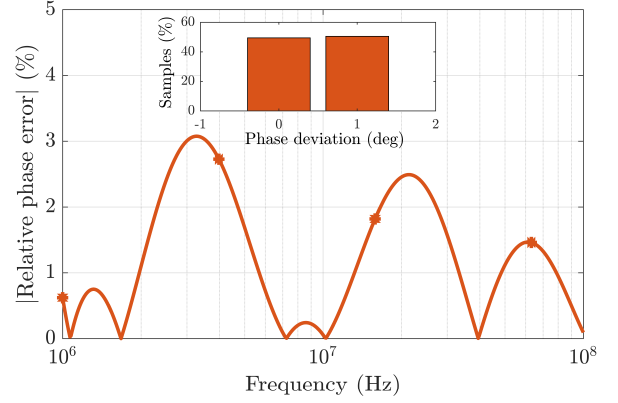
(b)

Fig. 4. Numerical simulation of three-branches Valsa RC network emulating fractional-order capacitor: (a) phase, pseudocapacitance, and magnitude responses, (b) relative phase errors and corresponding normalized histograms (%) in the frequency range of 1 MHz - 100 MHz.

been chosen as: $C_1 = C_2 = 4.7$ pF, while the resistor was: $R_1 = 4.3$ kΩ; according to (2) and $R_2 = 56$ kΩ. The theoretical value of the oscillation frequency was $f_0 = 12.8$ MHz. Figure 5(a) shows the simulated output waveforms with frequency of oscillation 10.03 MHz while the simulated total harmonic distortion (THD) is 4.84%. As the second case, the fractional-order oscillator with an order of $s^{1.5}$ has been implemented. For this purpose, the capacitor C_1 of the integer-order oscillator in Fig. 2 was replaced with its fractional-order equivalent, which was emulated using the three branches RC tree shown in Fig. 3. Note that the values of g_m, R_2, and C_2 have been kept the same with the previous case. Considering that $\alpha = 0.5$, its equivalent pseudo-capacitance value will be as follows: $C_\alpha \approx 37.3$ nF·s$^{-0.5}$ ($C_1 = 4.7$ pF @ 10.03 MHz). During simulations, in order to start up the oscillations, the resistor R_1 was set 7.5 kΩ and the obtained FO was $f_0 = 9.1$ MHz. The simulated output waveforms are shown in Fig. 5(b). As the last case, a fractional-order oscillator with $\alpha + \beta = 1$ has been investigated. Here, considering again the same values of g_m and R_2 as in integer-order case, the computed pseudo-capacitances for $\alpha = \beta = 0.5$ were $C_{\alpha,\beta} \approx 37.3$ nF·s$^{-0.5}$ ($C_{1,2} = 4.7$ pF @ 10.03 MHz), which after substituting in (6) the resulting condition of oscillation was $R_1 = 10$ kΩ. Figure 5(c) shows the output responses and simulated FO is equal to $f_0 = 5.4$ MHz while the simulated THD is 3.28%. In addition, the simulated
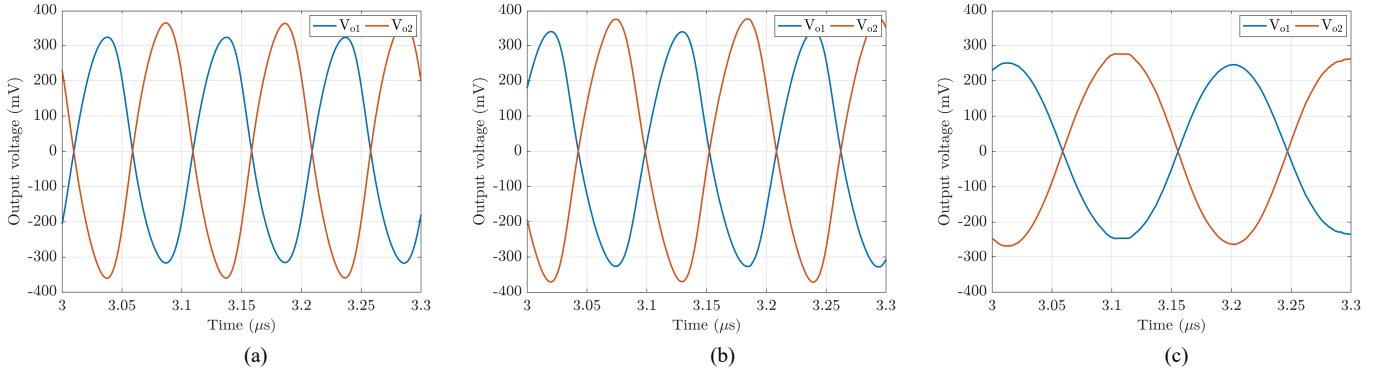
Fig. 5. Simulated output waveforms of the proposed voltage-mode oscillator: (a) $\alpha = \beta = 1$, (b) $\alpha = 1$, $\beta = 0.5$, (c) $\alpha = \beta = 0.5$.
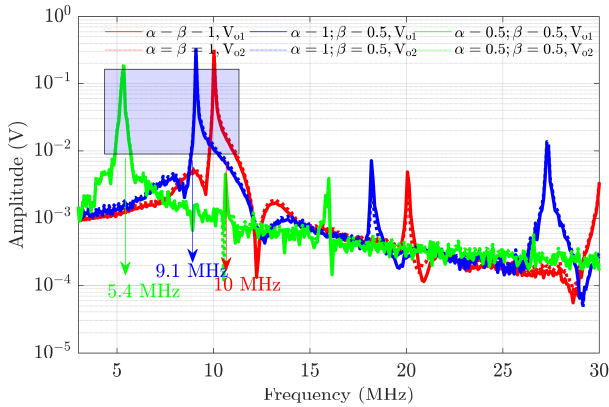

Fig. 6. Simulated frequency spectrum of outputs.

frequency spectrum of outputs for each case is given in Fig. 6. The total power dissipation of the oscillator in all three cases is found to be 10.5 mW.

IV. CONCLUSION

The integrated analog design of fractional-order oscillator design is studied. The proposed compact CMOS fractional-order oscillator behavior and performance was verified using SPICE simulations. Moreover, compared with the corresponding already introduced fractional-order oscillators, the proposed structures offer the benefit of low transistor count and, therefore, simplicity of its structure with decreasing FO.

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